BMBF TU9-IIT Mandi Workshop on

Current trends in Analog Circuit Designing

School of Computing and Electrical Engineering
IIT Mandi

BMBF TU9-IIT Mandi Workshop on "Current Trends in Analog Circuit Designing"

Agenda

Day 1 (Sept. 25, 2017)

9:00 am: Registrations for IIT Mandi students
9:30 am: Welcome note for the speakers from TU-Berlin by **Hitesh Shrimali** (10')
9:40 am: Part-I: Sigma delta modulators by **Friedel Gerfers** (55')
10:40 am: Coffee break (20')
11:00 am: Part-II: Sigma delta modulators by **Friedel Gerfers** (55')
12:00 pm: Lunch break
1:50 pm: Welcome note for the speakers from industry by Hitesh Shrimali (10')
2:00 pm: High Speed Wireline Communication by **Tapas Nandy** (55')
3:00 pm: High Speed Design Issues and Jitter Estimation Techniques
by **Jai Narayan Tripathi** (55')
4:00 pm: Coffee break (20')
4:20 pm: Case study: sigma delta modulator by **Marcel Runge** (45')

Day 2 (Sept. 26, 2017)

9:30 am: Part-III: Sigma delta modulators by **Friedel Gerfers** (55')
10:30 am: Coffee break (20')
10:50 am: Part-IV: Sigma delta modulators by **Friedel Gerfers** (55')
11:50 pm: Lunch break
1:50 pm: Welcome note for the speakers from industry by **Hitesh Shrimali** (10')
2:00 pm: Talk by **Nitin Gupta** (55')
3:00 pm: Design methodologies for state-of-the-art analog circuits by **Atul Bhargava** (55')
4:00 pm: Coffee break (20')
4:20 pm: Case study: sigma delta modulator by **Marcel Runge** (45')
5:00 pm: Closing ceremony (20')

Biographies of the speakers

Friedel Gerfers received the Dipl.-Ing. degree in electrical engineering from the Gerhard Mercator University, Duisburg, Germany, in 1996, and the Ph.D. degree in microsystems engineering from the Albert-Ludwig-University, Freiburg, Germany, in 2005. He has brought this commitment and expertise to several disciplines and different organizations in industry and academia. He has established himself as a leading architect of high-performance, high-bandwidth communications circuits and systems and low-power GS/s ADCs and DACs. With over 20 years of design, research and teaching experience, he has a proven track record in delivering cutting edge high-speed low-power and high-performance analog & mixed-signal circuits and systems. From 2003 to 2006, he was with Philips Semiconductor, Munich, Germany, leading the efforts on high-speed analog-to-digital converters and serial communication circuits for video applications. In 2006, he joined Intel Research, Santa Clara, CA, as a Senior Research Scientist. During his research fellowship, he developed an ultralow-noise MEMS accelerometer. Furthermore, he was Principal Investigator for ADC-based microelectromechanical system architectures. Prior to joining Alvand Technologies in 2011, he was Technical Director with Aquantia Inc., Milpitas, CA, where he developed multiple generations of high-volume 10 Gbase-T transceivers with best-in-class power efficiency for high-throughput networking switches. These products are now in mass production. As part of the acquisition of Alvand Technologies in 2012, he joined Integrated Device Technology Inc., San Jose, CA, where he is directing the R&D efforts and the portfolio of high resolution high-speed ADCs for 3/4G wireless applications. Since January 2015, Prof. Gerfers heads the "Mixed Signal Circuit Design (MSC)" department at the Faculty IV Electrical Engineering and Computer Science at the Berlin Institute of Technology, which is connected to a W3 professorship. He is coauthor of the book Continuous-Time Sigma-Delta A/D-Fundamentals, Performance Limits and Robust Implementations (Springer, 2006) and four other book chapters covering different topics. He authored and coauthored more than 40 papers and holds eight patents. He was appointed advisory board member of a leading EDA company. Dr. Gerfers is a member of the technical program committee of the European Solid-State Circuits Conference.

Tapas Nandy received the B. Eng. degree in electronics and telecommunication engineering from Bengal engineering college, Kolkata, India in and M. Tech. degree in microelectronics from Indian Institute of Technology, Kanpur, India. He currently is a director of R&D, High-Speed PHY, MSIP at Synopsis Inc. Prior to joining Synopsis Inc (2015), he worked for STMicroelectronics as a senior group manager of analog and mixed signal IP/high-speed links PHYs team. His research interests include High-Speed Link PHY designs and analog and mixed signal IPs. He holds 14 US and Europe patents and 6 international publications.

Nitin Gupta received B.E. Degree in Electronics and Communication from Indian Institute of technology Roorkee, India, in 1998. Currently, He is working as a Director at Western Digital. Previously, he worked for Synopsys and STMicroelectronics as well. He has 19 years of experience in analog and mixed-signal circuit design. His research interest includes High Speed Link Physical Layer, Analog and Mixed Signal IPs & Design Methodologies. Moreover, he architected various Analog & Mixed signal IPs from spec definition to production. He has strong knowledge of analog design, simulation & layout concepts. He holds 11 US patents and 6 IEEE international publications. Nitin is a Senior Member IEEE since 2013.

Jai Narayan Tripathi is currently a Technical Leader in STMicroelectronics, India. He received his Bachelor of Engineering (Electronics & Communication Engineering) in 2007 from M.L.V.T.& Engineering College (An institute of Govt. of Rajasthan), and Master of Technology (Information and Communication Technology) from DA-IICT, Gandhinagar in 2009, followed by Ph.D. (Electrical Engineering) from IIT Bombay, Mumbai in 2014. He has been working on design issues of high speed systems such as serial links, at STMicroelectronics. His areas of interest are signal integrity, power integrity, EMI/EMC, metaheuristic optimization, and RF circuits. Dr. Tripathi has served as a reviewer for many international journals, such as PIER, IEEE TEMC, IEEE TPES, Microelectronics Journal etc., and has been a TPC member for various international conferences. He has served as a Session Co-Chair for the session 'High-Speed Channels and Interconnects' in IEEE EDAPS 2015, held at Seoul (Korea). He was a recipient of Young Investigator Training Program (YITP) Research Award by Associazione Di Fondazioni EDi Casse Di Risparmio Spa, Italy in 2016 and 2017 consecutively. He has delivered invited talks in various universities including IIT Bombay, IIT BHU, IIIT Delhi etc. He has more than 40 international research publications to his credit. He was a Visiting Scientist at Politecnico Di Torino, Italy from April 2016 to May 2016 and from May 2017 to June 2017; where he was also a Visiting Postdoctoral Fellow from Aug. 2016 to Nov. 2016.

Atul Bhargava is currently a Senior Staff Engineer at STMicroelectronics, India. He has around 14 years experience with STMicroelectronics, India. He completed his bachelor degree and Master degree in 2002 and 2004, respectively. His area of interest are CAD Tools, Automation and Flows for Analog Design. He has published 31 national and international papers.

Marcel Runge received the B.Sc. in 2012 and the M.Sc. in 2015 from the Leibniz Universität Hannover, Germany both in electrical engineering and information technology. During a one-year internship at the Silicon Valley, USA based startup Aquantia Corp, he contributed to the high speed TX Digital-to-Analog-Converter design for 10GBase-T data communication in 28nm. While working on his Masters thesis at the company KLA-Tencor, USA, he developed a deep understanding of CCD sensor-readout architectures to maximize the signal-to-noise ratio. Currently, he is working towards the Ph.D. degree at MSC chair.