Dr. Rahul Shrestha

Curriculum Vitae

"Purity, patience, and perseverance are the three essentials to success, and above all, love." - Swami Vivekananda

Education

2009–2014 **Ph.D**, *Indian Institute of Technology Guwahati (VLSI Design Laboratory and National MEM Design Center).*

2004–2008 **Bachelor of Engineering (Specialized in Telecommunication Engineering)**, *Visveswaraiah Technological University*, B. M. S. College of Engineering, Bangalore, First Class.

2001–2003 **Intermediate studies (Specialized in physics, chemistry, mathematics and computer-science)**, *Government of Karnataka Pre-university Education Board*, American Pre-university College, Bangalore, First class.

2001 **Xth standard**, *Indian Certificate of Secondary Education (ICSE) Board*, West Point School Darjeeling, First Class.

Work Experience

August-2014 **Assistant Professor**, *Center for VLSI and Embedded System Technologies (CVEST), International Institute of Information Technology Hyderabad (IIIT-H).*
December-2016.

December-2016 **Assistant Professor**, *School of Computing & Electrical Engineering (SCEE), Indian Institute of Technology Mandi (IIT-M).*
Till Date.

May-2018 **Visiting Assistant Professor**, *Blekinge Institute of Technology (BTH), Sweden (Karlskrona).*
June-2018

Research Interests

Areas

- Computer architecture based on Posit arithmetic number systems.
- Hardware design for deep neural networks for artificial intelligence applications.
- Algorithm and VLSI architecture design for spectrum sensing in cognitive radio application.
- Digital architecture of communication baseband and CMOS circuitry of analog RF section for the transceiver of cognitive-radio wireless sensors.
- Reconfigurable channel decoder for the next-generation of wireless communication.
- System on Chip (SoC) design and implementation of high-speed digital-architectures.
- Algorithmic aspects of error-correcting codes (Turbo and LDPC codes) and VLSI architectures of efficient channel-decoders.
- Application-Specific-Integrated-Circuits (ASIC) and Field-Programmable-Gate-Array (FPGA) implementations of digital/analog/mixed-signal designs.

PhD topic VLSI Design and Implementation of High-Throughput Turbo Decoder for Wireless Communication Systems.

Supervisor Prof. Roy P. Paily.

Teaching Experience

Monsoon-2021 **Postgraduate Course in IIT-Mandi**, Analog CMOS Integrated-Circuit Design.

Spring-2021 **Undergraduate Course in IIT-Mandi**, Applied Electronics Laboratory.

Spring-2021 **Postgraduate Course in IIT-Mandi**, Digital VLSI Architecture Design.

Monsoon-2020 **Postgraduate Course in IIT-Mandi**, Analog CMOS Integrated-Circuit Design.

Spring-2020 **Postgraduate Course in IIT-Mandi**, Digital VLSI Architecture Design.

Monsoon-2019 **Undergraduate Course in IIT-Mandi**, Digital System Design.

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Assistant Professor - School of Computing & Electrical Engineering, IIT-Mandi.

Monsoon-2019 **Postgraduate Course in IIT-Mandi**, Digital MOS-LSI Circuit Design.

Monsoon-2019 **Postgraduate Course in IIT-Mandi**, CMOS Digital IC Design Practicum.

Spring-2019 **Undergraduate Course in IIT-Mandi**, Digital System Design Practicum.

Spring-2019 **Undergraduate Course in IIT-Mandi**, Applied Electronics Laboratory.

Monsoon-2018 **Postgraduate Course in IIT-Mandi**, Digital MOS-LSI Circuit Design.

Monsoon-2018 **Postgraduate Course in IIT-Mandi**, Digital VLSI Architecture Design.

Spring-2018 **Postgraduate Course in IIT-Mandi**, Digital MOS-LSI Circuit Design.

Monsoon-2017 **Postgraduate Course in IIT-Mandi**, CMOS Digital IC Design Practicum.

Monsoon-2017 **Postgraduate Course in IIT-Mandi**, Digital VLSI Architecture Design.

Spring-2017 **Postgraduate Course in IIT-Mandi**, Mixed Signal VLSI Design.

Monsoon-2016 **Postgraduate Course in IIIT-Hyderabad**, Analog Mixed Signal Design.

Monsoon-2016 **Undergraduate Course in IIIT-Hyderabad**, Embedded Hardware Design.

Spring-2016 **Postgraduate Course in IIIT-Hyderabad**, Digital VLSI Architecture Design.

Spring-2016 **Undergraduate Course in IIIT-Hyderabad**, Basic Electronics Laboratory.

Spring-2016 **Undergraduate Course in IIIT-Hyderabad**, Electronics Workshop - II.

Monsoon-2015 **Postgraduate Course in IIIT-Hyderabad**, Analog Mixed Signal Design.

Monsoon-2015 **Undergraduate Course in IIIT-Hyderabad**, Embedded Hardware Design.

Spring-2015 **Postgraduate Course in IIIT-Hyderabad**, Digital VLSI Architecture Design.

Spring-2015 **Undergraduate Laboratory in IIIT-Hyderabad**, Electronics & Communication Laboratory.

2012 **Laboratory**, Worked as teaching assistant of digital IC design lab and electronics circuit design lab for M. Tech VLSI and B. Tech courses, respectively, in the Indian Institute of Technology Guwahati (IITG).

2011 **Laboratory**, Worked as teaching assistant of VLSI system design lab and analog circuit design lab for M. Tech VLSI course in the Indian Institute of Technology Guwahati (IITG).

2010 **Tutorial**, Conducted tutorial classes for electrical network analysis, basic electronics and electrical instrumentation courses for the first year B. Tech Students in the Indian Institute of Technology Guwahati (IITG).

Publications

Peer Reviewed Journals

- Rohit B. Chaurasiya and **Rahul Shrestha**, "*Hardware-Efficient VLSI-Architecture and ASIC-Implementation of GRCR based Cooperative Spectrum Sensor for Cognitive-Radio Network*," **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Available Online in Early Acess (DOI: 10.1109/TVLSI.2021.3114859), October-2021.
- Anuj Verma and **Rahul Shrestha**, "*Hardware-Efficient and High-Throughput LLRC Segregation Based Binary QC-LDPC Decoding Algorithm and Architecture*," **IEEE Transactions on Circuits and Systems II: Express Briefs**, Volume: 68, Issue: 8, pp. 2835-2839, August-2021.
- Rohit B. Chaurasiya and **Rahul Shrestha**, "*Area-Efficient and Scalable Data-Fusion based Cooperative Spectrum Sensor for Cognitive Radio*," **IEEE Transactions on Circuits and Systems II: Express Briefs**, Volume: 68, Issue: 4, pp. 1198-1202, April-2021.
- Rohit B. Chaurasiya and **Rahul Shrestha**, "*A New Hardware-Efficient Spectrum-Sensor VLSI-Architecture for Data Fusion based Cooperative Cognitive-Radio Network*," **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Volume: 29, Issue: 4, pp. 760-773, February-2021.
- **Rahul Shrestha**, "*A Multiple-Radix MAP-Decoder Microarchitecture and its ASIC Implementation for Energy-Efficient and Variable-Throughput Applications*," **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Volume: 29, Issue: 1, pp. 65-75, January-2021.
- Rohit B. Chaurasiya and **Rahul Shrestha**, "*Fast Sensing-Time and Hardware-Efficient Eigenvalue based Blind Spectrum Sensors for Cognitive Radio Network*," **IEEE Transactions on Circuits and Systems I: Regular Papers**, Volume: 67, Issue: 4, pp. 1296-1308, April-2020.
- Rohit B. Chaurasiya and **Rahul Shrestha**, "*Hardware-Efficient and Fast Sensing-Time Maximum-Minimum-Eigenvalue based Spectrum Sensor for Cognitive Radio Network*," **IEEE Transactions on Circuits and Systems I: Regular Papers**, Volume: 66, Issue: 11, pp. 4448-4461, November-2019.
- **Rahul Shrestha** and Abhijit Sahoo, "*High-Speed and Hardware-Efficient Successive Cancelation Polar-Decoder*," **IEEE Transactions on Circuits and Systems II: Express Briefs**, Volume: 66, Issue: 7, pp. 1144–1148, October-2019.
- Mahesh S. Murty and **Rahul Shrestha**, "*Reconfigurable and Memory-Efficient Cyclostationary Spectrum Sensor for Cognitive-Radio Wireless Networks*," **IEEE Transactions on Circuits and Systems II: Express Briefs**, Volume: 65, Issue: 8, pp. 1039–1043, August-2018.
- Mahesh S. Murty and **Rahul Shrestha**, "*Hardware Implementation and VLSI Design of Spectrum Sensor for Next-Generation LTE-A Cognitive-Radio Wireless-Network*," **IET Circuits, Devices and Systems**, Volume: 12, Issue: 5, pp. 542–550, August-2018.
- Naman Govil, **Rahul Shrestha** and Shubhajit Roy Chowdhury, "*PGMA: An Algorithmic Approach for Multi-objective Hardware Software Partitioning*," **Journal of Microprocessors and Microsystems: Embedded Hardware Design (MICPRO) - Elsevier**, Volume: 54, pp. 83–96, October-2017.
- **Rahul Shrestha** and Roy Paily, "*Memory-Reduced Maximum-A-Posteriori-Probability Decoding for High-Throughput Parallel-Turbo Decoders*," **Journal of Circuits, Systems, and Signal Processing**, Volume: 35, Issue: 8, pp. 2832–2854, August-2016.
- Vijaya Kumar K, **Rahul Shrestha** and Roy Paily, "*Multi-Standard High-Throughput and Low-Power QC-LDPC Decoder for WiMAX and WiFi Standards*," **IET Circuits, Devices and Systems**, Volume: 10, Issue: 2, pp. 111–120, March-2016.
- **Rahul Shrestha** and Roy Paily, "*VLSI Design and Hardware Implementation of High-Speed Energy-Efficient Logarithmic-MAP Decoder*," **Journal of Low Power Electronics**, Volume: 11, Issue: 3, pp. 406–412, September-2015.
- Sachin Kumawat, **Rahul Shrestha**, Nikunj Daga and Roy Paily, "*High-Throughput LDPC-Decoder Architecture Using Efficient Comparison Techniques and Dynamic Multi-Frame Processing Schedule*," **IEEE Transactions on Circuits and Systems I: Regular Papers**, Volume: 62, Issue: 5, pp. 1421–1430, May-2015.
- **Rahul Shrestha** and Roy Paily, "*High-Throughput Turbo Decoder with Parallel Architecture for LTE Wireless Communication Standards*," **IEEE Transactions on Circuits and Systems I: Regular Papers**, Volume: 61, Issue: 9, pp. 2699–2710, September-2014.
- **Rahul Shrestha** and Roy Paily, "*Comparative Study of Simplified MAP Algorithms and an Implementation of Non-Parallel-Radix-2 Turbo Decoder*," **Journal of Signal Processing Systems**, Volume: 81, Issue: 2, pp. 305–320 , September-2014.
- **Rahul Shrestha** and Roy Paily, "*Performance and Throughput Analysis of Turbo Decoder for the Physical Layer of Digital-Video-Broadcasting-Satellite-Services-to-Handhelds (DVB-SH) Standard*," **IET Communications**, Volume: 7, Issue: 12, pp. 1211–1220, 2013.
- **Rahul Shrestha** and Roy Paily, "*Design and Implementation of a Linear Feedback Shift Register Interleaver for Turbo Decoding*," **Springer Berlin/Heidelberg Lecture Notes in Computer Science**, Volume: 7373, pp. 30–39, 2012.

International Conferences

- Rohit B. Chaurasiya and **Rahul Shrestha**, "*Hardware-Efficient ASIC Implementation of Eigenvalue Based Spectrum Sensor Reconfigurable-Architecture for Cooperative Cognitive-Radio Network*," **IEEE International Symposium on Circuits and Systems (ISCAS)**, pp. 1-5, May-2021.
- Anuj Verma and **Rahul Shrestha**, "*A New VLSI Architecture of Next-Generation QC-LDPC Decoder for 5G New-Radio Wireless-Communication Standard*," **IEEE International Symposium on Circuits and Systems (ISCAS)**, pp. 1-5, October-2020.
- **Rahul Shrestha** and Shubham Telgote, "*A Short Sensing-Time Cyclostationary Feature Detection Based Spectrum Sensor for Cognitive Radio Network*," **IEEE International Symposium on Circuits and Systems (ISCAS)**, pp. 1-5, October-2020.
- Anuj Verma and **Rahul Shrestha**, "*A New Partially-Parallel VLSI-Architecture of Quasi-Cyclic LDPC Decoder for 5G New-Radio*," **33rd IEEE International Conference on VLSI Design and 19th International Conference on Embedded Systems (VLSID)**, pp. 1-5, January-2020.
- Rohit B. Chaurasiya and **Rahul Shrestha**, "*Hardware-Efficient and Low Sensing-Time VLSI-Architecture of MED based Spectrum Sensor for Cognitive Radio*," **IEEE International Symposium on Circuits and Systems (ISCAS)**, pp. 1-5, May-2019, Japan (Sapporo).
- **Rahul Shrestha**, Pooja Bansal and Srikant Srinivasan, "*High-Throughput and High-Speed Polar-Decoder VLSI-Architecture for 5G New Radio*," **32nd IEEE International Conference on VLSI Design and 18th International Conference on Embedded Systems (VLSID)**, pp. 329-334, January-2019.
- **Rahul Shrestha** and Ashutosh Sharma, "*VLSI-Architecture of Radix-2/4/8 SISO Decoder for Turbo Decoding at Multiple Data-rates*," **26th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)**, pp. 131-136, October-2018, Italy (Verona).
- Rohit Chaurasiya, John Gustafson, **Rahul Shrestha**, Jonathan Neudorfer, Sangeeth Nambiar, Kaustav Niyogi, Farhad Merchant and Rainer Leupers, "*Parameterized Posit Arithmetic Hardware Generator*," **36th IEEE International Conference on Computer Design (ICCD)**, USA (Orlando, Florida), October-2018, In Press.
- Sweeta Ghosh, Vikram Thakur, **Rahul Shrestha**, Vinayak Hande and Shubhajit Roy Chowdhury, "*Design and Simulation of Low Cost and Low Magnetic Field MRI System*," **12th International Conference on Sensor Technologies and Applications (SENSORCOMM)**, Italy (Venice), September-2018, In Press.
- **Rahul Shrestha** and Ashutosh Sharma, "*Reconfigurable VLSI-Architecture of Multi-Radix Maximum-A-Posteriori Decoder for New Generation of Wireless Devices*," **22nd IEEE International Symposium on VLSI Design and Test (VDAT)**, June-2018, In Press.
- Mahesh S. Murty and **Rahul Shrestha**, "*Hardware-Efficient and Wide-Band Frequency-Domain Energy Detector for Cognitive-Radio Wireless Network*," **31st IEEE International Conference on VLSI Design and the 17th International Conference on Embedded Systems (VLSID)**, pp. 277-282, January-2018.
- Dinesh Kumar B., Sumit Pandey, Puneet Arora and **Rahul Shrestha**, "*A Self-Bandwidth Switching & Area-Efficient PLL Using Multiplexer-Controlled Frequency Selector*," **7th IEEE International Symposium on Embedded Computing and System Design (ISED)**, pp. 1-5, December-2017.
- Rahul Kurzekar, Hardik Arora and **Rahul Shrestha**, "*Embedded Hardware Prototype for Gas Detection and Monitoring System in Android Mobile Platform*," **3rd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, pp. 6-10, December-2017.
- Sumanth Gudaparthi and **Rahul Shrestha**, "*Energy-Efficient VLSI Architecture & Implementation of Bi-Modal Multi-Banked Register-File Organization*," **21st IEEE International Symposium on VLSI Design and Test (VDAT)**, pp. 299-312, December-2017.
- Naman Govil, **Rahul Shrestha** and Shubhajit Roy Chowdhury, "*A New Multi-Objective Hardware-Software-Partitioning Algorithmic Approach for High Speed Applications*," **21st IEEE International Symposium on VLSI Design and Test (VDAT)**, pp. 62-68, December-2017.
- **Rahul Shrestha**, "*High-Speed and Low-Power VLSI-Architecture for Inexact Speculative Adder*," **IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT)**, pp. 1-4, April-2017, Hsinchu, Taiwan.
- Enna Sachdeva, Pratik Porwal, Nalini Vidyulatha and **Rahul Shrestha**, "*Design of Low power VLSI-Architecture and ASIC Implementation of Fuzzy Logic based Automatic Car-Parking System*," **13th International IEEE India Conference (INDICON)**, pp. 1-6, December-2016.

- Soumitr Sanjay Dubey, **Rahul Shrestha** and Shubhajit Roy Chowdhury, "*A Novel Architecture for Computing Eigenvalues of Matrix for High Speed Applications*," **13th International IEEE India Conference (INDICON)**, pp. 1-5, December-2016.
- Lalit Kumar, Deepak Kumar Mittal and **Rahul Shrestha**, "*VLSI-Design and FPGA-Implementation of GMSK-Demodulator Architecture Using CORDIC Engine for Low-Power Application*," **13th International IEEE India Conference (INDICON)**, pp. 1-6, December-2016 (Best Poster Awarded).
- Gayatri Nair, Swathi Ramasahayam, **Rahul Shrestha** and Shubajit Roy Chowdhury, "*Non-Invasive Estimation of Blood Parameters from Composite Signal Using Near Infrared Spectroscopy Coupled with Independent Component Analysis*," **38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)**, August-2016, Orlando, USA.
- Mahesh S. Murty and **Rahul Shrestha**, "*VLSI Architecture for Cyclostationary Feature Detection based Spectrum Sensing for Cognitive-Radio Wireless Networks and Its ASIC Implementation*," **IEEE Computer Society Annual Symposium on VLSI (ISVLSI)**, pp. 69-74, July-2016, Pittsburgh, USA.
- **Rahul Shrestha**, Vinay Swargam and Mahesh S. Murty, "*Cognitive-Radio Wireless-Sensor Based on Energy Detection with Improved Accuracy: Performance and Hardware Perspectives*," **20th IEEE International Symposium on VLSI Design and Test (VDAT)**, Accepted & Presented, May-2016.
- **Rahul Shrestha** and Utkarsh Rastogi, "*Design and Implementation of Area-Efficient and Low-Power Configurable Booth-Multiplier*," **29th IEEE International Conference on VLSI Design and the 15th International Conference on Embedded Systems (VLSID)**, pp. 599-600, January-2016.
- **Rahul Shrestha** and Roy Paily, "*Hardware Implementation and Testing of Log-MAPP Decoder Based on Novel Un-Grouped Sliding-Window Technique*," **IEEE 5th International Symposium on Electronics System Design (ISED)**, pp. 171 - 175, 2014 (Best Paper Awarded).
- Vijaya Kumar K, **Rahul Shrestha** and Roy Paily, "*Design and Implementation of Multi-Rate LDPC Decoder for IEEE 802.16e Wireless Standard*," **IEEE International Conference on Green Computing, Communication and Electrical Engineering (ICGCCEE)**, pp. 1 - 5, 2014.
- **Rahul Shrestha** and Roy Paily, "*System Level Hardware Testing of a High Speed MAP Decoder Implemented on FPGA*," **IEEE International Conference on Signal Processing, Computing and Control (ISPCC)**, pp. 1 - 6, 2013.
- **Rahul Shrestha** and Roy Paily, "*A Novel State Metric Normalization Technique for High-Throughput Maximum-a-Posteriori-Probability Decoder*," **IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI)**, pp. 903 - 907, 2013.
- **Rahul Shrestha** and Roy Paily, "*Design and Implementation of a High Speed MAP Decoder Architecture for Turbo Decoding*," **26th IEEE International Conference on VLSI Design and the 12th International Conference on Embedded Systems (VLSID)**, pp. 86 - 91, 2013.
- **Rahul Shrestha** and Roy Paily, "*Design and Data Width Requirement for Fixed Point Turbo Decoders Based on Modified MAP algorithm*," **IEEE International Conference on Signal Processing and Communications (SPCOM)**, pp. 1 - 5, 2012.
- **Rahul Shrestha** and Roy Paily, "*Hardware Implementation of Max-Log-MAP Algorithm Based on Maclaurin Series for Turbo Decoder*," **IEEE International Conference on Communications and Signal Processing (ICCSP)**, pp. 509 - 511, 2011.

Awards and Honors

2021 **Awarded with "Teaching Honour Roll Award" for consistent teaching performance that is highly appreciated by the student community**, *Indian Institute of Technology (IIT) Mandi*, Received this award from the Chief Minister of Himachal Pradesh, Shri Jai Ram Thakur.

2020 **Elevated to Senior Member**, IEEE, USA.

2015 **Start-up Research Grants for Young Scientists**, Granted by Department of Science and Technology (DST) - Government of India, for the project entitled "ASIC Chip-Tapeout of Reconfigurable Multiple Radix Parallel-Turbo Decoder for Next-Generation Wireless-Communication Systems".

2014 **Winner**, of the Design Contest in 27th IEEE International Conference on VLSI Design and the 13th International Conference on Embedded Systems, for the work entitled "Hardware Implementation and Testing of LMAPP Decoder for High-Throughput Applications", held at the Indian Institute of Technology Bombay (IITB).

2012 **Reviewer**, "IEEE Transactions on Circuits and Systems I", "IEEE Transactions on Circuits and Systems II", "IEEE Transactions on VLSI Systems", "Integration, the VLSI Journals", "IET Circuits, Devices and Systems" and "IET Communications".

2012 **Membership**, Full member of IEEE technical society.

2011 **Fellowship at VLSID-2011**, Awarded fellowship by Indian Institute of Technology Madras to attain the tutorials and workshops at IEEE VLSID-2011 conference.

2009 **Graduate Aptitude Test Examination (GATE)**, Qualified GATE and cleared interview at Indian Institute of Technology Guwahati for admission in Ph.D program.

2006 **WIPRO Technology**, Placed in WIPRO Technology during the placement session in B. M. S College of Engineering Bangalore.

2004 **Karnataka Common Entrance Test (K-CET)**, Secured 525^{th} state rank in K-CET for engineering admission.

2002 **Table Tennis**, Held third position in inter college table tennis tournament in Bangalore.

2002 **Best Student Award**, Awarded by American Pre-unversity College Bangalore for academic excellence.

2000 **Table Tennis**, Winner of Darjeeling district level men's under-19 open table tennis tournament.

2000 **Blue Coat Holder of the year**, Awarded for the best all rounder student, by West Point School Darjeeling, with a full scholarship of one year.

1999 **Table Tennis**, Winner of inter ICSE-school table tennis tournament in B-division category.

Workshops Conducted

2014 **IEEE Workshop on MEMS and VLSI Digital Design Flow**, Organized by IEEE Student Branch, Indian Institute of Technology Guwahati.
February 08–09.

2014 **CADENCE Workshop - 2014, Schematic & Layout Design Flow in Cadence**, Organized by Department of Electronics and Communication Engineering, National Institute of Technology Meghalaya (Shillong).
January 16–18.

2012 **INUP Familiarization Workshop on "Nanofabrication Technologies" for North-East Region, India**, Organized by Indian Institute of Science Bangalore in association with Indian Institute of Technology Guwahati.
September 28–29.

2011 **Digital Design - Functional Verification, Synthesis and RTL to GDS II flow using tools from *Cadence* and *Synopsys***, Organized by VLSI Design Lab. at Indian Institute of Technology Guwahati.
21–22 April.

Personal Details & Interest

Date of Birth	**27^{th} of July 1985.**
Nationality	**Indian.**
Martial Status	**Married.**
Sports	**Table tennis.**
Musical Instrument	**Guitar.**

References

1. **Prof. Roy P. Paily**, *Room No. 103, Department of Electronics and Electrical Engineering*, Indian Institute of Technology Guwahati, Ph No. +91-361-2582512.
Email Address: *roypaily@iitg.ac.in.*
2. **Prof. Anupam Chattopadhayay**, *School of Computer Science and Engineering*, Nanyang Technological University, 50 Nanyang Avenue, Singapore, Ph No. +65-9174-1272.
Email Address: *anupam@ntu.edu.sg.*
3. **Prof. Shaik Rafi Ahamed**, *Room No. 304, Department of Electronics and Electrical Engineering*, Indian Institute of Technology Guwahati, Ph No. +91-361-2582520.
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