Anuj VERMA

Ph.D. Research Scholar (Google Scholar)

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+91 9958-612862 Bengaluru, Karnataka Indian Citizen

Passionate and accomplished PhD in VLSI, with a strong foundation in Digital VLSI architecture and hands-on experience in cutting-edge ASIC (RTL-to-GDS) designing. Eager to contribute to cutting-edge research and development, cutting-edge projects, and inspire the next generation of engineers in the evolving landscape of VLSI technology. Be Happy and Make Others Happy.

ACADEMIC QUALIFICATIONS

February 2018 – August 2024 | Doctorate of Philosophy, SCHOOL OF COMPUTING AND ELECTRICAL ENGINEERING, IIT Mandi

- **Efficient VLSI-Architectures and ASIC-Fabrication of Channel Decoder for Contemporary Wireless-Communication Systems:-** This thesis exploits various hardware-efficienct and high-throughput LDPC decoder archietctures for 5G-NR networks. Various hardware-friendly LDPC decoding algorithms has been proposed that reduces the routing and computational complexity. Finally, a reconfigurable channel (LDPC/polar) decoder has been **ASIC fabricated** that are compliant to mMTC and URLLC applications of the 5G-NR wireless-communication standard.
- **Final Grade** : 8.69 out of 10.
- Supervisor : **Dr. Rahul Shrestha**.

Digital Architectures | ASIC and FPGA Methodologies | RTL Coding Techniques | Timing Constraints | Physical Designing | Algorithms-to-Architectures Designing | 5G New Radio

July 2015 – June 2017 | Master of Technology | VLSI Design, ECE DEPARTMENT, DCRUST Murthal

- Design methodology of analog and digital circuits designing in 180nm CMOS Technology. FPGA implementation of peripheral component interconnect express (PCIe) interface using verilog HDL.
- **Final Grade** : 8.24 out of 10.
- Supervisor : **Dr. Pawan Kumar Dahiya**.

Physical Layer | Point-to-Point Communication | PCIe | PCI | PCI-X | AGP

July 2009 – June 2013 | Bachelor of Technology | ECE Department, IPEC, UPTU Lucknow

- Fundamental aspects of electronics devices, circuits and systems. Study of various modulation techniques & MATLAB implementation of various modulation schemes for communication applications.
- **Final Percentage** : 66.13.
- Supervisor : **Dr. Priyanka**.

FSO communication | MATLAB | ASK | FSK | BPSK | QPSK

July 2008 – June 2009 | Senior Secondary Education, S.D. INTER COLLEGE, UP Board

- **Final Percentage** : 69.00.

Mathematics | Physics | Chemistry

July 2006 – June 2007 | Secondary Education, S.D. INTER COLLEGE, UP Board

- **Final Percentage** : 64.00.

Mathematics | English

PROFESSIONAL EXPERIENCES

July 2024 – Present | Chief Engineer, SAMSUNG RESEARCH & DEVELOPMENT INSTITUTE, Bengaluru, India

- The project aims to leverage the flexibility and extensibility of RISC-V to create a highly efficient, scalable, and low-power solution for various image processing tasks. By optimizing the instruction set and hardware accelerators, the architecture is designed to handle complex image processing algorithms with improved performance, power, area (PPA), with reduced latency.

RISC V | Custom Instructions | Image Processing | Contrast Limited Adaptive Histogram Equalization (CLAHE)

March 2023 – September 2023 | Ph.D. Research Intern, SAMSUNG RESEARCH INSTITUTE, Bengaluru, India

- I designed a framework for architectural-level area and energy estimation tailored for custom hardware accelerators and digital architectures, involves integrating RTL and analytical modeling across various technology nodes. The goal is to develop a comprehensive area/energy estimator framework that optimizes both the design and performance of these digital architectures.

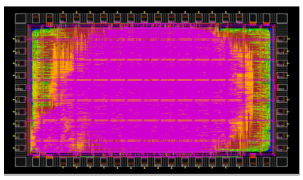
Area/Energy Estimators | RTL modelling | Analytical Modelling

July 2017 – January 2018 | **Senior Associate, Genpact Headstrong Capital Markets, Noida, India**

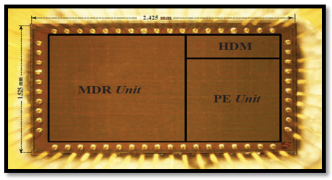
- I worked on configuring computer software or robots with Robotic Process Automation (RPA) to replicate human actions. These RPA robots interact with the user interface to capture data, manipulate applications, and perform tasks just as humans would.

Automation Anywhere | Openspan | Blue Prism

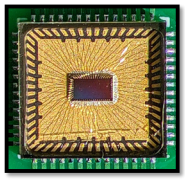
Ph.D. Research Work



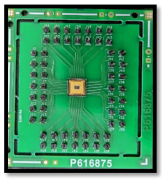
(a)



(b)



(c)



(d)

Our research work is mainly focused on the **reconfigurable low-density parity-check (LDPC) and polar channel decoder** with the exact specifications for **fifth-generation New Radio (5G NR) wireless communication standand**. We have implemented a **hardware-efficient VLSI architecture** (Click here) and **high-throughput digital architecture** (Click here) for LDPC decoder that is complaint to 5G NR standard and these designs are place and routed on the field-programmable logic array (FPGA) platform. Futher, We proposed hardware-efficient and high-throughput **log-likelihood-ratio compound (LLRC) segregation technique based algorithm and digital architecture** (Click here) of LDPC decoder. We also suggested a **simplified offset-minsum (SOMS) LDPC decoding algorithm** that alleviate the lower computational-complexity and its corresponding high-throughtput LDPC decoder architecture is also presented. The SOMS based LDPC decoder has been **FPGA prototyped and ASIC synthesized** (Click here) in the **90nm technology**. Finally, We **fabricated an ASIC for reconfigurable LDPC and polar channel decoder architecture** (Click here) that is complaint to **mMTC and URLLC application** of 5G-NR wireless communication standard. The **ASIC fabricated chip layout design, die-micrograph, QFN-packaged die, and chip printed circuit board (PCB) of reconfigurable channel decoder** are represented in **Figure (a)-(d), respectively.**

Ph.D. Thesis Title	**Efficient VLSI-Architectures and ASIC-Fabrication of Channel Decoder for Contemporary Wireless-Communication Systems**
Supervisor	**Dr. Rahul Shrestha**, Associate Professor, School of Computing & Electrical Engineering (SCEE), **IIT Mandi**, (Website)

Publications

July 2024	**Anuj Verma**, Rahul Shrestha, "High-Throughput and Hardware-Efficient ASIC-Chip Fabrication of Reconfigurable LDPC/Polar Decoder for mMTC and URLLC 5G-NR Applications", **IEEE Transactions on Circuits and Systems I : Regular Papers**, Jul. 2024 (**Early Access**). (Click here)
January 2023	**Anuj Verma**, Rahul Shrestha, "Low Computational-Complexity SOMS-Algorithm and High-Throughput Decoder Architecture for QC-LDPC Codes", **IEEE Transactions on Vehicular Technology**, vol. 72, no. 1, pp. 66-80, Jan. 2023. (Click here)
August 2021	**Anuj Verma**, Rahul Shrestha, "Hardware-Efficient and High-Throughput LLRC Segregation Based Binary QC-LDPC Decoding Algorithm and Architecture", **IEEE Transactions on Circuits and Systems II : Express Briefs**, vol. 68, no. 8, pp. 2835-2839, Aug. 2021. (Click here)
May 2020	**Anuj Verma**, Rahul Shrestha, "A New VLSI Architecture of Next-Generation QC-LDPC Decoder for 5G New-Radio Wireless-Communication Standard", **IEEE International Symposium on Circuits and Systems (ISCAS)**, pp. 1-5, May-2020.(Click here)
January 2020	**Anuj Verma**, Rahul Shrestha, "A New Partially-Parallel VLSI-Architecture of Quasi-Cyclic LDPC Decoder for 5G New-Radio", **33rd IEEE International Conference on VLSI Design and 19th International Conference on Embedded Systems (VLSID)**, pp. 1-6, January-2020.(Click here)
August 2017	**Anuj Verma**, Pawan Kumar Dahiya, "PCIe BUS : A State-of-the-Art-Review", **IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)**, Volume 7, Issue 4, PP 24-28, August-2017. (Click here)
March 2017	Kapil Kumar Sain, **Anuj Verma**, Priyanka, "Design and Implementation of Low Power D Flip-Flop in Cadence Virtuoso Tool", **2nd National Conference MANTHAN-2016 on Recent Trends in Computing and Communication Technologies (RCCT)**, March-2017.
September 2016	**Anuj Verma**, Pawan Kumar Dahiya, "Addressing the Key Dispersion Algorithm and Security in RFID Tag-Reader MAP", **1st National Conference MANTHAN-2016 on Recent Trends in Computing and Communication Technologies (RCCT)**, September-2016.

Technical Skills

VLSI Design Tools	Design Compiler and **Genus** for RTL Synthesis, VCS and **NCLaunch** for Functional Verification, **Innovus** for Physical Design flow, **Virtuoso schematic editor**, **Vivado (2018.2)** and ISE Design Suite for FPGA Based System Design, **ModelSim**, Symica, Magic VLSI Layout, Qflow.
Subjects	**Digital Architectural Designing**, **Digital MOS LSI Circuits**, **CMOS Designing**, **Digital Communication**, Digital & Analog Electronics, Electronics Devices and Circuits.
Hardware Language	**Verilog**, **System Verilog**, **SystemC**, VHDL.
Programming Language	C, Microsoft .Net, My SQL.
System Simulation Tool	MATLAB
Documentation Tool	Latex

Academic Teaching Assitantship

Feb'18-Aug'22 **Teaching Assistant**, School of Computing and Electrical Engineering, **Indian Institute of Technology Mandi**.

- **Digital VLSI Architecture Design** course and laboratory sessions for **M.Tech and Ph.D.** students.
- **Digital MOS LSI Design** course and laboratory sessions for **M.Tech and Ph.D.** students.
- **Digital System Design** and **Digial IC Design** laboratory sessions for **B.Tech** students.
- **Computer Architecture and Organisation** course and laboratory sessions for **B.Tech** students.
- **Applied Electronics** laboratory sessions for **B.Tech** students

Aug'15-May'17 **Teaching Assistant**, ECE Department, **Deenbandhu Chhotu Ram University of Science and Technology (DCRUST), Murthal, Sonipat**.

- **Digital CMOS IC Design** course and laboratory sessions for **M.Tech** students.
- **Verilog based Digital System Design** course and laboratory sessions for **M.Tech** students.
- **Digital Electronics** laboratory sessions for **B.Tech** students.

Membership of Professional Bodies

Membership	**Graduate Student Member**, Institute of Electrical and Electronics Engineers (IEEE).
Membership	Institute of Electrical and Electronics Engineers (IEEE) **circuits and systems (CAS) society**.
Membership	Institute of Electrical and Electronics Engineers (IEEE) **solid-state circuits society (SSCS)**.
IEEE Reviewer	**Transactions on Circuits and Systems I : Regular Papers**.
IEEE Reviewer	**Transactions on Circuits and Systems II : Express Briefs**.
IEEE Reviewer	**International Symposium on Circuits and Systems (ISCAS) conference** organized by **IEEE circuits and systems (CAS) society**.
IEEE Reviewer	**International MidWest Symposium on Circuits and Systems (MWSCAS) conference** organized by **IEEE circuits and systems (CAS) society**.
IEEE Reviewer	**Asia Pacific Conference on Circuits and Systems (APCCAS) conference** organized by **IEEE circuits and systems (CAS) society**.

Certifications

January 2023	International Conference on **36th IEEE International Conference on VLSI Design and 22nd International Conference on Embedded Systems (VLSID)** organized by AMD Semiconductor and VLSI seciety of India.
December 2022	International Workshop on **5G and Beyond : What is next ?** certified by Department of Electrical Engineering, IIT Kanpur.
October 2020	International Conference on **IEEE International Symposium on Circuits and Systems (ISCAS)** organized by IEEE circuits and systems (CAS) society.
January 2020	International Conference on **33rd IEEE International Conference on VLSI Design and 19th International Conference on Embedded Systems (VLSID)** organized by Qualcomm Semiconductor company.
January 2019	International Conference on **32nd IEEE International Conference on VLSI Design and 18th International Conference on Embedded Systems (VLSID)** organized by NXP Semiconductor company.
December 2018	International Workshop on **A Hands-on Introduction to Modern Wireless Systems : Theory and Simulation** certified by Department of Electrical Engineering, IIT Kanpur.
November 2018	Certification of Excellence for **International Workshop on Nano/Micro 2D-3D Fabrication, Manufacturing of Electronic-Biomedical Devices & Applications (IWNEBD)** certified by C4DFED, IIT Mandi.
July 2016	Summer Training in **VLSI design using VERILOG and FPGA** certified by DKOP Labs Private Limited.
July 2012	Industrial Training on **Communication Techniques** certified by Bharat Sanchar Nigam Limited (BSNL).
April 2012	Workshop on **Cyborg-The Robotics Workshop** conducted by KYRION ROBOTICS CLUB, IIT Kharagpur.

Honors and Awards

January 2023	**Fellowship Awarded** by AMD semiconductor and VLSI society of India at **36th IEEE International Conference on VLSI Design and 22nd International Conference on Embedded Systems (VLSID'2023)**.
March 2017	**Graduate Aptitude Test Examination (GATE)**, Qualified and cleared interview at Indian Institute of Technology (IIT) Mandi for admission in Ph.D program.
March 2014	**Graduate Aptitude Test Examination (GATE)**, Qualified and got addmission at Deen Bandhu ChhottuRam University of Science and Technology (DCRUST) Murthal in M.Tech program.
January 2013	Awarded as **Organizer** in ECE and EN forum : "Gentronix" at InderPrastha Engineering College (IPEC) affilated by UPTU.
January 2012	Awarded as **Promoter Team Leader** in ECE and EN forum:"Gentronix" at Inderprastha Engineering College (IPEC) affilated by UPTU.

Outreach and Volunteering

November 2018	International Workshop on Nano/Micro 2D-3D Fabrication, Manufacturing of Electronic-Biomedical Devices and Applications organized by **Centre for Design & Fabrication of Electronics Devices(C4DFED)** at Indian Institute of Technology (IIT) Mandi.
April 2012	Workshop on Cyborg-The Robotics Workshop conducted by **Kyrion Robotics Club (IIT Kharagpur)** at InderPrastha Engineering College (IPEC).

References

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