Md. Najrul Islam

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Personal Information

DOB : Dec 11, 1993
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EDUCATION

Pursuing PhD Programme in the School of Computing and Electrical Engineering at IIT Mandi. , (Feb. 2019 - June 2024 [Expected])
Thesis advisors:: Dr. Rahul Shrestha (Guide), and Dr. Shubhajit Roy Chowdhury (Co-Guide).
Research Interests: Area and Energy Efficient VLSI Architecture of Deep-Neural-Network Hardware Accelerator for Edge Applications.

Masters degree in VLSI from National Institute of Technology, Meghalaya (2016-2018).
Thesis advisors: Dr. Anup Dandapat.
Thesis title: Design and Implementation of High Performance Low power SRAM array.
CGPA: 8.05/10

Bachelor degree in Electronics and Telecommunication Engineering from the Tripura Institute of Technology, Agartala, under Tripura University (2012-2016).
Thesis advisor: Dr. Bijoy Kumar Upadhyaya.
Thesis title: Prototype Design of Pulse Oxi-meter and Heart Rate Monitoring System
Result Percentage: 71%

Higher Secondary School from Radha Kishore Institutions, Kailashahar under Tripura Board of Secondary Education (2012). Result Percentage: 66.80%

Secondary School (Madhyamik) from Irani High school, Kailashahar under Tripura Board of Secondary Education (2010). Result Percentage: 66.85%

Job experiences

July 2018 → Jan. 2019: Worked as Project Assistant in Special Manpower Development Program for Chips to System Design (SMDP-C2SD) project at **National Institute of Technology, Meghalaya.**

Publications

Journal Paper

1. M. N. Islam, R. Shrestha and S. Roy Chowdhury, "An Uninterrupted Processing Technique-Based High-Throughput and Energy-Efficient Hardware Accelerator for Convolutional Neural Networks," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 12, pp. 1891-1901, Dec. 2022, doi: 10.1109/TVLSI.2022.3210963.

2. M. N. Islam, R. Shrestha and S. R. Chowdhury, "Energy-Efficient and High-Throughput CNN Inference Engine based on Memory-Sharing and Data-Reusing for Edge Applications," *(TCAS I, (Major revision))*.

3. F. Begum, S. Mishra, M. N. Islam and A. Dandapat, "A 10-bit 2.33 fJ/conv. SAR-ADC with high speed capacitive DAC switching using a novel effective asynchronous control circuitry," *Analog Integrated Circuits and Signal Processing*, vol. 100, no. 3, pp. 221-235, Apr. 2019, doi: 10.1007/s10470-019-01450-w.

4. F. Begum, S. Mishra, M. N. Islam and A. Dandapat, "Frequency Improvement of 10-bit SAR-ADC using TSPC based Control Circuitry," *IEEE VLSI Circuits & Systems Letter (VCAL)*, vol. 5, no. 1, pp. 1-8, May. 2019.

Conference Paper

1. M. N. Islam, R. Shrestha and S. R. Chowdhury, "A New Hardware-Efficient VLSI-Architecture of GoogLeNet CNN-Model Based Hardware Accelerator for Edge Computing Applications," *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Nicosia, Cyprus, 2022, pp. 414-417, doi: 10.1109/ISVLSI54635.2022.00093.

2. M. N. Islam, R. Shrestha and S. R. Chowdhury, "Low-Complexity Classification Technique and Hardware-Efficient Classify-Unit Architecture for CNN Accelerator," *(Presented in 'The 37th International Conference on VLSI Design & the 23rd International Conference on Embedded Systems (VLSID 2024)', to be held at Kolkata, India, during January 6-10, 2024)*.

3. F. Begum, M. N. Islam, K. A. Ahmed, and K. K. Sharma, "A Compact 3 GHz Comparator for SAR-ADCs In Robotic Prosthetic Hand Designs.", *10th International Conference on Microelectronics*, Circuits and Systems, Guwahati, India, 2023.

4. F. Begum, S. Mishra, M. N. Islam and A. Dandapat, "Analysis and Proposal of a Flash Subranging ADC Architecture." *3rd International Conference on Microelectronics*, Computing and Communication Systems, pp. 283-290. March, 2018.

Book Chapters

1. F. Begum, S. Mishra, M. N. Islam and A. Dandapat, "Analysis and Proposal of a Flash Subranging ADC Architecture," *Lecture Notes in Electrical Engineering*, vol. 556, no. 3, pp. 283-290, May. 2019, doi: 10.1007/978-981-13-7091-5-26.

Workshops, short term courses, conducted:

1. "Six days Short Term Course on Analog and Digital VLSI Design using Cadence Tools", Gauhati University, July-2023.
   Role: Resource Person.

2. "Twenty five days Short Term Course on Embedded Systems", IIT Mandi, Dec.-2022.
   Role: Visiting Teaching Assistant.

COMPUTER SKILLS

Languages:
Verilog, VHDL, C, C++, Python, Matlab, LaTeX.

VLSI front end tools:
Xilinx Vivado, Xilinx SDK, Xilinx ISE, Modelsim, Cadence Genus, Cadence nclaunch, Synopsys Design Vision/Compiler, Synopsys VCS

VLSI back end tools:
Cadence Innovus, Cadence IC Tools , Synopsis PT. Synopsys NT.

Other tools:
Matlab, Origin, Microsoft Visio, Inkscape.

Operating Systems:
Linux (CentOS, Red Hat, Ubuntu), Windows, Android.

Languages known :

Speak: English, Bengali, Hindi/Urdu.
Understand: English, Bengali, Hindi, Assamese, Odia.
Read: English, Bengali, Hindi, Arabic, Assamese.

Hobbies   I love reading stories, news, health-fitness, and science-tech updates. Fond of exploring nature through treks and rides, i.e.**Traveling**, catching beautiful moments with lens, i.e. **Photography**.

Habits: Wake up early, and run 10–12 KMs every morning.

References
- Dr. Rahul Shrestha, Associate Professor,
  School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Himachal Pradesh - 175075, India
  ✉^{o}: rahul_shrestha@iitmandi.ac.in

- Dr. Shubhajit Roy Chowdhury, Associate Professor,
  School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Himachal Pradesh - 175075, India
  ✉^{o}: src@iitmandi.ac.in

- Dr. Hitesh Shrimali, Associate Professor,
  School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, Himachal Pradesh - 175075, India
  ✉^{o}: hitesh@iitmandi.ac.in

- Dr. Anup Dandapat, Associate Professor,
  Department of Elcectronics and Communication Engineering,
  National Institute of Technology Meghalaya,
  Meghalaya - 793001, India
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  ✉^{o}: anup.dandapat@nitm.ac.in