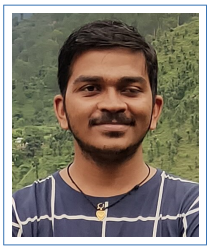
Rohit Chaurasiya

Curriculum Vitae

School of Computing and Electrical Engineering
Indian Institute of Technology Mandi
(+91) 7972019296
rohitchaurasiyaiitmandi@gmail.com
My Webpage
Google Scholar



Education

August 2017–Present: **Ph.D. Thesis Submitted on 08^{th} April 2022**, *School of Computing and Electrical Engineering*, **Indian Institute of Technology (IIT) Mandi**.

2012–2014 : **Master of Engineering, Electronics Engineering**, *University of Mumbai*, Ramrao Adik Institute of Technology, Navi Mumbai (*Presently:* Dr. D. Y. Patil, Deemed To Be University, Ramrao Adik Institute of Technology, Navi Mumbai).

CGPA : 8.92/10

2008–2012 : **Bachelor of Engineering, Electronics Engineering**, *University of Mumbai*, Ramrao Adik Institute of Technology, Navi Mumbai (*Presently:* Dr. D. Y. Patil, Deemed To Be University, Ramrao Adik Institute of Technology, Navi Mumbai).

Percentage : 74.73 %

2007 : **Higher Secondary Examination**, *Bhiwandi Nizampur Nagarpalika College*, Bhiwandi, Dist-Thane, Maharashtra, .

Percentage : 78.332 %

2006 : **Secondary School Certificate**, *Dr. Omprakash Agarwal English High School,*, Bhiwandi, Dist-Thane, Maharashtra.

Percentage : 73.47 %

Work Experience

January,2018 – June, 2018: ***Project Trainee***, *Research and Technology Center India (RTC-IN)*, **Robert Bosch Engineering and Business Solutions Private Limited**, Bengaluru.

Worked on project titled **Parameterized Posit Arithmetic Hardware Generator** under the supervision of Dr. Rahul Shrestha (Asst. Prof. IIT Mandi), Dr. Jonathhan Neudorfer (Senior Researcher at Robert Bosch Engineering and Business Solutions Private Limited) & Dr. Farhad Merchant (Post Doctoral Researcher RWTH Aachen University, Germany) .

January,2015 – August,2017: ***Assitant Professor***, *Electronics Department, Ramrao Adik Institute of Technology, Nerul, Navi Mumbai*,

• Conducted **Lecture Sessions & Laboratory sessions of Basic VLSI Design & Microprocessor and Peripherals course** for Undergraduate Students..

August,2012 – December,2014: ***Lecturer***, *Electronics Department, Ramrao Adik Institute of Technology, Nerul, Navi Mumbai*,

• Conducted **Lecture Sessions of Electronic Devices and Microcontroller and Applications course** for Undergraduate Students.

• Conducted Laboratory sessions of **Electronic Devices, Microcontroller and Applications, Basic Electrical and Electronics Engg, Electronics Devices & Digital Circuit Design** for Undergraduate Students. .

Teaching Assistant-ship

August,2018 – April,2022 ***Teaching Assistant***, *School of Computing and Electrical Engineering, Indian Institute of Technology, Mandi*,

• Worked as Teaching Assistant in **Laboratory sessions of CMOS Analog IC Design Lab, Digital Electronics Lab & Digital Design IC Practicum Lab** for M.Tech & B.Tech Students.

• Worked as Teaching Assistant in **Lecture sessions of Digital VLSI Architecture & Digital MOS LSI Circuits** for M.Tech & B.Tech Students.

• Worked as Teaching Assistant in **Lecture sessions of IC Course and Applied Electronics Lab for B.Tech Students and conducted doubt solving session and tutorial sessions** for same.

August,2017 – December,2017 ***Teaching Assistant***, *School of Computing and Electrical Engineering, Indian Institute of Technology, Mandi*,

• Worked as Teaching Assistant in **Lecture sessions of Matrix Theory** for M.Tech Students..

Research Interests

Areas

- VLSI-Algorithm Design for Spectrum Sensing in Cognitive Radio Network.
- Digital VLSI-Architecture Design of Standalone and Cooperative Spectrum Sensors for Cognitive Radio Network.
- Application-Specific Integrated Circuit (ASIC) Chip Design, Implementation, Testing and Field-Programmable Gate Array (FPGA) prototyping for digital processing tasks in Wireless Communication System, Power Electronics, Computer Arithmetic and Fractional-order chaotic system domains.
- Testing of Spectrum Sensing feature in Cognitive Radio Network by developing a test-bed based on practical communication scenario using universal software radio peripheral (USRP) platform & LabVIEW environment.

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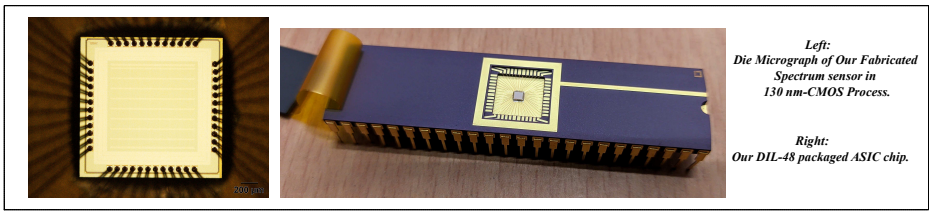
PhD Topic **Hardware Efficient VLSI-Algorithms and Digital-Architectures of Standalone and Cooperative Spectrum Sensors for Cognitive Radio Network**.

Supervisor **Dr. Rahul Shrestha**, *Assistant Professor, School of Computing & Electrical Engineering, IIT Mandi*, (*Personal Web-page*).

Ph.D. Work, ASIC Chip Tapeout, Testing and FPGA Prototyping



In our research work, we addressed the problem of reliable licensed user detection, hardware inefficiency and long sensing time of spectrum sensors. We developed hardware-friendly VLSI spectrum sensing algorithms and proposed hardware-efficient digital architectures for stand-alone spectrum sensors (SSSRs) and cooperative spectrum sensors (CSRs). These spectrum sensors were FPGA prototyped (Click here for details) and ASIC-Chip designed in 90 & 130 nm-CMOS process. Four CSRs were fabricated on a single silicon die in 130 nm-CMOS process and its die micrograph is shown in above figure. The fabricated ASIC-Chip was tested in practical scenario of cooperative cognitive radio network (Click here for details) & measurement results were obtained. The proposed SSSRs and CSRs delivered reliable detection in negative Signal-to-Noise Ratio regime with short sensing time and higher hardware efficiency that is suitable for portable cognitive radio devices.

Publications

Citations on Google Scholar: 177

Peer Reviewed Journal Publications

2022 **Rohit B. Chaurasiya and** Rahul Shrestha, "Design and ASIC-Implementation of Hardware-Efficient Cooperative Spectrum-Sensor for Data Fusion Based Cognitive Radio Network," ***IEEE Transactions on Consumer Electronics***, DOI: 10.1109/TCE.2022.3167471, Early Access, April-2022, Click to Access Paper.

2022 **Rohit B. Chaurasiya and** Rahul Shrestha, "Hardware-Efficient VLSI-Architecture and ASICImplementation of GRCR based Cooperative Spectrum Sensor for Cognitive-Radio Network," ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***, Volume: 30, Issue: 2, pp. 166-176, February-2022, Click to Access Paper.

2021 **Rohit B. Chaurasiya and** Rahul Shrestha, "Area-Efficient and Scalable Data-Fusion based Cooperative Spectrum Sensor for Cognitive Radio," ***IEEE Transactions on Circuits and Systems II: Express Briefs***, Volume: 68, Issue: 4, pp. 1198-1202, April-2021, Click to Access Paper.

2021 **Rohit B. Chaurasiya and** Rahul Shrestha, "A New Hardware-Efficient Spectrum-Sensor VLSI-Architecture for Data Fusion based Cooperative Cognitive-Radio Network," ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***, Volume: 29, Issue: 4, pp. 760-773, February-2021, Click to Access Paper.

2020 **Rohit B. Chaurasiya and** Rahul Shrestha, "Fast Sensing-Time and Hardware-Efficient Eigenvalue based Blind Spectrum Sensors for Cognitive Radio Network," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, Volume: 67, Issue: 4, pp. 1296-1308, April-2020, Click to Access Paper.

2019 **Rohit B. Chaurasiya and** Rahul Shrestha, "Hardware-Efficient and Fast Sensing-Time Maximum-Minimum-Eigenvalue based Spectrum Sensor for Cognitive Radio Network," ***IEEE Transactions on Circuits and Systems I: Regular Papers***, Volume: 66, Issue: 11, pp. 4448-4461, November-2019, Click to Access Paper.

2017 Divya K. Shah**, Rohit B. Chaurasiya,** Vishwesh A. Vyawahare**,** Khushboo Pichhode**,** Mukesh D. Patil, "FPGA implementation of fractional-order chaotic systems," ***AEU - International Journal of Electronics and Communications***, Volume: 78, pp. 245-257, August-2017, Click to Access Paper.

Conference Publications

2021 **Rohit B. Chaurasiya and** Rahul Shrestha, "Hardware-Efficient ASIC Implementation of Eigenvalue Based Spectrum Sensor Reconfigurable-Architecture for Cooperative Cognitive-Radio Network," ***IEEE International Symposium on Circuits and Systems (ISCAS)***, pp. 1-5, May-2021, South Korea (Daegu). Click to Access Paper.

2019 **Rohit B. Chaurasiya and** Rahul Shrestha, "Hardware-Efficient and Low Sensing-Time VLSI-Architecture of MED based Spectrum Sensor for Cognitive Radio," ***IEEE International Symposium on Circuits and Systems (ISCAS)***, pp. 1-5, May-2019, Japan (Sapporo). Click to Access Paper.

2018 **Rohit Chaurasiya,** John Gustafson**,** Rahul Shrestha**,** Jonathan Neudorfer**,** Sangeeth Nambiar**,** Kaustav Niyogi**,** Farhad Merchant**,** Rainer Leupers, "Parameterized Posit Arithmetic Hardware Generator," $\mathbf{36^{th}}$ ***IEEE International Conference on Computer Design (ICCD)***, pp. 334-341, October-2018, USA (Orlando, Florida). Click to Access Paper.

2015 Khushboo Pichhode**,** M. D. Patil**,** Divya Shah and **Chaurasiya Rohit B**, "FPGA implementation of efficient vedic multiplier," ***IEEE International Conference on Information Processing (ICIP)***, pp. 565-570, December-2015, India (Pune). Click to Access Paper.

2015 Divya Shah, **Chaurasiya Rohit B,** Devdip Sen and Shaswat Goyal , "Vehicle parking system implementation using CPLD," ***IEEE International Conference on Communication, Information & Computing Technology (ICCICT)***, pp. 1-5, January-2015, India (Mumbai). Click to Access Paper.

2014 **Chaurasiya Rohit B.,**M. D. Patil,Divya Shah and Abhijit Kadam , "FPGA implementation of SVPWM control technique for three phase induction motor drive using fixed point realization," ***IEEE International Conference on Circuits, Systems, Communication and Information Technology Applications (CSCITA)***, pp. 93-98, April-2014, India (Mumbai). Click to Access Paper.

Patents Filed:

21stFeb 2018: **IoT based Cortic Pad for sleep analysis**, Inventors: Mr. Rohan Stanley, Dr. Ramesh Vasappanavara, Ms. Ananya Iyer, **Mr. Rohit Chaurasiya**, Ms. Divya Shah, ***Application Number: 201821006596, Date of Filing: 21/02/2018***

1stMay 2018: **FPGA based Hardware System for implementation of Complex-order Dynamical System**, Inventors: Divya Shah, Mukesh D. Patil, Vishwesh A. Vyawahare, **Rohit Chaurasiya** and Khushboo Pichode, ***Application Number: 2018210000547, Date of Filing: 01/05/2018***

Fellowships & Awards

2019 ***ISCAS-2019 Student Travel Grant***, Awarded with ISCAS-2019 Student Travel Grant to attend IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, May 26-29, 2019.

2019 ***VLSID-2019 Fellowship*** , Awarded with IEEE VLSID-2019 fellowship to attend tutorials and main conference at 32^{nd} IEEE International Conference on VLSI Design and 18^{th} International Conference on Embedded systems, New Delhi, India, Jan 5-9, 2019.

2016 ***Project Grant***, Received Grant of Rs. 40,000/- from University of Mumbai for Project entitled FPGA Implementation of Fractional order operator.

2016 ***Contribution to R & D***, Awarded for contributing to Research and Development work at Ramrao Adik Institute of Technology, for the academic year (2013-2014), (2014-2015) and (2015-2016).

Conferences & Workshops

2021 ***Conference Attended:*** IEEE International Symposium on Circuits and Systems **(ISCAS)**, Daegu, Korea (On-site) & Virtual Platform, May 23-26, 2021. (Attented on Virtual Platform.)

2019 ***Conference Attended:*** IEEE International Symposium on Circuits and Systems **(ISCAS)**, Sapporo, Japan, May 26-29, 2019.

2019 ***Conference Attended:*** 32^{nd} IEEE International Conference on VLSI Design **(VLSID)** and 18^{th} International Conference on Embedded systems, New Delhi, India, Jan 5-9, 2019.

2014 ***Conference Attended:*** IEEE International Conference on Circuits, Systems, Communication and Information Technology Applications **(CSCITA)**, Mumbai, India, 2014,

2018 ***Workshop Attended:*** Short course on A hands-on Introduction to Modern Wireless Systems: Theory and Simulation, **IIT Kanpur**, Dec. 3-6, 2018.

2017 ***Workshop Attended:*** Cadence Design Flow: Analog and Digital Circuit Design organized by organized by **Entuple technologies**, **IIT Mandi**.

2018 ***Workshop Attended:*** International workshop on Nano Micro 2D & 3D fabrication and manufacturing of Electronic & Biomedical Devices and Applications **(IWNEBD-2018)**, **IIT Mandi**.

2017 ***Workshop Attended:*** BMBF TU9-IIT Mandi workshop on Currents Trends in Analog Circuit Designing, **IIT Mandi**, Sept. 25-26, 2017.

2017 ***Workshop Attended:*** Power Electronics Application to Renewable Energy Conversion Organized by **TEQIP-II**, VJTI in collaboration with Quality Improvement Continuing Education Program, **IIT Bombay**, Feb 17-22, 2017.

2016 ***Workshop Attended:*** Fractional Calculus Engineering Laboratory organized by EE Department, **VNIT,Nagpur**, Nov. 15-19, 2016.

2016 ***Workshop Attended:*** Two day workshop on SCILAB and Arduino Interfacing organized at **IIT Bombay**.

2016 ***Workshop Attended:*** 102nd Indian Science Congress held at **University of Mumbai**, Mumbai.

2016 ***Workshop Attended:*** Three day workshop on Virtual Instrumentation using LABVIEW At Wadhwani electrical lab, **IIT Bombay**.

2016 ***Workshop Attended:*** Three day workshop on Embedded System Design on MSP430 conducted by **TEXAS Instruments**.

2016 ***Workshop Attended:*** Workshop and field trial on SIMULATION AND CONTROL OF MAGNETIC LEVITATION SYSTEM sponsored by MHRD & conducted at RAIT, Navi Mumbai.

2016 ***Workshop Attended:***1 Week Embedded System Training Program at **Thinkslab SINE IIT Bombay.**

2015 ***Workshop Attended:*** Faculty Development Program on Control Engineering Analysis & Design with MATLAB/ Simulink organized by Department of Avionics at **Indian Institute of Space Science and Technology (IIST), Kerala.**, 15-18 December 2015.

2015 ***Workshop Attended:*** Two Week Faculty Development Program on Electronic System Design: From Devices to Applications approved by AICTE at Electronics Engg. **Sardar Patel Institute of Technology, Andheri, Mumbai.**, 4-15 May 2015.

2015 ***Workshop Attended:*** Five Day Certified Course on Rapid Embedded Systems using ARM mbed organized by Department of Electronics Engg. **Ramrao Adik Institute of Technology, Navi Mumbai.**, 7-11 Oct 2015.

2015 ***Workshop Conducted:*** Worked as a resource person in the workshop on Digital Circuit Implementation using CPLD and FPGA organized by Department of Electronics Engg. **Ramrao Adik Institute of Technology, Navi Mumbai.**, 7-8 Aug 2015.

2014 ***Workshop Conducted:*** Worked as a resource person in the workshop on Modern Digital Design organized by Department of Electronics Engg. **Ramrao Adik Institute of Technology, Navi Mumbai.**, 8-9 Aug 2014.

Membership of Professional Bodies

Membership: **Graduate Student Member**, Institute of Electrical and Electronics Engineers (IEEE).

Technical skills

VLSI Design Tools **Design Compiler and Genus** for RTL Synthesis, **VCS and NCLaunch** for Functional Verification, **Innovus** for Physical Design flow, **Virtuoso schematic editor**, **Vivado (2018.2)** for FPGA Based System Design, **Symica, Magic VLSI Layout, Qflow.**

Hardware Description Languages: VHDL, Verilog
System Simulation Tool : MATLAB.
Documentation Tool: Latex.

Personal Details and Interest

Date of Birth 06^{th} March 1991

Nationality Indian

Martial Status Single

Hobbies I love **Reading Books**. A comprehensive list of my read books, Insights and beauty from them can be accessed here. I also have interests in **Writing, Travelling, Art, Philosophy, Music and Poetry.**

Referees

Dr. Rahul Shrestha
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Indian Institute Technology (IIT) Mandi
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✉ rahul_shrestha@iitmandi.ac.in