2016 IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), 16-19 October 2016, Abu Dhabi, UAE

The Pole-zero Doublet: a Cascode Operational Amplifier with Cross Coupled Capacitor

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***Abstract*—A symbolic analysis is presented to investigate the effect of cross coupled capacitor on a cascode operational amplifier. A complete transfer function of the amplifier with cross coupled capacitor is derived and verified through circuit simulations. The modeled transfer function shows presence of a pole-zero doublet in the amplifier's frequency response when the cross-coupled capacitor is connected across it. The analysis further results in a closed form equations to optimize the amplifier based on user defined specifications such as, an open loop dc gain, a unity gain bandwidth and a phase margin. To check the validity of the model, a 50 dB open loop dc gain and 255 MHz unity gain bandwidth cascode amplifier is designed in a standard 90 nm CMOS technology with the supply voltage of 1.5 V. The results obtained from simulation and modeled transfer function show good agreement with each other and have an acceptable average relative error of 3 %.**

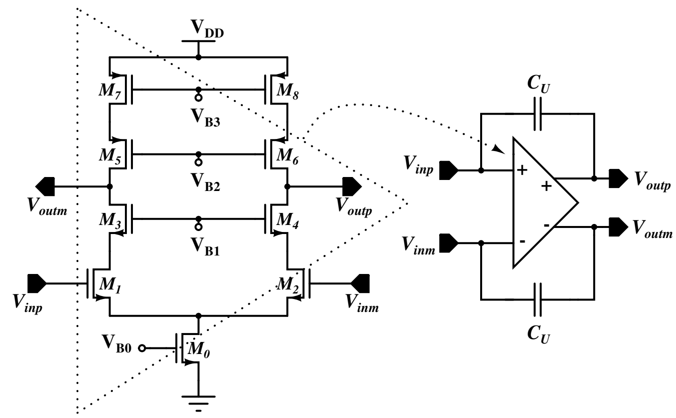

Fig. 1. Fully differential telescopic op-amp with cross coupled capacitor C_U.

I. Introduction

A cascode operational amplifier (op-amp) achieves high voltage gain by increasing the output impedance of the amplifier [1], [2]. The cascode op-amp also provides better bandwidth because of single stage architecture and less parasitic capacitance in the signal path [3], [4]. However, the fully differential telescopic op-amp has limited gain and a rigorous effort to increase the gain results in reduced unity gain bandwidth (UGBW). This happens because the parasitic pole becomes more dominant; causing gain to fall quickly at high frequencies [3], [5]. Depending on exact location, the non dominant pole may have significant effect on high speed high gain amplifier; leading to either larger settling time or higher power dissipation.

An analytical approach to study the cascode amplifier and current mirror can be found in [6], [7], [8]. Frequency behavior of cascode load and its effect on settling response of the amplifier is given by [4]. In this paper, the effect of cross coupled capacitor on a single stage multi-pole cascode amplifier (Fig. 1) is investigated using analytical techniques and computer simulations. The detailed analysis presented in this article is useful to design high speed high gain op-amps for the application of analog to digital converter (ADC), reported in [9].

The paper is organized as follows. The transfer function for the op-amp with cross coupled capacitor (C_U) is derived in Section II. A closed form of equation for C_U is derived in Section III to optimize the value of cross coupled capacitor, based on the desired open loop dc gain, UGBW and phase margin specifications. Finally, to validate the effectiveness of the model, a comparison between results obtained from circuit simulation and derived transfer function is presented in Section IV, followed by conclusions in Section V.

II. Modeling the op-amp

Two case studies are presented to understand the effect of cross coupled capacitor on fully differential telescopic op-amp. In the first case, the cascode load's frequency behavior in presence of C_U is explained considering an ideal transconductance stage, while in the second, the cascode load is assumed to be frequency independent.

Case 1: Frequency Behavior of the Cascode Load

The equivalent ac half circuit in Fig. 2(a) is used to analyze the effect of C_U on frequency response of the cascode load. The effect of parasitic capacitance at node Q of the circuit in Fig. 2(a) on cascode amplifier's settling response is studied in [4]. Since the effect of cross coupled capacitor on the output and node Q is unknown, this case study of cascode load becomes necessary from the design prospective.

A technique to model the positive feedback capacitor (C_U) is presented in Fig. 2(a). For a differential circuit operation, the input ac signals are 180° phase shifted with respect to each other. Hence, capacitor C_U is synthesized in the ac half circuit model by connecting it between nodes v_{outm} and $-v_{inp}$.

The small signal model used to analyze the effect of C_U on cascode load is shown in Fig. 2(b). For the assumption of an

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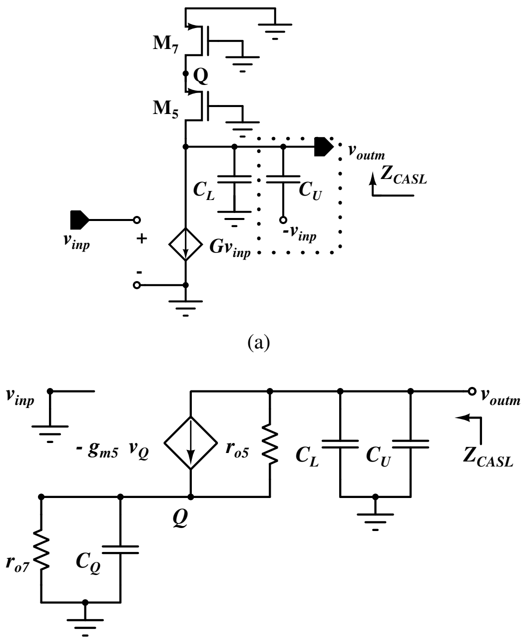
$$G(s) = \frac{-R_D\ ro_3\ ro_1 C_U(C_P + C_{GD1})s^2 - [R_D R_{CAS}(C_U - C_{GD1}) + R_D(ro_3 + ro_1)C_U]s - gm_1 R_D R_{CAS}}{R_D\ ro_3\ ro_1(C_U + C_L)(C_P + C_{GD1})s^2 + [R_D R_{CAS}(C_U + C_L) + R_D\ ro_1(C_P + C_{GD1})]s + R_{CAS} + R_D} \quad (5)$$



(a)

(b)

Fig. 2. (a) The equivalent ac half circuit of op-amp with cascode load and an ideal input transconductance stage, (b) the small signal model of Fig. 2(a) to calculate the output impedance of the load.

ideal input transconductance stage, C_U appears in parallel with the load capacitance at the output. The small signal impedance Z_{CASL} is obtained as,

$$Z_{CASL}(s) = \frac{(1 + R_Q \cdot C_Q \cdot s)}{a \cdot s^2 + b \cdot s + 1} \quad (1)$$

$$a = R_{CASL} R_Q \cdot (C_U + C_L) C_Q,$$

$$b = R_{CASL} \cdot (C_U + C_L) + ro_7 \cdot C_Q,$$

$$R_{CASL} = gm_5 ro_5 ro_7 + ro_5 + ro_7 \approx gm_5 ro_5 ro_7,$$

$$R_Q = \frac{1}{gm_5} || ro_5 || ro_7.$$

Equation (1) is a second order system because it is a parallel combination of frequency dependent cascode load and the capacitance at output node. From (1), the locations of the poles and zero are obtained as follows,

$$\omega_{p1'} = \frac{-1}{R_{CASL} \cdot (C_U + C_L)} \quad (2)$$

$$\omega_{p3} \approx -\left(\frac{1}{R_Q \cdot C_Q} + \frac{1}{ro_5 \cdot (C_U + C_L)}\right) \approx \frac{-1}{R_Q \cdot C_Q} \quad (3)$$

$$\omega_{z3} = \frac{-1}{R_Q \cdot C_Q} \quad (4)$$

While it is known that cascode load introduces a high frequency pole-zero pair in amplifier's frequency response [4], (3) and (4) show that the location of this pair is independent of C_U. The positive feedback only contributes to the output pole, and hence the exponential settling component, as far as the cascode load's frequency behavior is concerned. So it can be concluded that for modeling the op-amp with cross coupled capacitor, the cascode load shows frequency independent behavior since the effect of pole-zero pair is trivial at the moment.

Case 2: Op-amp with Frequency Independent Cascode Load

The PMOS cascode load of the amplifier in Fig. 1 is replaced by a resistive load, R_D. The equivalent ac small signal model used to analyze the positively closed loop op-amp is shown in Fig. 3. The transfer function of op-amp with cross coupled capacitor is therefore incurred by solving nodal equations for Fig. 3. The simplified transfer function is given by Equation (5).[1] $gm_{1,3}$ and $ro_{1,3}$ are the transconductance and small signal output resistance of transistors M_1 and M_3 respectively, C_{GD1} and C_L are the gate-drain capacitance of M_1 and the load capacitance respectively, $R_{CAS} = gm_3 ro_3 ro_1$ and $R_D \approx gm_5 ro_5 ro_7$. The parasitic capacitance associated with node P is determined as, $C_P = C_{GS3} + C_{SB3} + C_{DB1}$. Further, R_D and R_{CAS} being the impedance of cascode stage, while deriving (5) and subsequent poles and zeros it is assumed that $R_D \gg ro_5, ro_7$ and $R_{CAS} \gg ro_3, ro_1$.

From (5), it is observed that the three capacitors C_P, C_L and C_U, form a loop yielding a second order transfer function with two poles, ω_{p1} and ω_{p2}. For typical values of load, if we assume $C_L > C_P$ and therefore $|\omega_{p1}| < |\omega_{p2}|$, then the two poles are obtained at frequencies,

$$\omega_{p1} \approx \frac{-1}{R_{OUT} \cdot (C_U + C_L)} \quad (6)$$

[1] For an accurate annex, the back gate effect of transistor where bulk and source are not tied together must also be considered in the analysis. The body effect can be included in the equations by replacing gm with $(gm + gmb)$.

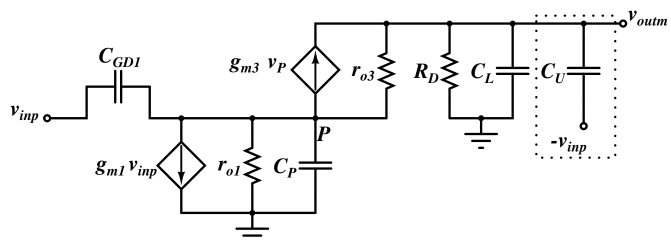


Fig. 3. Equivalent ac small signal model to derive the transfer function of the op-amp with cross coupled capacitor.

$$\omega_{p2} = \frac{-(gm_3 ro_1 + 1)}{ro_1 \cdot (C_p + C_{GD1})} \approx \frac{-gm_3}{(C_p + C_{GD1})} \tag{7}$$

where, $R_{OUT} = R_D || R_{CAS}$ is the output resistance of the amplifier.

Equation (5) suggests that the addition of C_U in the circuit gives a second order numerator. The nature and the locations of two zero frequencies depend on the parasitic capacitance at node P and values of gm_1 and gm_3. If the C_P is small then two real valued zeros are located at frequencies,

$$\omega_{z1} \approx \frac{-gm_1}{(C_U - C_{GD1})} \tag{8}$$

$$\omega_{z2} = \frac{-(gm_3 ro_3 + 1)}{ro_3 \cdot (C_p + C_{GD1})} \approx \frac{-gm_3}{(C_p + C_{GD1})} \tag{9}$$

where $|\omega_{z1}| < |\omega_{z2}|$. On the other hand, if the C_P is high and gm_1 is comparable to gm_3, a complex conjugate pair of zeros is obtained at the location,

$$\omega_{z1,2} \approx x \pm j\ y \tag{10}$$

$$x = \frac{-gm_3}{2\ (C_P + C_{GD1})},$$

$$y = \frac{1}{2\ (C_P + C_{GD1})} \sqrt{gm_3 \left(gm_3 - \frac{4\ gm_1 (C_P + C_{GD1})}{C_U} \right)}.$$

An interesting fact can be observed is that, although the cross coupled capacitor does not affect the non dominant pole, it creates a pole-zero doublet in the positively closed loop system. Location of the doublet is given by (7) and (9). This doublet is not present in the op-amp without cross coupled capacitor.

III. Analysis and Formulation

Equation (6) reveals that, because of additional capacitance C_U, ω_{p1} has shifted towards the origin. Since dc gain remains constant and the dominant pole moves inside, the positively close loop system has relatively small UGBW compared to its open loop similitude. Note that the transfer function of op-amp without cross coupled capacitor can be obtained by putting C_U=0 in (5) and hence proves the significance of symbolic analysis. For practical assumption of $C_U > C_{GD1}$, the RHP zero of open loop system moves to the left half plane (LHP) of complex plane. Location of this zero is given by (8). This zero starts to provide additional phase a decade before its actual occurrence and hence improves the phase margin. Phase margin (PM) of the op-amp is given as,

$$PM = 180^\circ + \arctan\left(\frac{\omega_u}{\omega_{z1}}\right) - \arctan\left(\frac{\omega_u}{\omega_{p1}}\right) \tag{11}$$

where, $\omega_u \approx gm_1/(C_U + C_L)$ is the modified UGBW of the amplifier. For $C_U = nC_L$, error in UGBW of the op-amp with and without cross coupled capacitor (ω'_u) is given as, $-n\omega'_u/(n+1)$. Substituting the values of ω_{p1} and ω_{z1} from (6) and (8), we have,

$$\tan(PM - 180^\circ) = \frac{C_U - A_{dc}(C_U + C_L)}{(C_U + C_L) + A_{dc} C_U} \tag{12}$$

where, $A_{dc} \approx gm_1 R_{OUT}$ is the dc gain. If $A_{dc} C_U > C_L$ is assumed then rearranging terms yields,

$$C_U = \frac{-C_L}{\tan(PM - 180^\circ) + 1} \tag{13}$$

For the complex conjugate pair of zeros, the numerator of (5) can be written as,

$$\alpha \cdot s^2 + \beta \cdot s + \gamma$$

$$\alpha = -R_D\ ro_3\ ro_1 \cdot C_U (C_P + C_{GD1}),$$

$$\beta \approx -R_D R_{CAS} \cdot (C_U - C_{GD1}), \quad \gamma = -gm_1 R_D R_{CAS}.$$

The closed form of equation relating the C_U to the phase margin of system under consideration in this case is given by,

$$\frac{\beta \cdot \omega_u}{\gamma - \alpha \cdot \omega_u^2} = \tan\left[PM - 90^\circ + \arctan\left(\frac{\omega_u}{\omega_{p2}}\right)\right] \tag{14}$$

Equations (13) and (14) can therefore be used to achieve required phase margin specification without altering the other design parameters such as dc open loop gain and power consumption. Change in phase margin of the op-amp with and without C_U is now given as,

$$\tan^{-1}\left[\frac{(n+1)\beta \cdot \omega'_u}{(n+1)^2 \gamma - \alpha \cdot \omega'^2_u}\right] + \tan^{-1}\left[\frac{n \cdot \omega_{p2} \cdot \omega'_u}{(n+1)\omega_{p2}^2 + \omega'^2_u}\right].$$

The step response of the amplifier depends on the location of negatively closed loop poles and zeros. When the system represented by (5) is placed in a negative feedback, the negatively closed loop transfer function is of the form

$$G_{CLN}(s) = \frac{-A_{dc}}{1 + A_{dc} \cdot H} \cdot \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \cdot \left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{pc1}}\right) \cdot \left(1 + \frac{s}{\omega_{pc2}}\right)} \tag{15}$$

where ω_{pc1} and ω_{pc2} are the closed loop poles and H is the feedback factor. For the system with cross coupled capacitor the step response is therefore given by,

$$v_o(t) = \frac{-A_{dc}}{1 + A_{dc} \cdot H} \left[1 - A\ e^{\frac{-t}{\tau_3}} + B\ e^{\frac{-t}{\tau_4}}\right]$$

$$A = \frac{\tau_1\ \tau_2 - \tau_1\ \tau_3 - \tau_2\ \tau_3 + \tau_3^2}{\tau_3(\tau_3 - \tau_4)},$$

$$B = \frac{\tau_1\ \tau_2 - \tau_1\ \tau_4 - \tau_2\ \tau_4 + \tau_4^2}{\tau_4(\tau_3 - \tau_4)},$$

$$\tau_1 = \frac{1}{\omega_{z1}}, \quad \tau_2 = \frac{1}{\omega_{z2}}, \quad \tau_3 = \frac{1}{\omega_{pc1}}, \quad \tau_4 = \frac{1}{\omega_{pc2}}.$$

Hence (15) shows an over damped system response. The zeros created by the positive feedback adds a slow settling component into the negatively closed loop system.

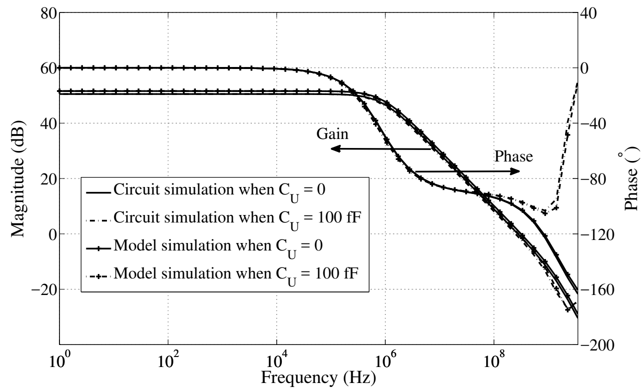


Fig. 4. Magnitude and phase response of the designed amplifier for $gm_1 = 2.5\ mS$, $gm_3 = 2.6\ mS$, $gm_5 = 1.4\ mS$, $gm_7 = 1.5\ mS$, $R_{CAS} \approx 216\ k\Omega$, $R_D \approx 781\ k\Omega$, $C_L = 1\ pF$ and $C_U = 100\ fF$.

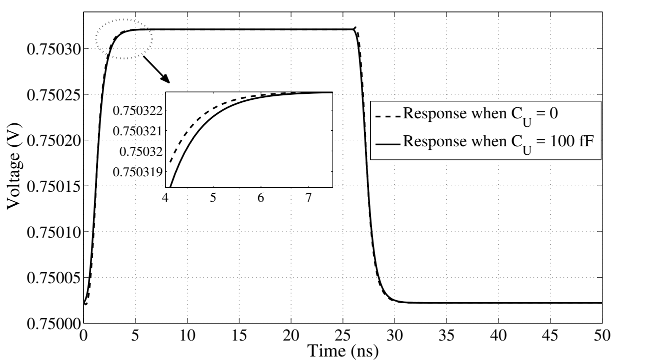


Fig. 5. Step response of the amplifier with the parameters of Fig. 4.

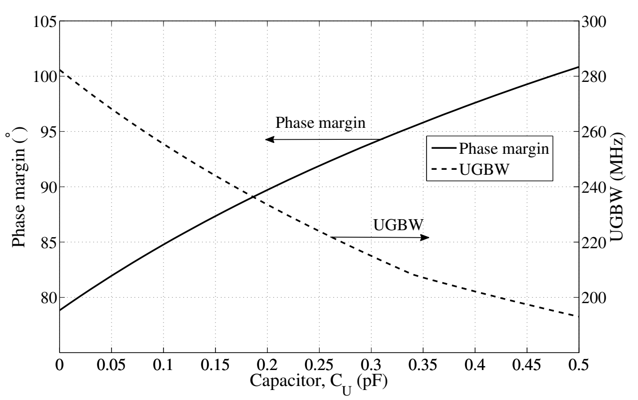


Fig. 6. PM and UGBW of the amplifier for different values of C_U.

IV. Validation and Simulation Results

The op-amp of Fig. 1 is implemented in a standard 90 nm CMOS technology with the supply voltage of 1.5 V. The modeled equation given by (5) is implemented in MATLAB. Fig. 4 compares the magnitude and phase response of the modeled op-amp with the circuit simulation. From the figure, it is evident that both the results are in close agreement with each other. As shown in Table I, the locations of poles and zeros obtained from model are found matched with the pole-zero simulation result with an average relative error of 3 %. The effect of LHP zeros created by positive feedback can be observed from the phase plot. Fig. 5 shows the transient behavior of the amplifier when it is connected in unity gain configuration. The effect of cross coupled capacitor is visible from the inset shown in the figure. As predicted from the above analysis, Fig. 6 shows the improvement in phase margin of the positively closed loop op-amp. However, the UGBW decreases proving trade-off between the two.

TABLE I
The locations of poles and zeros for $C_U = 100fF$.

	Circuit Simulation (Hz)	Model Simulation (Hz)
ω_{p1}	-7.64×10^5	-7.73×10^5
ω_{p2}	-1.42×10^9	-1.47×10^9
$\omega_{z1,2}$	$-(6.48 \pm j\ 19.4)10^8$	$-(6.27 \pm j\ 20.9) \times 10^8$

V. Conclusion

The complete analysis of amplifier with the cross coupled capacitor is presented. It is shown that cross coupled capacitor introduces a pole-zero doublet into the op-amp's frequency response. The results obtained from circuit simulation and symbolic analysis match with each other. The results show improvement in phase margin of the amplifier at the cost of UGBW. This paper modeled a closed form of equation for the cross coupled capacitor to optimize the UGBW and phase margin specifications. The analysis presented in this article can further be useful to design a high-speed high-resolution data converters, where stringent settling accuracies are required.

Acknowledgment

The authors would like to thank DeitY, Govt. of India for supporting the work through SMDP-C2SD project.

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