A Steep Slope MBE-Grown Thin p-Ge Channel FETs on Bulk $Ge_{-on-}Si$ Using HZO Internal Voltage Amplification

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***Abstract*—There are vital challenges to harness the unique assets of germanium (Ge) because of Ge-on-insulator (GeOI) processing issues. The advances in molecular beam epitaxy (MBE) technology have enabled the defect-free growth of atomic-level Ge stacks over the standard monolithic silicon platform to leverage the properties of the Ge as a channel layer. Here, we present the first ever report on the authoritative integration of ferroelectric (FE) hafnium zirconium oxide (HZO) over the $p-Ge/n-Ge_{-on-}n-Si$ system. A rudimentary approach for the carrier modulation in the channel was employed using depletion approximation and negative capacitance (NC) to fabricate HZO and thin p-Ge channel-based FET. The TaN/HZO/TaN stacks were optimized and characterized for enhanced ferroelectricity and non-centrosymmetric orthorhombic phase, which is further confirmed with piezoresponse force microscopic (PFM) analysis. The trivial loop hysteresis conditions to validate the NCFET operation was discussed. The devices demonstrated a lower subthreshold swing (SS) of ∼23.44 mV/dec and I_{ON}/I_{OFF} ratio of 10^5. The threshold voltage shift $V_t = -0.6$ and -1.1 V with the body bias voltage of 0.25 and 0.5 V, respectively. Minimum DIBL measured ∼26 mV/V, and rule-out gate induces drain lowering (GIDL) effect due to no gate–drain region overlap.**

***Index Terms*—Depletion approximation, depletion FET, germanium, hafnium zirconium oxide (HZO), molecular beam epitaxy (MBE), negative capacitance (NC), NC FET, piezoresponse force microscopy (PFM).**

I. INTRODUCTION

THE quest for energy-efficient logic and switching devices is the need of the hour. Currently, leading contenders fin field-effect transistor (FinFET) and ultra-thin-body silicon-on-insulator (UTB-SOI) are trending in the current generation technology node due to their low power consumption and excellent suppression of short-channel effects (SCEs) [1]. However, in both potential transistor types, subthreshold swing (SS) beyond 60 mV/dec is still the bottleneck coupled with the scaling down of supply voltage and iso-I_{OFF} power consumption simultaneously. The evolution of negative (−ve) capacitance (NC) conception has brought the possibility of realizing sub-60 mV/decade switching by amplifying the gate voltage, while the electronic transport and rudimentary semiconductor physics of the underlying MOSFET endure unchanged [2]. Germanium (Ge) is one of the low-bandgap, energy-efficient materials and having considerably higher electron and hole mobilities than silicon [3]. The Si FinFET and SOI still need higher V_{dd} and hence consume more power. The Ge-on-insulator (GOIs) production is neither cost-effective nor process-compatible when compared to the production of SOI with Smart-Cut technology [4]. The molecular beam epitaxy (MBE) allows high-quality ultrathin epitaxial growth of Ge over the standard Si and enables to harness the accredited supremacy of Ge as a channel and simultaneously exploiting the standard state-of-the-art front-end-of-line (FEOL) Si platform as a low-cost alternative.

The voltage scaling could figure out the higher power consumption by reducing the power per switching event [2]. The overall power consumption can be lowered below the fundamental thermionic limit of SS if the conventional gate insulator is replaced by the ferroelectric (FE) material. Henceforth, the inherent ferroelectricity and spontaneous polarization of FE materials have attracted extensive attention. The conventional perovskite-type FEs, such as $PbZr_{1-x}Ti_xO_3$ (PZT), $SrBi_2Ta_2O_9$ (SBT), and $(Ba,Sr)TiO_3$ (BST), have key process integration issues at the forefront of incumbent CMOS technology. Ge interface compatibility of FE is another key concern. Fortunately, in 2011, it was reported that thin films of Si-doped HfO_2 exhibit ferroelectricity. With the advent of HfO_2 based FE material aside from memory technology [5], [6] has led to a strong interest in NC based FETs. This surprising breakthrough has led to a strong interest in NC-based transistors. Many different dopants such as Si, Al, Y, Gd, and La were reported to promote the stabilization of the o-phase in HfO_2 [7], [8]. However, one of the most feasible and intuitively fab-friendly materials is $Hf_{1-x}Zr_xO_2$ (HZO), with the optimum compositional ratio and a lower crystallization temperature (<500 °C) compared with other contenders [6], [9].

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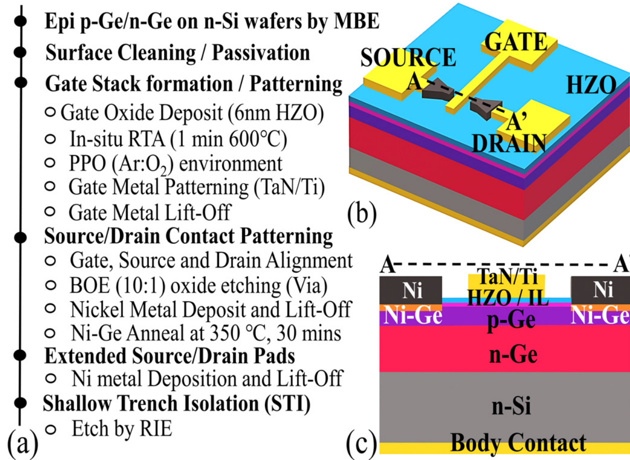

Fig. 1. (a) Fabrication flow for fabrication of p-Ge-on-Si NC FET. (b) Overall fabricated device structure. (c) Vertically cut plane across A–A′ for visualizing the device insight layers.

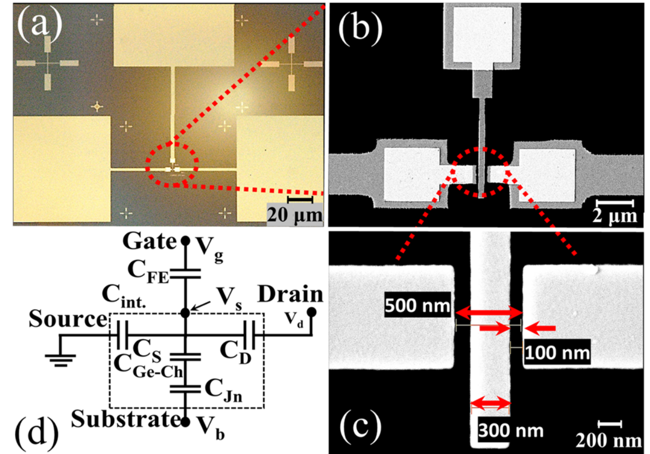

Fig. 2. (a) Optical micrograph of the fabricated device (p-Ge-on-Si) FET. (b) Enlarged view of SEM image demonstrating the DS and gate pads. (c) Zoomed-in view nanoscale channel region. (d) Device capacitance model.

From the integrated circuits (ICs) processing standpoint, Ge FETs have some sort of indispensable challenges. The native GeO_2 is volatile [10], and Ge has low bandgap, leading to high tunneling [11] high contact resistivity on n-Ge [12]. Inversion-mode (IM) MOSFETs exhibit high sensitivity to the interface quality of the gate dielectric, and traverse electric field (EF) affects the carrier mobility. The junctionless transistor (JLT), on the other hand, is expected to be less susceptible to the interface imperfections because of depletion mode operation and lower traverse EFs. However, the realization of ultrathin Ge layers on the insulator is intractable and has yet to be mature [13].

In this work, hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$) (HZO)-based NC FET device structures are fabricated directly on Si substrates. First, the p-Ge channel is epitaxially grown over n-Ge$_{-on-}$n-Si substrates. The physical channel thickness approximation was estimated using the TCAD framework. The optimized 30 nm p-Ge channel thickness is finalized for the prototype device structure fabrication. The effect of body bias on the channel EF and potential was also demonstrated. The HZO stacks were fabricated and optimized for FE properties before integrating them into the FETs. The fabricated NC-FETs are characterized for transfer and output characteristics. The parameters such as SS, DIBL, I_{ON}/I_{OFF}, and V_{th} shift with body bias were extracted.

II. Experiments

Fig. 1(a) depicts the process flow. The ~400 nm of the epi-n-Ge layer with a doping density of 1E18 was grown on an n-type Si substrate with the standard MBE process to minimize thermal expansion mismatch. Thereafter, a defect-free p-Ge channel layer was grown with the same doping density. Around ~30 nm of the epi-p-Ge layer was selected for channel processing. The samples were cleaned in buffered oxide etchant (BOE) (10:1) solution and subjected to the surface passivation with 5 min HCL (36%) immersion. Henceforth, a set of samples were immediately loaded into the sputtering chamber for HZO deposition, and prior optimized process for oxide deposition was carried out at 100 W RF power for 15 min under Ar (70 sccm), process pressure of 5×10^{-3} mbar. Thereafter, the *in situ* rapid thermal annealing (RTA) was performed at 600 °C for 1 min, under (N_2:H_2 90:10) ambient [14]. The post plasma oxidation (PPO) was carried out under Ar/O_2 environment for 1 min. After that, the gate alignment/patterning is performed using electron beam lithography (EBL) and poly (methyl methacrylate) (PMMA) 950K A2 and EL-9 resist. Henceforth, TaN/Ti (50 nm/10 nm) was deposited as a gate material and patterned using the lift-off method. Similarly, the drain/source (D/S) pads were also aligned and patterned, and subsequently developed samples were dipped in the oxide etchant, for opening windows for D/S contacts. Ni (30 nm) metal was deposited for D/S contacts. Afterward, thermal treatment was given for germanide (Ni-Ge) formation at 350 °C for 30 min. The extended D/S pads were patterned by lift-off. Finally, device shallow trench isolation (STI) patterning under the p-Ge layer was done using SF_6/O_2 plasma (reactive ion etching (RIE) tool). At last, the fabricated device structures were annealed under N_2 ambient, at 400 °C for 30 min. The device architecture, optical, SEM micrographs, and model are depicted in Figs. 1(b) and (c) and 2(a)–(d), respectively.

III. Device Optimization and Operation

The channel doping concentration of 1E18 cm^{-3} was selected to ensure high drain current under ON operation, low drain–source (DS) contact resistance, and simultaneously the channel depletion under OFF operation. Here, the gate and bulk (p-n) junction depletion is exploited to squeeze the current in the channel region. Prior to prototyping of device structures, the intended architecture performance is optimized by the Silvaco^{TM} TCAD framework. The models used in this work are: Bohm quantum potential (BQP) (to model the quantum confinement effects), Schlocky–Read–Hall (SRH) to model the carrier recombination, Fermi–Dirac statistics (FERMI), bandgap narrowing (BGN) to model carrier statistics, and Lombardi's to model the carrier mobility [15], [16]. Particularly, to deplete the channel majority carriers, thickness needs to be approximated. Eventually, the channel is analogous to a resistor without gate control. Hereby, by applying a −ve gate voltage, the hole accumulation layer at the gate interface is formed by virtue of majority carriers (holes). In the case of positive (+ve) gate voltage, holes are electrostatically depleted up to a certain depth. Therefore, the width of the depletion layer is a critical parameter for the JLT-FET to

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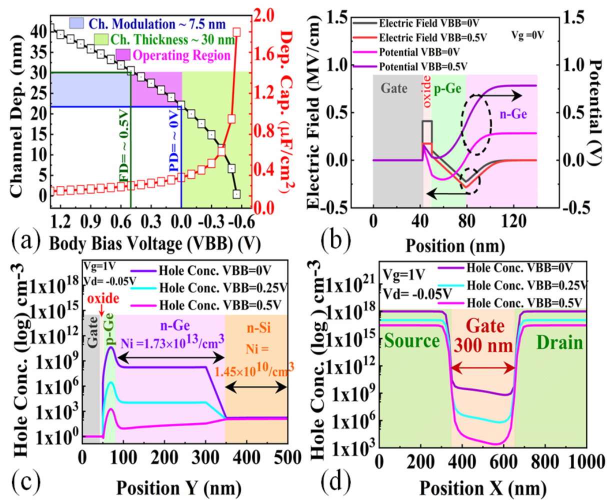

Fig. 3. (a) Channel layer depletion approximation. (b) EF and potential profiles along the device depth. (c) Majority charge carriers depletion in the channel as well as in the device along the y-axis at a gate voltage of 1 V and different body bias voltages at 0, 0.25, and 0.5 V. (d) Horizontally, channel hole carrier concentration depletion w.r.t. gate and body bias at $V_g = 1$ V and $V_d = -0.05$ V.

achieve the full off-state. Considering the above facts of a p-n junction, depletion width exploited for channel depletion has been computed with the variation of body bias voltage (VBB) depicted in Fig. 3(a), akin the cognate junction capacitance is also shown on the double y-axis plot. Albeit, with the application of the +ve voltage at the body contact was also exploited for switching the channel into partially depleted (PD) to fully depleted (FD) channel. The maximum depletion width of the p-Ge layer at zero bias is assessed to be about ~22 nm, considering intrinsic carrier concentration (N_i) of Ge and the dielectric constant (ε_r) to be 1.73×10^{13} cm^{-3} and 16.0 at room temperature, respectively. In order to investigate the channel depletion and effect of body bias onto V_{th} of the top gate, the corresponding EF and potential profiles are simulated. Fig. 3(b) shows the simulated EF and potential plots along the y-axis cutline. As noticed, the peak of maximum EF is confined at the p-Ge and n-Ge junctions, and the depletion width and EF peak vary with the body bias voltage. It implies that the EF across the junction increases. Hence, the channel depletion width expands across the channel thickness as depicted in Fig. 3(b). Similarly, the potential curves are simulated to perceive the channel surface potential modulation with body bias (V). Unlikely, in the bulk devices, the average EF in the p-Ge channel over n-Ge is given by the following relation: $E_{p-\text{Ge(avg.)}} = (\Phi_f - \Phi_b)/t_{p-\text{Ge}}$, where Φ_f is the front surface potential and Φ_b is the backside potential of the channel as presented in Fig. 3(b). As observed, a low transverse field is required to deplete the channel surface with applied VBB, and therefore the channel can be depleted at a lower gate potential. As revealed from Fig. 3(b), Φ_b increases with body bias, so the average EF ($E_{p-\text{Ge(avg.)}}$) required by the gate to deplete the channel gets reduced. These results demonstrate that the channel electrostatics can be modulated markedly by body bias, similar to top gated V_{th} that can be tuned by the second gate in double-gate SOI devices [17]. Due to low transverse field operation, the higher carrier mobility is expected, which gives higher current drive and endorse low voltage and power consumption of transistors. Fig. 3(c) and (d) shows the hole concentration along with the vertical and horizontal directions of the device operation under turn-off conditions, that is, $V_d = -0.05$ V and $V_g = 1$ V. In Fig. 3(c), the cut lines were drawn vertically at $x = 0.5$ and $Y_{\min} = -0.05$, $Y_{\max}$ at 0.5 μm. For Fig. 3(d), the cut lines were made just on the oxide and semiconductor interface. $X_{\min} = 0$, $X_{\max} = 1.0$, and $Y = 0.0005$ μm. It is visible that the majority of charge carriers (holes here) are depleted from the channel region. What is more, the channel hole concentration is reduced to $\sim 1 \times 10^3$ cm^{-3} in the middle of the channel from an initial concentration of 1×10^{18} cm^{-3} at $V_g = 1$ V. Fortiori, the charge carriers at oxide/semiconducting interface are more depleted as depicted in Fig. 3(c). The parabolic profile in the center of the channel confirms the two-sided depletion of the channel region. Similarly, the hole concentration is portrayed through the horizontal profile in DS regions. Specifically, the hole concentration at DS regions shifts from 1×10^{18} cm^{-3} to 3×10^{16} cm^{-3} with variation in body bias from 0 to 0.5 V. These results affirm the transistor action and prelude to implementation of optimized physical channel film thickness of the p-Ge channel.

Even so, the channel depletion can be controlled by the engineered gate work function. Utilizing the low work function of gate metal and channel depletion due to body junction, V_{th} close to ~0 V or even −ve V_t can be possible. In this work, the stack of TaN/Ti with work function values of ($\Phi_m = 4.22 - 4.56/4.33$ eV), respectively, is utilized [18], [19].

To ensure the JLT performance, the D/S contact resistance must be considered beforehand. Ni Fermi level pins close to the valence band of Ge, leading to ohmic contacts between the p-type D/S and the Ni metal [20]. It is important to note that the application of a body bias leads to a reduction in the hole concentration in the channel under the D/S contact and thus increases D/S resistance differing from the simple ohmic behavior. Most metals reacted with Ge only at temperatures well above 450 °C and were prone to oxidation [20], [21]. The NiGe (germanide) is also formed at low-temperature annealing treatment and also shows high resistance to oxidation in 300 °C–760 °C range and having a sheet resistance of (3.1 Ω/□) [22].

In depletion mode devices as current conduction is not sole at the surface as compared to counterpart IM. Besides this, oxide and semiconductor interface quality is still an important aspect. HfO_2 on Ge has been investigated in our previous work and reported elsewhere [23]. PPO-based reports demonstrated the better quality Ge-oxide interface in [24] and [25]. Hereafter, HZO deposition PPO is processed in the presence of Ar and O_2 plasma for high-density GeO_x interlayer (IL) layer formation beneath the HZO layer, which provides a better interface quality and encapsulation of the IL effectually. Considering the volatile nature of GeO_x, the gate first approach is used here for encapsulation. For FE, Hf doped with Zr is considered here. The non-centrosymmetric orthorhombic phase can be achieved in hafnium oxide, if doped with Zr atoms and annealed at optimized conditions to result in the desired strain in the atomic structure. Furthermore, metal capping on the FE layers is employed to impart confined strain during post-deposition RTA treatment [26]. Hence, HZO-based stacks were fabricated and characterized before integration in FET.

IV. Results and Discussion

A. Ferroelectricity Optimization in HZO

For ferroelectricity in TaN/HZO/TaN, structures after annealing at 600 °C, the transient response is studied by

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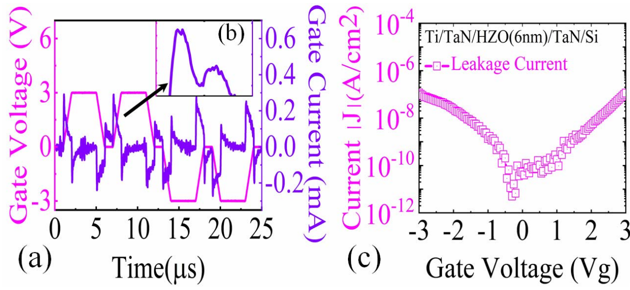

Fig. 4. (a) Transient gate current response of 6-nm thick FE-HZO stacks. Inset in (b): insight enlarged view. (c) Leakage current density in steady dc gate voltage sweep in the TaN/HZO/TaN (MFM) capacitor.

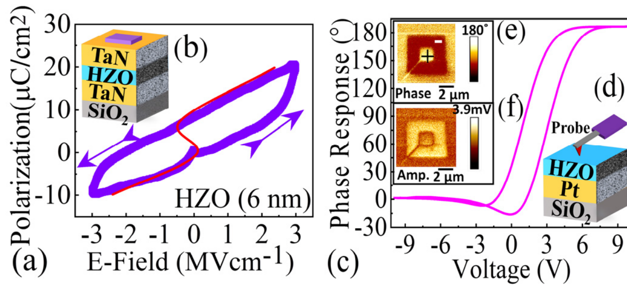

Fig. 5. (a) P–E hysteresis and fitted S-curve for defining the NC operation region. Inset of (b): MFM stack. (c) PFM phase response versus voltage curve. Inset of (d): PFM measurement schematic. Inset of (e) and (f): phase and amplitude contrast images of PFM measurement.

applying ±3 V pulses as shown in Fig. 4(a). The inset in Fig. 4(b), an enlarged view of Fig. 4(a), exhibits the −ve as well as +ve slopes of current switching w.r.t. increasing gate voltage, showing the noteworthy signatures of the NC effect. However, the measured gate current is the sum of FE charges plus leakage current at fast transient pulses. Henceforth, the direct NC observation is not conclusive. Fig. 4(c) shows the gate leakage current of sweep from −3 to 3 V. The ∼1 nA/cm^2 at −1 V reveals the minimal conduction through the HZO thin film at lower voltages, and therefore the current transients at stimulus ±3 V up-down voltage pulses are conceivably on account of FE switching.

Fig. 5(a) and inset of Fig. 5(b) show the polarization versus EF (P–E) loop analysis and fabricated metal-ferroelectric-metal (MFM) stack intended for PE measurement. The triangular pulse excitation (+ve then −ve) is used for polarization extraction. Integration of current flowing through the MFM stack when excited to +ve and −ve pulses sequentially to obtain the P–E loop characteristics in the counterclockwise direction is revealed in Fig. 5(a). The S-curve is fitted by the Landau–Khalatnikov (L–K) relation. Looking at the polarization–EF (P–E) loop characteristics of Fig. 5(a), the system seems multidomain FE rather than the anti-FE as coercivity is around 1.5 MV·cm^{-1}. For voltages less than the coercive field, the ferroelectricity may be due to multidomains, provided EF is not enough to offer the complete polarization. However, for voltages greater than the coercive field, we can visualize the entire alignment of domains around 2.5 MV·cm^{-1} and sharp enough to convince the ferroelectricity inside the HZO system. Moreover, to further confirm the ferroelectricity in the 600 °C annealed layer of HZO, the stack is investigated using piezoresponse force microscopy (PFM) as shown in Fig. 5(c). The inset in Fig. 5(d) shows the device schematic for PFM measurement. The PFM curves depict the coercivity around 2 V and shows saturation at both ends. At higher voltage bias, the system is in full polarization as observed from the PFM results and consistently demonstrates a hysteresis window of ∼2 V. The contrast difference of inner and outer squares for HZO thin films clearly evidences robust 180° polarization reversal, stable, bipolar, remanent polarization states on the application of external EF, attributed from the phase and amplitude PFM surface micrographs as depicted in the inset of Fig. 5(e) and (f), respectively. However, direct transient measurements of thin HZO films in metal/HZO/metal for the P–E loop leads to leakage issues and challenges. Therefore, analogous indirect measurements endorse the direct application of FE on FET gate-stack and by analysis of various criterions such as cyclic hysteresis-free characteristics, subthreshold slope (SS) in both forward/reverse sweep, measuring the drive current, DIBL, and collectively conclude the NC-FET operation.

B. Depletion-Based p-Ge NCFET Operation

The device design considerations for non-hysteretic NCFET capacitance matching, the FE capacitance operating conditions need to be meet. Condition (a): C_{FE} and C_{int} should be as close as possible [27]. C_{FE} is the ferroelectric capacitance and C_{int} is the underlying MOSFET capacitance. The proposed device structure can be represented by the simplified capacitance model [see Fig. 2(d)] to illustrate the voltage amplification (A_v). $A_v = (\partial V_{\text{int}})/(\partial V_G) = |C_{\text{FE}}|/(|C_{\text{FE}}| - C_{\text{int}})$ [28], [29]. C_{FE} is −ve, and A_v will be greater than 1. To achieve large A_v, C_{FE} and C_{int} should be as close as possible. Condition (b): the FE should operate in the NC region for the entire operating biasing range of the S-curve in the P–E loop, if $P_r \geq \sqrt{3}^{*}\varepsilon_{\text{ox}} * E_{\max}$ (MV/cm) μC/cm^2 condition is met [30]. For instance, IL (GeO_2), $\varepsilon_{\text{ox}} = 5.2$ [31], $E_{\max} = 1$ MV/cm, and $P_r \geq 0.795$ μC/cm^2. Fig. 5(c) clearly shows that the remanent polarization P_r value ∼5 μC/cm^2 at zero EF met this condition. Condition (c): to avoid hysteresis, the $C_{\text{FE}} \geq C_{\text{int}}$ [30] condition need to be met. C_{int} is the nonlinear capacitance, which increases with gate charge (Q_g) and asymptotically approaches C_{ox}. Due to junction-less design and thin channel layer, C_{dep} and C_{ox} dominate over the DS capacitance, and DS capacitance can be ignored. Assuming a major contributor of capacitance in the channel region is oxide capacitance, $C_{\text{int}} \approx C_{\text{ox}}$. C_{FE} and C_{ox} are given by the following equations:

$$|C_{\text{FE}}| \approx \frac{3.84 * P_r\left(\mu\text{C}\cdot\text{cm}^{-2}\right)}{T_{\text{FE}}(\text{nm}) * E_c\left(\text{MV}\cdot\text{cm}^{-1}\right)}$$

$$C_{\text{ox}} = \frac{3.45}{\text{EOT}(\text{nm})}\mu\text{F/cm}^2 \quad (1)$$

$$\frac{3.84 * P_r}{T_{\text{FE}} * E_c} \geq \frac{3.45}{\text{EOT}} \Longrightarrow \frac{1.1 P_r}{E_c} \geq \frac{T_{\text{FE}}}{\text{EOT}}. \quad (2)$$

By extracting $E_C = 1$ MV·cm^{-1} and $P_r = 10$ μC/cm^2 values from Fig. 5(a), $T_{\text{FE}} = 6$ nm, EOT $= 0.75$ nm, which satisfies the $C_{\text{FE}} \geq C_{\text{int}}$ condition.

Furthermore, to establish the hysteresis-free operation of the FET structures with HZO, as heretofore FE was characterized for transfer characteristics in both forward and reverse sweeps. Fig. 6(a) depicts the semi-log transfer characteristics of the p-Ge junction-less NC-FETs, measured from −3 to +3 V (forward sweep) and +3 to −3 V (reverse sweep) in dual-mode at fixed V_{ds} of −50 mV, substrate voltage of 0 V, and

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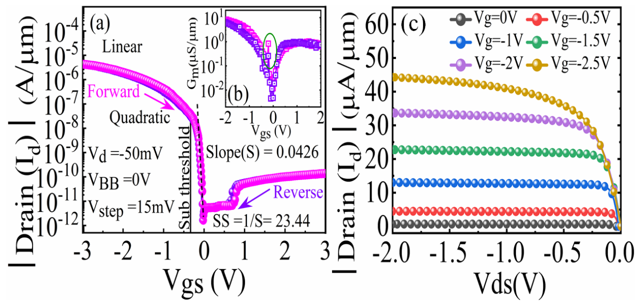

Fig. 6. (a) Hysteresis free transfer characteristics of Ge-on-Si NC FET in both forward and reverse directions. (b) Transconductance (G_m) versus gate voltage curve for p-Ge-on-Si NC FET. (c) I_d versus V_{ds} characteristics.

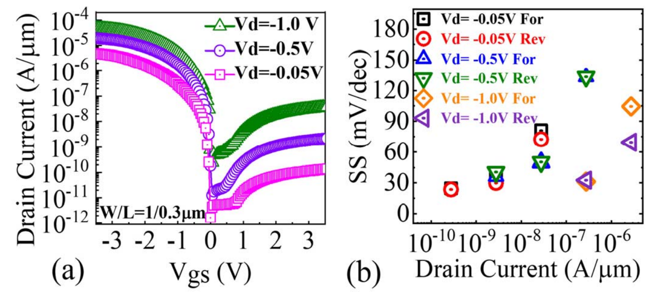

Fig. 7. (a) Transfer characteristics of p-Ge-on-Si NC FET device for various drain voltages. (b) Average subthreshold slope (SS) values w.r.t. the drain current. The SS extracted from forward and reverse sweep transfer characteristics at different drain voltages.

V_{gs} step of 15 mV. As perceived from the sub-threshold region, the characteristics confirm the noteworthy steep threshold swing (SS) of ∼23.44 mV/dec and considerable I_{ON}/I_{OFF} ratio of 10^5, computed from the maximum saturation current in the ON region and current measured at $V_t + 1$ V in the OFF region. The top of the transfer characteristics illustrate the nearly non-hysteresis loop characteristics in forward and reverse sweeps, which substantiates the FE capacitance matching and the FET transfer characteristics follow the S-curve region of the FE capacitor. The NC induces the potential amplification in the channel region, which varies the channel potential state without overriding the drive-in voltage and results in a substantial variation in the drain current w.r.t. the gate voltage. Hence, for the confirmation of NC effect on investigated structures, the transconductance (G_m) versus V_{gs} characteristics were plotted, where transconductance is defined as $G_m = \mathrm{d}I_{ds}/\mathrm{d}V_{gs}$ at fixed V_{ds}. The forward and reverse sweep transconductance are depicted in the inset of Fig. 6(b), and as noticed in the subthreshold region, there is substantial variation in the current w.r.t. very small change of the gate voltage that provides the direct signatures of voltage amplification, due to NC effect, illustrated by the marked peaks in the SS region. In Fig. 6(c), the output characteristics were measured by sweeping the drain to source V_{ds} from 0 to −2 Vs with different gate voltages (V_{gs}) 0 to −2.5 V and measuring the drain current I_d. The results reveal the sharp I_d variation from ∼1 to ∼41 μA/μm with the variation of V_{gs} from 0 V to −2.5 Vs, respectively, at V_{ds} of −1 Vs.

Fig. 7(a) depicts the effect of drain voltage on transfer characteristics which clearly shows that with increasing drain voltage, I_{ON}/I_{OFF} is severely affected which reveals that this is due to increasing horizontal EF component. Increasing drain voltage increases I_{ON} of the device in the linear region that simultaneously increases the leakage currents (I_{OFF}) in the cutoff region possibly due to band-to-band tunneling (BTBT), substrate leakage, and so on. The off-state leakage current is a result of BTBT and low band gap of Ge (0.66 eV), as will be discussed later. However, there is an insignificant change in the SS and V_t observed with increasing drain voltage to −1.0 V. Fig. 7(b) depicts the average (two orders) subthreshold swing (SS) w.r.t. the drain current at different drain voltages. The minimum extracted SS is ∼23.44 mV/dec. Moreover, as in junction-less devices, the physical channel length, ($L_{PHY} = L_{EFF}$), L_{EFF} is the modulated channel length due to drain voltage effect, which may also contribute to lowering SS and SCE. As there is no gate overlap with the drain in the present device architecture, the gate-induced drain lowering (GIDL) is not accountable here.

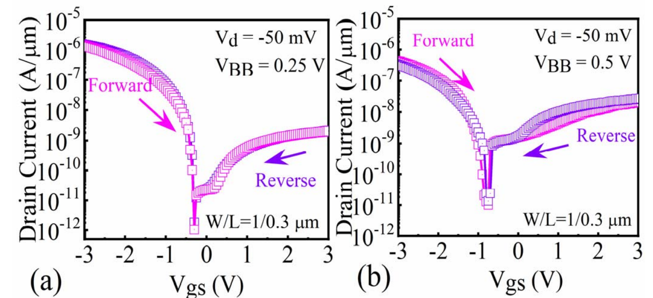

Fig. 8. Forward and reverse sweep transfer characteristics at body bias voltage of (a) 0.25 and (b) 0.5 V, respectively.

Apart from the NC behavior of the devices, the effect of body bias on transfer characteristics is explored, to study the shift of threshold voltage. Fig. 8(a) and (b) shows the influence of the body biases 0.25 and 0.5 V on the I_d–V_{gs} characteristics at $V_d = -0.05$ V, respectively. By comparing Fig. 8(a) and (b), it is clear that the threshold voltage is shifted to the −ve side. At the same time, the I_{ON}/I_{OFF} ratio is badly affected if the body bias is raised to −0.5 V, as body bias modulates the depletion region in the channel, and with an increase of the body bias, the depletion region expands toward the channel surface, depletes the channel, and results in the variation of the I_{ON}/I_{OFF} current ratio. There is a significant shift in the reverse drain current (I_d) at $V_{gs} = 0$ V with variations in VBB of 0.25 and 0.5 V. This is may be due to the fact that the drain terminal is at −50 mV and body bias VBB at 0.5 V reverse biases the p-n junction exists between the drain and body region, results in an increase I_d as leakage current due to minority carriers flows through the drain and substrate which is also responsible for shifting the I_d minima in off state. This increased I_d due to leakage much experienced in the off-state w.r.t. on-state as the channel is already depleted with gate and body bias voltages, so the minority carrier leakage current might be following the path between the drain and the substrate. In other words, at $V_{gs} = 0$ V, the reverse I_d =∼2E−11 A/μm at VBB of 0.25 V increases to I_d =∼2E−9 A/μm at VBB of 0.5 V, that is, ∼2 order difference. Additionally, there is a shift in the I_d minima observed due to increased leakage. In Fig. 8, the effect of body bias is demonstrated for achieving the low threshold voltage, but yet again as stated, the body bias voltage (VBB) introduces

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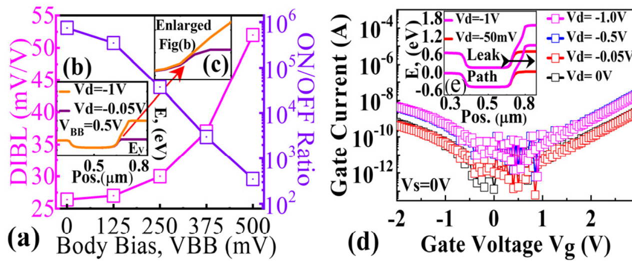

Fig. 9. (a) DIBL and I_{ON}/I_{OFF} ratio w.r.t. VBB. Inset of (b): energy (E) (eV), hole conduction level at $V_d = 0.05/-1$ V. Inset of (c): enlarged view of (b). (d) Gate current leakage versus gate voltage curves at source voltage (V_s), 0 V. Inset of (e): possible leakage path due to BTBT.

nonlinearity in the system, resulting in capacitance mismatch. The operation region in the S-curve in the P–E loops interrupts. It affects FE switching along with non-perfect capacitance matching, revealing that abrupt changes in the I_d minima may be due to FE switching. These experimental results are in line with our simulation study. However, this effect can be exploited to switch the low power and high-performance mode of the transistors by modulating V_{th}. The results reveal that V_t shifts from -0.6 to -1.1 V with a VBB of 0.25 and 0.5 V, respectively.

In short-channel devices, the drain effect hardly hits the gate control. However, in the proposed JLT architecture, the drain voltage does not much affect the gate (channel) potential. The measured DIBL is ~26 mV/V at drain voltages $V_d = -50$ mV, $V_d = -1$ V, and VBB $= 0$ V. Moreover, with increasing body bias, the DIBL is slightly increased to ~52 mV/V. The drain-side space charge region is increased due to reverse bias of the p-channel region and n-bulk region and significantly influences the potential at channel regions more likely toward the drain. The extracted DIBL for various body bias voltages is depicted in Fig. 9(a). The hole conduction band (E_v) levels for $V_d = -0.05$ V, -1 V at VBB $= 0.5$ V are shown in the inset of Fig. 9(b) and enlarged view in Fig. 9(c). A very slight band bend at the corner of the band is observed if V_d increased to -1 V from -0.05 V, which may be responsible for the trivial DIBL variation, and no barrier lowering due to drain voltage is observed. The influence of the DIBL can also be directly experienced by looking at the transfer characteristics under subthreshold region at different V_d voltage as depicted in the transfer characteristics plotted in Fig. 7(a) and all characteristics are coinciding under the subthreshold region concludes the insignificant impact of DIBL. Similarly, the extracted I_{ON}/I_{OFF} ratio with VBB is depicted in the double y-axis plot in Fig. 9(a). The computed I_{ON}/I_{OFF} ratios are estimated at the OFF current at V_t+1 V. The calculated I_{ON}/I_{OFF} ratio is approximately 10^5 and 10^2 at, VBB $= 0$ and 0.5 V, respectively.

In continuation with the results of Fig. 7, initially, it is assumed that drain current leakage at higher drain voltages may be through gate oxide leakage. This is confirmed by measuring the gate current versus gate voltage at different drain voltages ($V_d = -0.05, -0.5, -1$ V) as depicted in Fig 9(d). The gate leakage current less than ~1 nA, at V_t+1 V at $V_d = 0$ V. Also, it is observed that at low $V_d = -50$ mV, the gate leakage current is comparable to the drain leakage current. When $|V_d| = 1$ V, the gate leakage is much smaller than the absolute drain leakage current. Extracted drain leakage current is considered here, at $V_t + 1$ V [32]. In Fig. 9(d), the curves with ($V_d = 0, -0.05$) and ($-0.5, -1.0$ V) V fall on top of each other, which signifies that increase of drain potentials affects the drain leakage but not the gate leakage. So, gate oxide leakage is obsoleted here. This indicates that the drain leakage current varies probably due to BTBT or substrate leakage. In Fig. 9(e), it is clearly observed that the leakage path exists due to band overlapping with variation in the drain voltage $V_d = -50$ mV to -1 V as depicted in Fig. 9(e). BTBT seems to be the dominant gate leakage mechanism here, although Ge is an indirect bandgap material, and the direct transition is usually dominating in the BTBT process. Considering this fact into account, the remaining intrinsic or thermally generated strain is known to increase direct BTBT, thereby increasing the leakage current [33], [34]. Therefore, proper strain management is an important factor for the significant reduction in the leakage current. At higher drain voltages ($V_d = -1$ V), it is observed that substrate leakage due to minority carriers may also be responsible for off-state leakage alongside BTBT. This is inline with the discussion in Fig. 8. Table I depicts the benchmark comparison of Ge/HZO devices published recently.

TABLE I
EXPERIMENTAL BENCHMARK DEVICE PARAMETERS FOR GE-FETS

Device	Gate Stack	Structure	W/L	SS mV/dec	Ref.
Si	TiN/HfZRO & TaN/HfO_2	Planer pFET	136μm/ 20 μm	52	[35]
Ge	TiN/HZO/ IL/Ge	NW n-FET	L_g=60nm	54	[36]
GeOI	Al_2O_3/HZO/ Al_2O_3/GeO_x	n-Fin FET	41 nm/ 302 nm	43	[37]
Ge Bulk	TaN/HZO/TaN/HfO_2	Planer pFET	L_g=5 μm L_g=2 μm	43	[38]
GeSn	TaN/HZO/TaN/HfO_2	Planer pFET	L_g=5 μm L_g=2 μm	40	[38]
Ge-on-SOI	HZO/GeO_x	p-Fin FET	20 nm/ 100 nm	86	[39]
Ge-on-Si	TaN/HZO/ GeO_x	Planer pFET	1 μm/ 0.3 μm	23.44	This Work

V. CONCLUSION

This work proposes the utilization of MBE-processed epi-Ge as channel material on standard silicon wafer. CMOS-compatible HZO integrated in the gate-stack to breach the Boltzmann's Tyranny limit <60 mV/dec with the ease of fabrication process. The performance of fabricated FETs was measured, with low SS = ~23.44 mV/dec, considerable I_{ON}/I_{OFF} ratio = ~10^5, and low DIBL = ~26 mV/V. However, due to low $E_g = 0.66$ eV of Ge, the fabricated devices experienced the drain leakage current issue with increment in the gate bias in the off-state, which can be further overcome by adjusting the channel and substrate doping to reduce the substrate leakage. MESA-based Fin architecture not only reduces the leakage, but also increases the channel coupling.

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