Two-Dimensional Van Der Waals Hafnium Disulfide and Zirconium Oxide-Based Micro-Interdigitated Electrodes Transistors

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***Abstract*— There are indelible challenges related to transistor action and realization of emerging two-dimensional van der Waals (vdW) multilayer ($2D_{ml}$) field-effect transistors (FETs), to the post silicon technology era. For scalability, a cost-effective large area ultrafine thin films interface and band alignment of multilayer channel material with compatible gate dielectric are essential. Here, $2D_{ml}$ hafnium disulfide (HfS_2) and ZrO_2 are employed as channel material and gate dielectric, respectively, and anticipated that vdW interaction of said structures entails the high-quality interface with trivial dangling bonds and defects caused by lattice mismatch. The investigated $Al/ZrO_2/HfS_2/Al_{\mu\text{-IDE}}$ FETs exhibit the subthreshold swing (SS) ~65 mV/dec, I_{ON}/I_{OFF} ratio of ~104, transconductance of ~3.99 μS, effective mobility of ~74 cm^2/Vs at V_{gs} of 2 V, and leakage current density of ~33.8 nA/cm^2 at V_{gs} of −1 V. Thus, the steep SS, sturdy current saturation, low-voltage operation (~3 V), and leakage current establish the potential candidature of HfS_2 and ZrO_2-based 2-D FETs for both conventional and ubiquitous electronics.**

***Index Terms*— 2-D field-effect transistors (FETs), hafnium disulfide (HfS_2), high-quality interface, micro-interdigitated electrodes (μ-IDEs), van der Waals (vdW) interaction, ZrO_2.**

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I. Introduction

THE current bottleneck of forefront silicon technology can be excelled by layered van der Waals (vdW) transition metal dichalcogenides (TMDs), due to intuitive protean properties, such as ultimate scaling of material dimension in the vertical direction, minimization of the local potential variation at interface, extremely ultrathin channel geometries down to ~5 nm or beyond, finite bandgap, high carrier mobility, and promising ability to push scaling limit of 2-D electronics [1]. The key exotic feature of multilayered ($2D_{ml}$)-based TMDs involves vdW interactions among the staking layers yielding a high-quality transistor-level film interface [1], [2], [3], [4], [5].

Hence, two-dimensional multilayer ($2D_{ml}$)-based TMDs offer numerous benefits to extend further scaling trends of the electronic devices beyond Moore's law and render the attractive feasibility for nanoelectronics [6]. Recently, the ample of $2D_{ml}$-based TMDs in particular MoS_2, $MoSe_2$, WS_2, WSe_2, hafnium disulfide (HfS_2), and so on has attracted considerable attention, and a collection of them has been reported to a large extent [7], [8], [9]. Amid of these, HfS_2 has lately staged a potential candidature and complement to conventional 2-D TMDs due to octahedra coordination structure, monolayer thickness of ~0.59 nm, and considerably high simulated electron mobility of ~1833 cm^2/V-s in contrast to analogous systems. Also, HfS_2 remained less explored for the realization of the next-generation IC applications on various platforms. Over and above, the HfS_2 direct bandgap of ~1.2 eV is advantageous over silicon for suppressing the source-to-drain tunneling and extending the scaling limit of transistors [10], [11], [12], [13].

In addition to many integration challenges of $2D_{ml}$ TMDs for future CMOS technology, the accessibility of a compatible gate dielectric is foremost for better device performance and lower power consumption. There are different pathways for the reduction of power consumption, such as the 1) reduction of operating voltage to lessen the switching power; 2) minimization of standby power by lowering OFF-state leakage current; and 3) reduction of the subthreshold slope to turn the transistor "ON" at a relatively low voltage [14]. The high-κ gate dielectrics integration with alternate semiconductors has emerged as a promising solution to the enhancement of

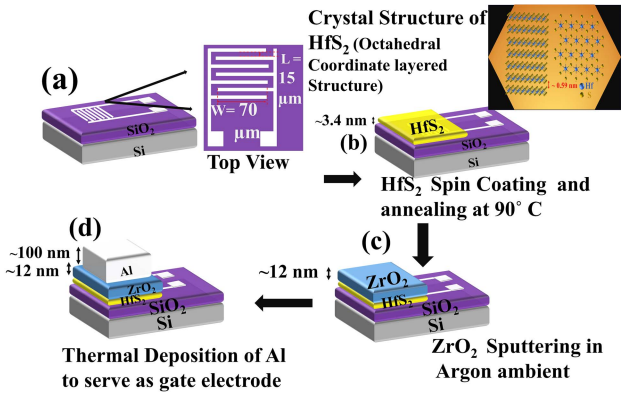

Fig. 1. Schematic process flow for the fabrication of Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ device structure. (a) μ-IDE through Photolithography. (b) Spicoating of HfS_2. (c) RF sputtering of ZrO_2. (d) Thermal deposition of Al.

transistor performance as it reduces gate leakage current with physically thicker film and enhances carrier mobility [15]. There is negligible accessibility of dangling bonds in multilayered ($2D_{ml}$)-based TMDs; hence, one cannot expect the formation of new interfacial bonding with typically oxygen-containing high-κ dielectrics [2], [16]. Furthermore, the vdW-based $2D_{ml}$ TMDs/high-κ dielectric structures can enhance the transistor action due to lower trap density with minimal lattice mismatch at the interface [17].

Limited reports are available, where HfS_2 as a channel material is integrated with high-κ dielectrics like HfO_2 [18]. To the best of our knowledge, there are no such reports of ZrO_2, in the amorphous phase being used as a dielectric to integrate with 2-D, vdW multilayered HfS_2 on micro-interdigitated electrodes (μ-IDEs)-based field-effect transistors (FETs) structures.

This work, hereby, for the first time provides a novel insight into the multilayer (~5 layers, monolayer thickness ~0.59 nm [11]) HfS_2-based FETs with ZrO_2 high-κ dielectric in the top-gated configuration and the deployment of Al μ-IDEs as the source and drain for better electrical performance and nanoelectronics applications.

II. Experiment

The Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$-based FETs have been fabricated on SiO_2/Si substrates, as presented in Fig. 1. Initially, the deposition of aluminum thin film (~40 nm) is performed by thermal evaporation at $\sim 1 \times 10^{-6}$ mbar pressure. After that, Al μ-IDEs are patterned by standard Maskless Lithography (Intelligent Micro Patterning) process, already elucidated elsewhere [18], [19], [20]. The negative tone standard photoresist, SU-8 (2002, Micro-Chem) is spin-coated on the Al/SiO_2/Si substrate at the wetting cycle of 500 r/min followed by a spreading cycle of 3000 r/min to obtain a thickness of ~2 μm. The samples are then subjected to pre-exposure bake (PB) from room temperature (RT) to 95 °C for 10 min, and after PB, the samples are cooled down to RT again. After the PB process, the samples were exposed to the illumination of ~365 nm, UV irradiation, using maskless optical lithography to pattern μ-IDEs structures. Subsequently, the samples are subjected to postexposure bake (PEB) from RT to 105 °C for 10 min. Thereafter, SU-8 developer (Micro-Chem) is used to develop the patterned μ-IDEs for 1 min followed by isopropyl alcohol (IPA) rinse and nitrogen (N_2) gas purging and performed the hard bake at 150 °C for 20 min. To pattern, the Al μ-IDEs samples are etched through the standard Al etchant [19]. The SU-8 covering the desirable Al is stripped from samples by using N-methyl-2-pyrrolidone (NMP). The samples are incessantly stirred in NMP at 50 °C for about 5 h and rinsed by IPA to remove the NMP.

Here, the channel length (L) and width (W) of the device are chosen as ~15 and ~70 μm, respectively. In the next step, few layers (~6 layers) of HfS_2 are spin-coated over, aluminum, μ-IDE/SiO_2/Si substrates. Here, HfS_2 is synthesized by low-cost hot injection method using hafnium chloride and carbon disulfide as formulation precursors at 350 °C [20], [21]. Furthermore, amorphous ZrO_2 thin films are deposited at $\sim 5 \times 10^{-3}$ mbar process pressure by RF magnetron sputtering from a ZrO_2 target (purity 99.99%) with the power of ~130 W and continuous Ar (80 sccm) flow. Finally, the top metal gate Al (~100 nm) is thermally evaporated through a shadow mask confined over the μ-IDE's fingers, as shown in Fig. 1.

The thickness and dielectric constant of the as-deposited ZrO_2 film are analyzed by variable angle spectroscopic imaging ellipsometer (EP4-SE; Accurion). The optical thickness and dielectric constant of as-deposited ZrO_2 thin films are measured to be ~12 and ~14 nm, respectively. Moreover, the physical thickness of HfS_2 and ZrO_2 is confirmed using line profile in atomic force microscopy (AFM) tapping mode and estimated to be ~3.4 and ~11.8 nm, respectively. The estimated rms surface roughness of the ZrO_2 and HfS_2 is ~0.2 and 1.2 nm, respectively, from AFM surface micrographs discussed next.

The chemical analysis of HfS_2 formulation has been confirmed by the confocal Raman spectrophotometer (LabRAM HR Evolution; Horiba) with the excitation wavelength of ~532 nm in the range of 330–350 cm^{-1}, as represented in Fig. 2(a). The μ-Raman spectrum peak near ~336.6 cm^{-1} confirms the presence of a first-order A1g peak of HfS_2. Fig. 2(b) shows the surface morphology of the as-deposited ZrO_2 thin films, which reveals rms surface roughness of ~0.2 nm and confirms exceptionally smooth ZrO_2 thin films suitable for nanoelectronics applications. Furthermore, the height profile and the surface morphology of spin-coated multilayers HfS_2 have been analyzed by tapping mode AFM (Dimension Icon Bruker), as shown in Fig. 2(c) and (d), respectively. The AFM surface micrographs revealed uniformly distributed ~3.4 nm thickness of HfS_2 flakes, suitable to be confined in the μ-IDE's fingers. The depth profiling X-ray photoelectron spectroscopy (XPS) analysis for the ZrO_2/HfS_2 hybrid structure deposited over SiO_2 is shown in Fig. 2(e) (i). Zr3d and O1s scans [see Fig. 2(e) (ii)] were performed during the depth profile analysis, where the peaks are observed at 183, 186, and 531 eV [22]. Hf 4f scan and S 2p scan were performed and peaks are observed at 16 and 18.3 eV for Hf and for sulfur peaks are observed at ~163.4 and ~164 eV [23]. It is revealed from the XPS profiling that there is very less interaction of the hafnium atom from HfS_2 with the oxygen atoms of the ZrO_2. The negligible

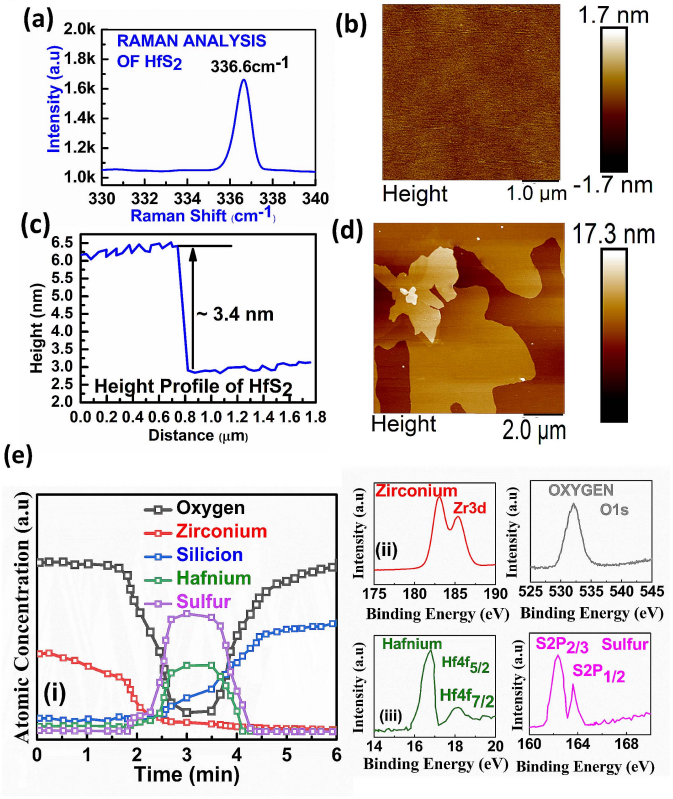

Fig. 2. (a) Confocal μ-Raman spectroscopy of spin-coated HfS_2 ultrathin films at RT. (b) Surface micrographs of sputtered ZrO_2 thin films. (c) Thickness profile of spin-coated HfS_2 ultrathin films. (d) Micrographs of spin-coated HfS_2 thin films. (e) (i) Depth profiling XPS analysis for the ZrO_2/HfS_2 hybrid structure deposited over SiO_2, (ii) XPS of the sputtered ZrO_2, and (iii) XPS of the spin-coated HfS_2 taken while depth profiling.

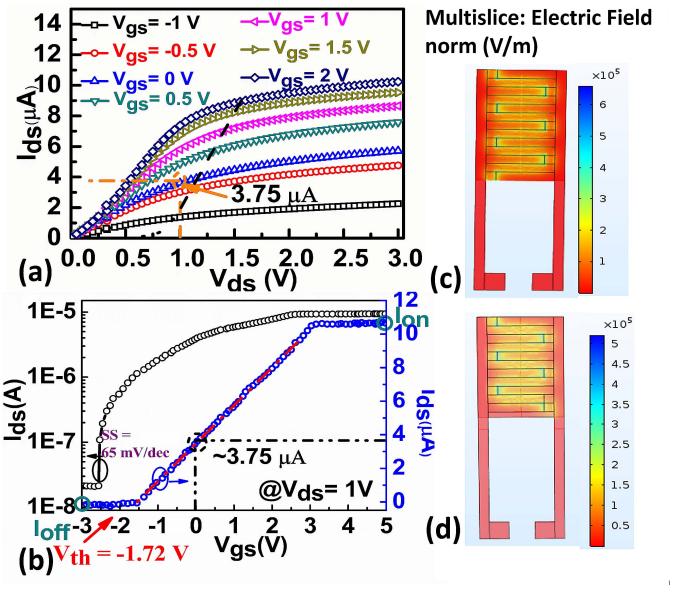

Fig. 3. Electrical characteristics of the μ-IDE-based FET on SiO_2 substrate. (a) Output characteristics of the $Al/ZrO_2/HfS_2/Al_{\mu\text{-IDE}}$ μ-IDE. V_{ds} was swept from -1 to 2 V at each V_{gs} varied from -1 to 2 V with a step of 0.5 V. (b) Transfer characteristics at $V_{ds} = 1$ V varying the V_{gs} from -3 to 5 V. Electric field distribution simulation using Comsol Multiphysics of (c) asymmetric IDEs structure: seven fingers structure (four source contact and three drain contact). (d) Symmetric IDEs structure: six fingers structure (three source contact and three drain contact).

broad peak of HfO_2[see Fig. 2(e) (iii)] near 18.5 eV may be attributed to the residue left while etching of the structure. The sharp decrease in the oxygen concentration when hafnium and sulfur concentration rise justifies that there is no bond formation between Hf–O and S–O as there is no corresponding peak observed. Therefore, ZrO_2/HfS_2 interface is mainly vdW interaction since Hf–O or S–O covalent bonds are below the detection limit while performing the depth profiling of the structure [24].

Confocal Raman spectroscopic analysis has performed with the excitation wavelength of 532 nm for the confirmation of HfS_2, as represented in Fig. 2. The Raman spectrum peak near 325 cm^{-1} confirms the presence of A_{2u} mode for 1H phase of HfS_2, which corresponds to the out-of-plane vibration of S atoms in the HfS_2 structure. Similar observations are noticed by Singh et al. [25] and Taur and Ning [26].

The electrical characterization of fabricated $Al/ZrO_2/HfS_2/Al_{\mu\text{-IDE}}$, 2-D FETs consisted of measurements of $I_{ds} - V_{ds}$, $I_{ds} - V_{gs}$, capacitance–voltage (C–V), and J_g–V_g characteristics. These measurements were conducted using Keithley 4200 SCS parameter analyzer at RT.

III. Results and Discussion

The output (I_d–V_{ds}) characteristics of the $Al/ZrO_2/HfS_2/Al_{\mu\text{-IDE}}$-based FETs are depicted in Fig. 3(a). As can be noticed, adequately respectable output characteristics are demonstrated with the definite transition from linear region to saturation region and distinct cutoff region.

The partially good ohmic contact between the μ-IDE and HfS_2 leads to the linear behavior of I_{ds} versus V_{ds} characteristics. The high-κ dielectric ZrO_2 leads to the significant enhancement in drain saturation current (~10.2 μA at $V_{gs} =$ 2 V) as compared to our previous work with HfO_2/HfS_2 system [18] (~5.8 μA at $V_{gs} = 2$ V). This implies higher gate control through band alignment over the channel region in ZrO_2/HfS_2 system, hence increasing the stability. The ameliorated gate coupling with ZrO_2 as a dielectric is evident and leads to the demonstration of strong drain current saturation (~10.2 μA at $V_{gs} = 2$ V). The output transfer characteristics (I_{ds}–V_{gs}) obstinate by measuring the drain current (I_{ds}) as a function of gate voltage (V_{gs}) at a fixed drain voltage (V_{ds}) confirm the gratifying transistor action, as shown in Fig. 3(b). The electrical characteristics, such as the current I_{ON}/I_{OFF} ratio, subthreshold swing (SS), and threshold voltage (V_{th}), are computed to be ~10^4, 65 mV/decade, and ~-1.72 V, respectively. I_{ON}/I_{OFF} ratio is computed from the transfer characteristics at a given V_{ds}, where I_{OFF} and I_{ON} at $V_{gs} = -3$ and 5 V, respectively. In spite of Fig. 3(b) depicts the standard graphical approach followed to calculate I_{OFF} (OFF state) at $V_{gs} \sim -3$ V, where I_{ds} intends to minimum of ~9×10^{-9} A and active $2D_{ml}$ $Al/ZrO_2/HfS_2/Al_{\mu\text{-IDE}}$ channel is considered fully depleted.

Likewise, I_{ON}(ON state) computed at 5 V, where I_{ds} approaches to maximum of ~1.08×10^{-5} A as also reported by Kanazawa et al. [11] for computation and signified with red circle in the graphs for better understanding. Thus, the

computed I_{ON}/I_{OFF} ratio is around $\sim 10^4$ order. The threshold voltage (V_{th}) is computed from standard established technique [27] from linear extrapolation of I_{ds}–V_{gs} curve and estimated to be ~ -1.72 V, as shown in Fig. 3(b). $2D_{ml}$, $Al/ZrO_2/HfS_2/Al_{\mu\text{-IDE}}$ structure field-effect mobility (μ) was reckoned by fitting the plot of I_{ds} versus V_{gs} at a fixed drain voltage of 1 V using the slope of the transfer characteristics in the following relation [28], [29]:

$$\mu = \frac{\partial I_{ds}}{\partial V_{gs}} \frac{L}{WCV_{ds}} \tag{1}$$

where C is the total effective capacitance of $Al/ZrO_2/HfS_2/Al_{\mu\text{-IDE}}$, which is the series combination of oxide capacitance (C_{ox}) and quantum capacitance of the channel (C_q), W and L are the channel width and length, respectively, and $(\partial I_{ds}/\partial V_{gs})$ is the maximum transconductance derived from the transfer characteristics as similarly extracted by Jun et al. [30], hence leads to calculated electron mobility of ~ 74 cm^2/Vs in the linear regime and in the saturation regime, the mobility is ~ 2.71 cm^2/Vs [20].

The prominent role in enhancing the device performance is the device structure. The electric field distribution of the asymmetric (seven fingers) and symmetric (six fingers) simulated through Comsol Multiphysics 5.2 is shown in Fig. 3(c) and (d). The device dimensions and simulation parameters were kept constant for both the structures to verify the amount of electric field distribution along the finger gap. The gap was filled with HfS_2 semiconducting channel material, and the fingers' material was defined as aluminum similar to the fabricated structure. It has been already reported that the asymmetrical structure generates a higher electric field than the symmetrical structure [31], [32]. It is clearly depicted in Fig. 3(c) and (d) that the maximum field generated by the asymmetrical and symmetrical structure is $\sim 600\ 000$ and $\sim 500\ 000$ V/m, respectively.

Fig. 4(a) shows the cyclic C–V characteristics retrieved by sweeping the gate voltage from accumulation (+5 V) to inversion (−5 V) to (+5 V) at 500 kHz. The cyclic CV justifies the fact that there is low charge trap density at the interface and there is negligible change in the threshold voltage, which justifies the stability and reliability of the structure. The inclusion of ZrO_2 as the dielectric layer reduces the slower border traps. The slower border traps can charge during device operation, thereby causing a shift of the threshold voltage, which, over time, accumulates and leads to device failure. Although HfS_2 is intrinsically n-type, behaves as the active channel at $V_{gs} > 0$ V leading to transistor operation in accumulation region. Similar observations are also made from the output characteristics, and the majority charge carrier (electrons) accumulates in the channel region that leads to increases in I_{ds} when V_{gs} varies from 0 to 2 V, while at $V_{gs} < 0$ V, the channel depletes gradually, baptize from the decrease in I_{ds} with the change in V_{gs} from −1 to −2 V in the output characteristics. This results from the depletion of majority charges in channel region or at the interface of ZrO_2/HfS_2, which eventually onsets region for the inversion of the charges beyond −2 V [33], [34].

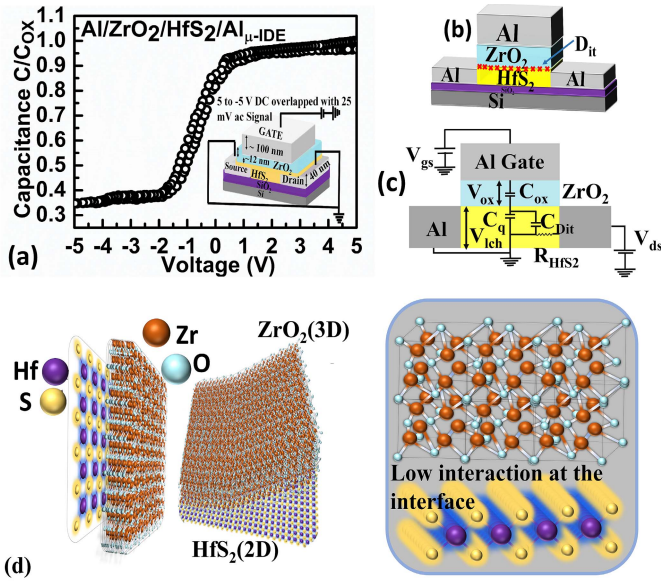

Fig. 4. (a) C–V characteristics of $Al/ZrO_2/HfS_2/Al_{\mu\text{-IDE}}$ device at 500 kHz. (b) Schematic of the density of trap charge in HfS_2/ZrO_2 interface. (c) Equivalent circuit of the varying capacitance including the contribution of trap charges (C_{it}) and quantum capacitance (C_q) [18]. (d) Schematic representation of the quasi-vdW interaction mechanism between HfS_2 and ZrO_2 system explaining no covalent bond formation between Hf–O and S–O.

Fig. 4(b) shows the effective capacitance dispersal for $Al/ZrO_2/HfS_2/Al_{\mu}$-IDE structure, where the overall effective capacitance has resulted from the synergy of various network capacitances, such as quantum confinement in the channel region (C_q), the trapped charges (C_{Dit}) at the ZrO_2/HfS_2 interface, and the oxide capacitance (C_{ox}). Apart from this, the excess charge carriers generation in $2D_{ml}$ HfS_2 channel region might be due to the partial penetration of the external electric field owing to the applied gate bias (V_{gs}), attributed to the quantum capacitance (C_q) [18], [35], [36]. Even though the quantum capacitance (C_q) is the function of the localized channel potential (V_{lch}) since the voltage dribbled across the channel is less than the applied bias at the gate terminal, the quantum capacitance (C_q) can be expressed as [35]

$$C_q = -\frac{\partial Q_{ch}}{\partial V_{lch}}. \tag{2}$$

The interface trap density for $Al/ZrO_2/HfS_2/Al_{\mu}$-IDE structure, which is responsible for affecting the device performance, primarily originates and schematically represented in Fig. 4(b). In the presence of the trap at the interface of the semiconductor, the interface traps density (D_{it}) and the capacitance associated with these traps are in parallel with the depletion capacitance (C_D), which is estimated to be $\sim 7 \times 10^{10}$ eV^{-1} · cm^{-2} [20], [37]. The significantly lower interface trap density justifies the high-quality interface between the ZrO_2/HfS_2 channel region.

Besides this, contrary to the conventional epitaxy standard processes of semiconductor heterostructures devices, vdW interaction enables us to produce the high-quality interfaces between diverse 2-D materials and high-k dielectrics without any serious concerns for their compatibility during the

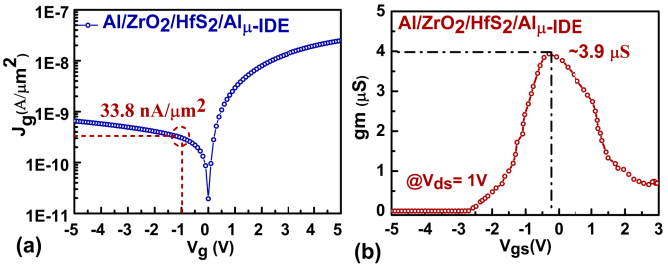

Fig. 5. (a) J_g–V_g (density of gate leakage current versus applied gate bias) at $V_{ds} = 0$ V and (b) g_m–V_{gs} (transconductance versus gate bias) at $V_{ds} = 1$ V characteristics of Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ μ-IDE FET fabricated structure.

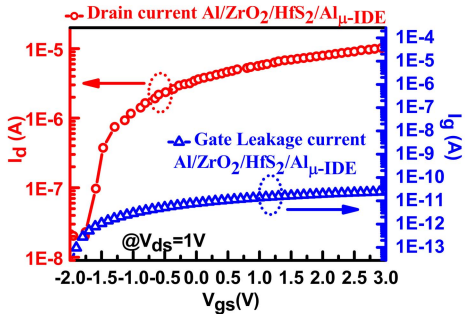

Fig. 6. Drain current (I_d) and gate leakage current (I_g) (logarithmic scale) versus applied gate bias (V_{gs}) for Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$FETs in the operating range of the FET when the applied bias drain bias ($V_{ds} = 1$ V).

standard fabrication process. Here, considering the low thermal budget-based opted approach for Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ structures fabrication may not be drawn up any major chemical interaction formulated by cleavage of interfacial species old bonds and formation of new ones as revealed from Fig. 2(e). Hence, the high-quality interface and electrical characteristics of $2D_{ml}$ HfS_2 layer and ZrO_2 oxide system are borne out by vdWs interaction for Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ aforesaid structures. The key advantage of this type of weak interaction between 2-D semiconducting film and 3-D oxide results in a forbearance of lattice match and minimum strain effect on the semiconducting film [38], as schematically depicted in Fig. 4(d). The absence of dangling bonds and strong covalent interaction between HfS_2 and ZrO_2 allows for the fabrication of device quality sharp interfaces and permits the downscaling of devices realized by standard semiconductors processes. Due to this, the ions in ZrO_2 can accommodate the change in the local chemical environment produced in HfS_2 because of applied bias. It is, therefore, less probable that defects will be formed at the surface or interface. Furthermore, the ZrO_2/HfS_2 structure displays a weak noncovalent interaction at the interface, which results in the maintenance of the effective mass of HfS_2 as the free-standing form, which leads to the minimum distortion of the electronic property of the 2-D HfS_2 and hence the high-quality interface and higher mobility [39]. Therefore, the Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ transistors based on vdW exhibit firm potential in the next-generation digital logic applications with low-power ICs.

The leakage current density-voltage (J–V) characteristics at $V_{ds} = 0$ V are shown in Fig. 5(a). For the higher lifetime of FETs, the static power dissipation (at OFF state of the devices) should be as low as possible. Therefore, the gate leakage current is assessed as ~33.8 nA/cm^2 at -1 V (V_{gs}) gate voltage. This computed markedly low gate leakage current density (J_g) evidently and establishes that ZrO_2 acts as a potential next-generation gate dielectric for $2D_{ml}$-Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ FETs with improved transistor action and performance. Next to this, for the implementation of $2D_{ml}$-Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$-based FETs for high performance and functionality, IC applications, the transconductance (g_m) serves a pivotal role in the transistor gain, an imperative criterion, especially for the device to chip-level implementations. Fig. 5(b) shows the

TABLE I
COMPARISON OF SS AND MOBILITY (μ) FOR VARIOUS STATE-OF-THE-ART TMD MATERIAL

TMDs	Synthesis	SS	V_{gs} (V)	μ (cm^2/V-s)	Ref
MoS_2	Mechanical exfoliation	140 V/dec	2	512	[41]
WSe_2	Mechanical exfoliation method	15000	40	4.7*E-3	[42]
MoS_2/ HfS_2	Mechanical exfoliation method	300	12	-	[43]
WS_2	Mechanical exfoliation method	70	-	20	[44]
HfS_2	Mechanical exfoliation method	156 mV/dec	2	0.75	[45]
HfS_2	Mechanical exfoliation method	-	40	45	[11]
HfS_2	Mechanical exfoliation method	-	80	7.6	[46]
HfS_2	Chemically Synthesized	70	2	56.7	[18]
HfS_2	**Chemically Synthesized**	**65**	**2**	**74**	**This work**

transconductance of Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ FETs assessed by the following relation:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}. \tag{3}$$

The FETs performance increases at minimum contact resistance. Thus, for the integration of $2D_{ml}$-Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ in ICs, the transconductance (g_m) magnitude should be as high as possible [40]. Here, the calculated transconductance (g_m) of Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ FETs is ~3.99 μS. The drain current at the fixed gate bias (transfer characteristics) and the gate leakage characteristics for Al/ZrO_2/HfS_2/$Al_{\mu\text{-IDE}}$ 2-D FETs at fixed drain bias (V_{ds}) of ~1 V are depicted in Fig. 6. As apparently exhibited that the gate leakage current (I_g) of the order $\sim 10^{-11}$ A and the drain current (I_d) $> 10^{-6}$ A at $V_{ds} = 1$ V for varying gate bias (V_{gs}) from -2 to 3 V. This

transistor action analogous to the conventional FETs evidently proves the higher performance of Al/ZrO_2/HfS_2/Al$_{\mu\text{-IDE}}$ structures. Table I indicates Al/ZrO_2/HfS_2/Al$_{\mu\text{-IDE}}$ 2-D FETs SS and mobility performance comparison with the state-of-the-art available reports 2-D TMD FETs. It manifestly confirms that the newly fabricated and demonstrated 2D$_{\text{ml}}$-Al/ZrO_2/HfS_2/Al$_{\mu\text{-IDE}}$ structure shows much improved electrical performance than other contestants of the same classification. The extracted enhanced electrical characteristics assuredly endorsed the high-quality ZrO_2/HfS_2/Al$_{\mu\text{-IDE}}$ interface of the demonstrated FET structures for beyond silicon technology.

IV. Conclusion

In a nutshell, the improved performance of the 2D$_{\text{ml}}$-Al/ZrO_2/HfS_2/Al$_{\mu\text{-IDE}}$ structures with ZrO_2 and HfS_2 as a gate dielectric and channel material is systematically investigated. The improved SS of ∼65 mV/dec, electron mobility of ∼74 cm^2/Vs, threshold voltage of ∼−1.72 V, and transconductance of ∼3.99 μS reveal high concord of 2D$_{\text{ml}}$-Al/ZrO_2/HfS_2/Al$_{\mu\text{-IDE}}$ for low-power FET applications. The ultralow OFF-state leakage current, low threshold voltage, steep SS, and low-voltage operating prove its potential for the next-generation low-power device applications.

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