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Unveiling Thermal Effects on Sn-Doped β-Ga_2O_3 Schottky Barrier Diodes on Sapphire for High-Temperature Power Electronics

Manoj K. Yadav, Arnab Mondal, Satinder K. Sharma, *Senior Member, IEEE*, and Ankush Bag, *Member, IEEE*

***Abstract*— The study investigates the performance of Schottky barrier diodes (SBDs) fabricated on high-quality Sn-doped β-gallium oxide (Ga_2O_3) film on sapphire (0006) substrate. Temperature-dependent performances are probed, in terms of forward and reverse bias characteristics. When temperature increases from 25 °C to 200 °C, the barrier height increases, and the ideality factor advances to unity. The current conduction happens differently at low and high temperatures because of the inhomogeneity in Schottky barrier height. Different methods are used to analyze temperature variations in the barrier heights. A high breakdown voltage of >200 V at 25 °C and a decent J_{ON}/J_{OFF} ratio for the all-temperature range are measured. The leakage current of the device does not significantly change with the temperature. These characteristics make the investigated Schottky diode structures on sapphire promising for future high-power electronics applications at elevated temperatures. Thus, cost-effective integration of Ga_2O_3 with non-native substrates is emphasized to enable rapid commercialization success.**

***Index Terms*— Gallium oxide (Ga_2O_3), low-pressure chemical vapor deposition (LPCVD), sapphire, Schottky barrier diode (SBD), Sn doping.**

I. Introduction

RECENTLY, β-gallium oxide (Ga_2O_3) has been considered as a promising wide-bandgap semiconductor material for the next-generation power electronics, owing to its superior material properties, such as ultrawide-bandgap of 4.5–4.9 eV [1] compared with GaN (3.4 eV) and SiC (3.2 eV), which enables a high theoretical breakdown field (E_c) of 8 MV/cm [2], [3], [4]. Consequently, β-Ga_2O_3 has a high Baliga's figure of merit (BFOM; defined as $\varepsilon\mu E_c^3$) of 3444 [5], [6], which is more than three times higher than that of GaN and SiC [7], endorsing its proficiency, particularly for power electronics.

In the last few years, most researchers have used Ga_2O_3 as a substrate to fabricate Ga_2O_3 Schottky barrier diodes (SBDs). However, due to the small wafer size and high cost of the Ga_2O_3 substrate, the sapphire substrate could be a potential candidate for the deposition of Ga_2O_3 film. Moreover, the poor thermal conductivity of Ga_2O_3 hinders its commercial use in a high-temperature regime leading to undesirable results [8], [9]. Indeed, the incorporation of a sapphire substrate in Ga_2O_3-based power devices offers significant advantages, particularly in terms of enhancing heat dissipation efficiency. The higher thermal conductivity of sapphire enables it to effectively dissipate the heat generated during device operation at elevated temperatures. Consequently, this improved heat dissipation capability contributes to the overall reliability and performance of Ga_2O_3-based power devices under high-temperature conditions.

The ultrawide-bandgap of Ga_2O_3 allows for smaller device dimensions, leading to reduced power consumption losses. Impressive studies on Ga_2O_3 SBDs, MOSFETs, and MESFETs have demonstrated high breakdown voltages and low ON-state resistances [2], [3], [10], [11], [13]. Limited studies have been conducted on Ga_2O_3 on sapphire substrates, with a focus on optoelectronic applications [14], [15], [16], [17], [18], [19], [20]. However, Hu et al. [21] have fabricated Ga_2O_3 nanomembrane on sapphire substrates for high-power applications, although the nanomembrane could be less promising for commercial applications considering scalability and reliability issues. Wang et al. [7] reported β-Ga_2O_3/TiN SBDs on heterogeneous integrated Ga_2O_3–Al_2O_3–Si substrate, studying their temperature-dependent electrical performance.

The next section describes the experimental details of device processing steps. Section III with results and discussions presents the material and electrical characteristics of the Ga_2O_3 SBD where the overall performance of SBD has been probed and evaluated in terms of high-power response in the temperature range of 25 °C–200 °C. The last section refers the conclusion of this work.

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Manoj K. Yadav is with the Institute of Sensor and Actuator Systems, TU Wien, 1040 Vienna, Austria (e-mail: manojyadav.iitmandi@gmail.com).

Arnab Mondal and Satinder K. Sharma are with the School of Computing and Electrical Engineering, IIT Mandi, Mandi 175005, India (e-mail: sunny.mondal2010@gmail.com; satinder@iitmandi.ac.in).

Ankush Bag is with the Department of Electronics and Electrical Engineering, IIT Guwahati, and Centre for Nanotechnology IIT Guwahati, Guwahati 781039, India (e-mail: bag.ankush@gmail.com).

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II. Experimental Detail

The Sn-doped β-Ga_2O_3 film was grown on c-plane sapphire substrate using the low-pressure chemical vapor deposition (LPCVD) technique. Before deposition, the sapphire wafer underwent cleaning with acetone and isopropyl alcohol for 5 min. Inside a quartz boat, 100 mg of Ga metal and 20 mg of Sn metal were positioned, while the substrate was placed on a separate quartz boat and loaded into the tube furnace. The substrate temperature was maintained at 1050 °C, and the base pressure and processing pressure of the furnace were 5×10^{-2} and 1 mbar, respectively. The thin-film deposition was carried out for 1 h. Material characteristics of the thin film have been carried out using X-ray diffraction (XRD), field-emission scanning electron microscope (FESEM), and atomic force microscopy (AFM). Doping concentration and mobility of samples have been determined using the Hall technique.

To fabricate lateral SBDs, Pt (60 nm) and Ti/Au (20/60 nm) layers were sputtered on the top of the Ga_2O_3 film to form the Schottky and ohmic contacts, respectively. The schematic of the fabricated device structure is illustrated in Fig. 1, with a distance of 418.30 μm between Pt and Ti/Au contacts. Electrical characteristics of the Pt/Ga_2O_3 SBD structures were investigated over a temperature range of 25 °C–200 °C, with measurements taken at interval of 25 °C using a Keithley 4200 semiconductor measuring unit. The temperature dependence study was performed using the LINKAM LTS420E heating stage.

III. Results and Discussion

In Fig. 2(a), XRD pattern of the sample confirms that a high crystalline quality Ga_2O_3 film with β phase was deposited on sapphire substrate. The dominant planes are (-201) of β-Ga_2O_3 and (0006) of sapphire. The (-402) and (-603) planes are fundamentally higher order diffraction of the (-201) plane. The peak at 21° is from the (0003) plane of the sapphire substrates. A peak around 37° has also been observed, which might be the (401) plane of Ga_2O_3 as given in JCPDS 01-076-0673, observed for all the samples. The full-width half-maxima (FWHM) of 0.0841° has been obtained using Voigt fitting of the (-201) plane, as shown in Fig. 2(b). The average crystallite size (D) is determined using the Scherrer formula. The measured value of D was ~95.78 nm. The small FWHM and large crystallite size signify the high crystalline quality of the film. Thereby, XRD results reveal the single-phase crystalline nature of the Ga_2O_3 film deposited on sapphire. A film thickness of 985 nm for the Sn-doped Ga_2O_3/Al_2O_3 sample is confirmed by cross-sectional FESEM, as shown in Fig. 2(c). A thicker layer can improve the overall surface flatness and reduce roughness. The interface roughness is an important factor in determining the performance of devices, especially in SBDs. The AFM technique was used to determine the topology of the film surface. A root-mean-square (rms) roughness of ~2 nm was measured, as shown in Fig. 2(d). Typical step-flow dominating surface morphology has been observed. The Sn-doped Ga_2O_3 film has net-doping concentration and mobility of 3×10^{17} cm^{-3} and 4 cm^2/V·s, respectively, measured at room temperature using the standard Hall method.

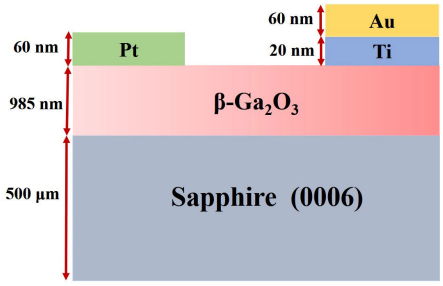

Fig. 1. Schematic (not in scale) of lateral Pt SBDs on Ga_2O_3 layer with the approximate dimensions of each layer.

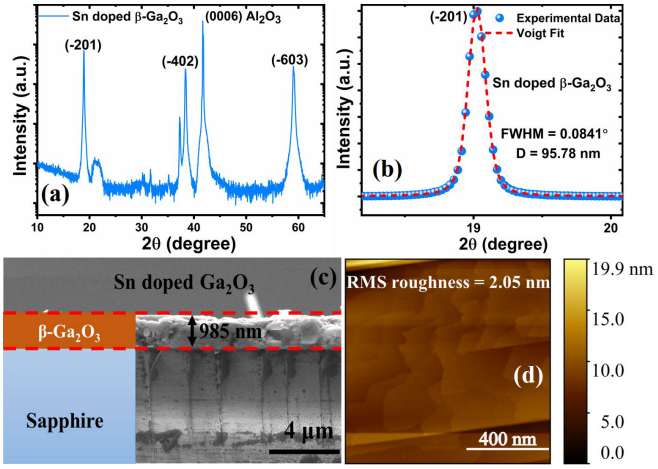

Fig. 2. (a) XRD pattern of the Ga_2O_3/Al_2O_3 sample. (b) XRD pattern to measure FWHM and crystallite size using (-201) plane of β-Ga_2O_3. (c) Cross-sectional FESEM image. (d) AFM image of the Ga_2O_3 surface.

Fig. 3(a) depicts temperature-dependent current density versus voltage (J–V) characteristics of Pt/Ga_2O_3 SBDs in both linear and semilogarithmic scale. At low forward bias, the J–V behavior is linear, as shown in Fig. 3(a). However, higher forward bias reveals deviation, likely due to significant effect of series resistance [22]. Typically, thermionic emission is the dominant current conduction mechanism at high temperatures [7]. Hence, the current density increases, as the temperature increases from 25 °C to 200 °C at the same forward bias [Fig. 3(a)]. The reverse bias nonsaturation behavior could stem from image force barrier lowering [23] and Schottky barrier height inhomogeneity [22], [24], [25]. The J–V characteristics based on the thermionic emission theory considering series resistance can be described by the following relation [26], [27]:

$$J = J_0\left[\exp\left(\frac{q(V - JAR_S)}{\eta kT}\right) - 1\right] \quad (1)$$

$$J_0 = A^*T^2 \exp\left(\frac{-q\phi_B}{kT}\right) \quad (2)$$

where J_0 is the saturation current density, η is the ideality factor, q is the free electron charge, k is Boltzmann's constant, A is the diode area, A^* is the Richardson constant, ϕ_B is the barrier height, R_S is the series resistance, and T is the temperature at which the device is operating. Here, image force barrier lowering could be neglected, because it is a weak function of applied voltage [25]. It is also observed that J_0 increases with an increase in temperature, and the

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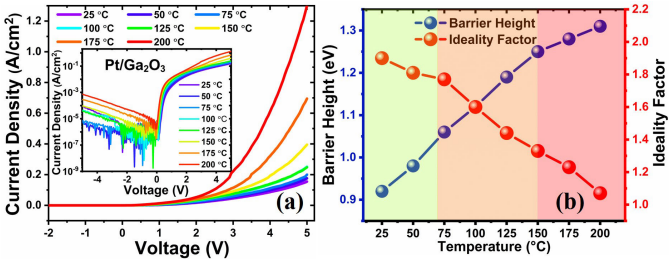

Fig. 3. (a) Linear and semilogarithmic scale J–V characteristics of Pt/Ga_2O_3 SBD in the temperature range of 25 °C–200 °C. (b) Temperature dependence of barrier height and ideality factor extracted from J–V characteristics of SBD. In the figure, yellow green, orange, and red colors indicate the mild-, moderate-, and high-temperature regions, respectively.

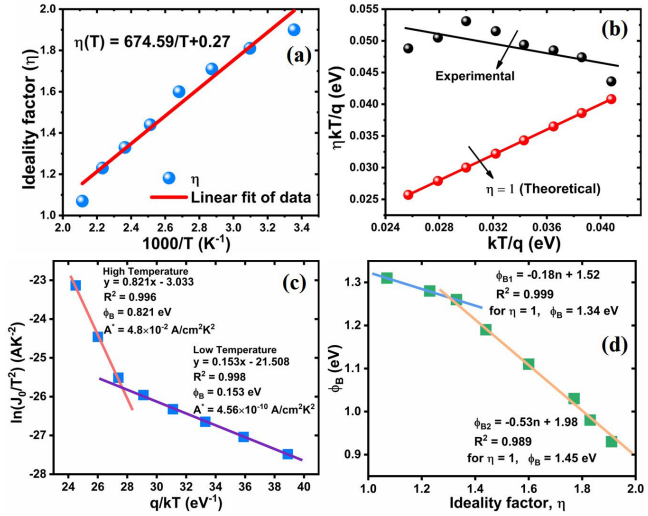

Fig. 4. (a) Plot of ideality factor versus 1000/T. (b) Plot of $\eta kT/q$ versus kT/q. (c) ln(J_0) versus q/kT plot. (d) ϕ_B versus η plot to verify the barrier height inhomogeneity in the lateral Pt/Ga_2O_3 SBD.

value of J_0 varies from 2.58×10^{-7} A/cm^2 (at 25 °C) to 2.01×10^{-5} A/cm^2 (at 200 °C). In the investigation of SBDs, the ideality factor is a crucial parameter measured using J–V characteristics. A desirable η value of 1.90 at 25 °C is obtained for SBD. Barrier height of the diode can be determined using (2). As temperature varies from 25 °C to 200 °C, ϕ_B increases from 0.92 to 1.31 eV, while η decreases from 1.90 to 1.07, as shown in Fig. 3(b). This temperature-dependent trend indicates a strong influence of temperature on ϕ_B and η. This behavior could be attributed to the unevenness of Schottky surface in SBDs [28]. The presence of barrier height inhomogeneity could result from the nonepitaxial deposition of Schottky contacts on the semiconductor surface, leading to a rough metal–semiconductor (MS) interface [29]. Another possible reason might be due to the difference in thermal expansion coefficients between the materials involved [30]. The other reasons for barrier inhomogeneity in the Schottky diodes could be vacancy-related defects, surface and bulk defects, and variation in the electric field at the MS interface due to dislocations [24], [31], [32]. Surface and bulk defects in Ga_2O_3 Schottky diodes introduce energy levels and affect charge carrier trapping and emission in a temperature-dependent manner. These defects can lead to temperature-sensitive inhomogeneities in the Schottky barrier height [33]. Dislocations in the Ga_2O_3 material can cause localized variations in the electric field at the MS interface. These dislocations can create regions with altered electrical properties, including changes in carrier concentration and mobility, which affect the electric field. These variations are temperature-sensitive and can result in inhomogeneities in device performance [34].

Theoretically, the MS interface should be flat and uniform according to thermionic emission theory. However, there is the existence of locally nonuniform regions having lower and higher barrier height patches on very small scales in an inhomogeneous Schottky barrier surface. This leads to uneven current conduction at the MS interface across different temperatures. At lower temperatures, conduction occurs through charge carriers crossing lower barrier height patches, while at higher temperatures, conduction involves charge carriers crossing relatively higher barrier patches. Consequently, current increases with rising temperatures. At 200 °C, η approaches unity, indicating a thermionic emission behavior. The ϕ_B value (1.31 eV) at this temperature aligns closely with the theoretical barrier height of Pt/Ga_2O_3 diodes.

The variation in ideality factor with temperature was found to change in linearity with temperature, as shown in Fig. 4(a)

$$\eta(T) = n_k + \frac{T_k}{T} \tag{3}$$

where n_k and T_k are constant having the values of 0.27 and 674.59 K, respectively. The high value of ideality factor at lower temperatures may be attributed to the existence of image force lowering, barrier inhomogeneity at the MS interface, and interface states [22], [24], [25], [29], [35].

Furthermore, the temperature-dependent ideality factor was further investigated to explain the primary transport mechanisms by plotting $\eta kT/q$ versus kT/q. The plot of $\eta kT/q$ versus kT/q is shown in Fig. 4(b), which illustrates the theoretical along with the experimental results in the plot. It is clear that there is a relationship between the theoretical and experimental curves of the SBD. In this plot, the straight line fit to the experimental values should be parallel to the line of theoretical values [36]. However, as shown in Fig. 4(b), the straight line fit to the experimental data is not parallel to the theoretical data line. Thus, the fabricated SBD does not follow the ideal Schottky diode behavior.

In order to further investigate the barrier height inhomogeneity, a robust and extensively validated technique has been used—the Richardson plot of saturation current density [36]. Equation (2) of reverse saturation current density can be expressed as follows:

$$\ln\left(\frac{J_0}{T^2}\right) = \ln(A^*) - \frac{q\phi_B}{kT}. \tag{4}$$

The Richardson plot of ln(J_0) versus q/kT has two different linear regions with different slopes and intercepts, as shown in Fig. 4(c). This type of behavior of the Richardson plot is attributed to the inhomogeneous Schottky barrier heights [37]. In the first region, at high temperatures, the values of Richardson constant (A^*) and activation energy ($E_a = \phi_B$) were extracted from the intercept and slope of the straight line

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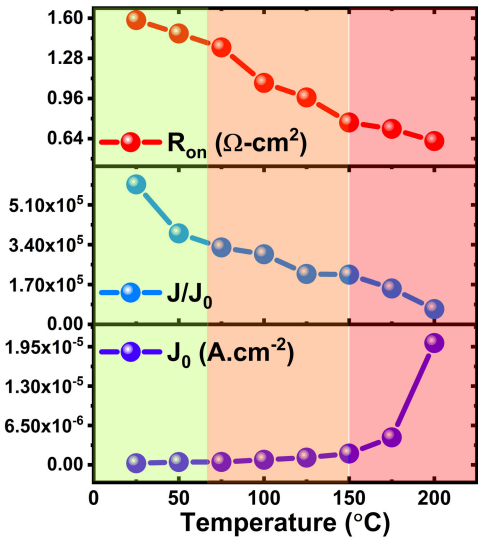

Fig. 5. Variation of J_0, (J/J_0), and R_{ON} with the temperature increases from 25 °C to 200 °C. In the figure, yellow green, orange, and red colors indicate the mild-, moderate-, and high-temperature regions, respectively.

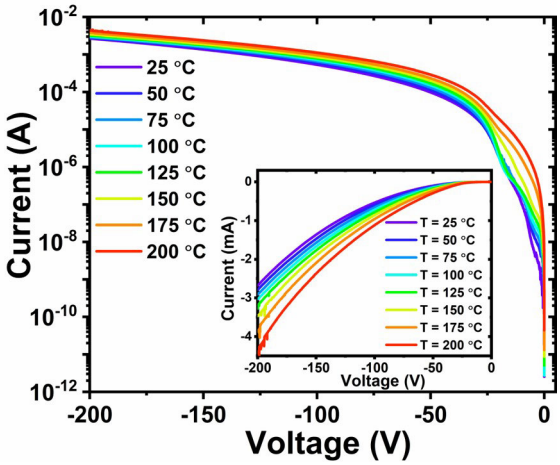

Fig. 6. Semilogarithmic and linear scale reverse *I–V* characteristics in the temperature range of 25 °C–200 °C.

as 4.8×10^{-2} A/cm^{2}K^2 and 0.821 eV, respectively, Whereas, in the second region, at low temperatures, the values of A^* and E_a were found to be 4.56×10^{-10} A/cm^{2}K^2 and 0.153 eV, respectively. The A^* notably differs from Ga_2O_3 theoretical value (41.1 A/cm^{2}K^2), implying a shift from thermionic emission theory, possibly toward thermionic field emission. The $\ln(J_0)$ versus q/kT plot underscores distinct barrier heights and Richardson constants, pinpointing inhomogeneous barrier heights at the Schottky interface. This gives rise to elevated ideality factors at lower temperatures [24], [36]. Furthermore, this investigation is supporting the previous observation on barrier height inhomogeneity.

To corroborate the effectiveness of the previously employed methodologies for evaluating barrier height inhomogeneity within Schottky diodes, an additional investigation was conducted. This technique enhances our technical understanding and rigorously validates our assessment of the diode's barrier height variations. Fig. 4(d) shows the plot of temperature-dependent barrier height versus ideality factor. It reveals two distinct barrier heights and a linear correlation between barrier height and ideality factor. Extrapolation at $\eta = 1$ yields 1.34 eV in one region and 1.45 eV in another, highlighting barrier height inconsistency at the MS junction. High values ideality factor at low temperatures are attributed to this barrier height inhomogeneity, consistent with findings by Schmitsdorf et al. [38], who linked it to lateral inhomogeneities in the barrier heights. Thus, the high ideality factor at low temperatures primarily results from this barrier height inhomogeneity.

The variations in J_0, (J/J_0), and R_{ON} with the temperature are shown in Fig. 5. The specific ON-state resistance (R_{ON}) decreases from 1.585 Ω·cm^2 (at 25 °C) to 0.621 Ω·cm^2 (at 200 °C) for the Pt/Ga_2O_3, which has been measured from the slope of the fitting line to the temperature-dependent $J–V$ characteristics. Poor mobility may be the reason for this relatively high R_{ON}. The current density ON/OFF ratio (J_{ON}/J_{OFF}) decreases, as the temperature increases from $T = 25$ °C to 200 °C. However, the lateral SBD has a decent J_{ON}/J_{OFF} ratio even at a high temperature of 200 °C.

Fig. 6 shows the reverse current–voltage ($I–V$) characteristics of the lateral Ga_2O_3 SBD across the temperature range of 25 °C–200 °C. Notably, no breakdown of the device is observed up to 200 V. Given the instrument's operational limits, we cannot surpass this voltage, implying that the device breakdown voltage exceeds the recorded value. The current values at −200 V are ∼2.8×10^{-3} to ∼4.8×10^{-3} A for the $T = 25$ °C–200 °C, respectively. It is observed that there is no significant difference in the current value at a high reverse voltage (200 V) across various temperatures. The temperature effect is more prominent at low reverse voltages where thermal energy plays a significant role, while at high reverse voltages, field emission becomes the dominant mechanism, reducing the impact of temperature on leakage current [39]. This suggests that higher temperature does not notably affect leakage current of the lateral device.

Table I presents a comprehensive comparison between the previously reported lateral and vertical β-Ga_2O_3 device structures fabricated on sapphire substrates and the current research findings. While there are limited published reports available regarding β-Ga_2O_3 SBDs fabricated on sapphire substrates, it is noteworthy that the growth of the epilayer has been performed using various methods, resulting in distinct epilayer structures. These discrepancies in growth techniques and epilayer structures necessitate a careful examination and comparison in order to ascertain the impact of these variations on the overall device performance and characteristics.

Among the assortment of cited works detailed in Table I, our study presents a unique opportunity to conduct a highly precise and comprehensive comparison with the research conducted by Sood et al. [40]. This is primarily attributed to the remarkable similarity observed in terms of both epilayer and device structures. However, it is important to acknowledge that divergences exist in the growth method and doping material employed. Sood et al. [40] have reported Si-doped β-Ga_2O_3 lateral SBDs in the year of 2023. In their study, they deposited Si-doped β-Ga_2O_3 thin film onto a sapphire substrate using a metal–organic chemical vapor deposition

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TABLE I
VARIOUS REPORTED β-Ga_2O_3 DEVICE STRUCTURES ON SAPPHIRE SUBSTRATES AS COMPARED WITH THIS WORK

Device Structure	Epilayer Structure	Growth Method	Doping	Epilayer Thickness	η	ϕ_B (eV)	R_{on} (Ω-cm^2)	V_{BR} (V)	References
L-SBDs	Thin film	LPCVD	Sn-doped	985 nm	1.07	1.31	0.62	$>$ 200	This work
L-SBDs	Thin film	MOCVD	Si-doped	210 nm	1.97	0.54	0.81	370	[40]
L-MISD	Thin film	MOCVD	Si-doped	210 nm	1.61	-	1.92	309	[41]
MOSFET	Thin film	MOCVD	Si-doped	150 nm	-	-	-	360	[42]
MOSFET	Thin film	MOCVD	Si-doped	150 nm	-	-	-	400	[43]
V-SBDs	Flakes	Exfoliation	-	10 μm	1.17	1.30	0.005	172	[44]
L-SBDs	Nano-membrane	Exfoliation	Sn-doped	400 nm	-	-	.05	1700	[21]
MOSFET	Nano-membrane	Exfoliation	-	190 nm	-	-	0.0074	800	[45]

(MOCVD) technique. Their experimental results revealed a V_{BR} of 370 V, an R_{ON} of 0.81 Ω·cm^2, an η of 1.97, and a ϕ_B of 0.54 eV for the lateral SBDs.

Present work demonstrates superior device performance characteristics, specifically a lower R_{ON} and η, indicating improved conductivity and more efficient charge transport. In addition, our research reveals a higher barrier height, indicating enhanced energy barrier for carrier injection and reduced leakage current. Moreover, our estimations indicate that the V_{BR} is much greater than 200 V because of low leakage current. Furthermore, our devices exhibit stable dc responses even under high-temperature conditions.

Thus, this study focuses on the growth of Sn-doped β-Ga_2O_3 thin films on sapphire substrates using the LPCVD technique. The fabricated SBDs exhibited commendable performance, particularly in high-temperature and high-power applications. Moreover, the enhancement of device performance for high-power applications can be achieved through the utilization of diverse device structures. However, it should be noted that these alternate structures require meticulous consideration and evaluation to ensure their compatibility and effectiveness in meeting the desired power requirements.

IV. CONCLUSION

In this study, Sn-doped β-Ga_2O_3 SBDs were fabricated on sapphire using LPCVD. Pt/Ga_2O_3 devices were characterized from 25 °C to 200 °C. The SBD exhibited excellent static and dynamic characteristics, including low saturation current density, low ideality factor, high barrier height, and good J_{ON}/J_{OFF} ratio. As temperature increased, the barrier height rose, and ideality factor decreased. The ideality factor reaching close to unity at 200 °C and barrier height approaching the theoretical value. The current conduction mechanism changed with temperature due to the inhomogeneous barrier heights. This inhomogeneity in barrier height led to significantly high ideality factors at low temperatures, as evident from the results of various plots. SBD had >200 breakdown voltage, consistent leakage current across temperatures. The stable performance at high temperatures may be attributed to the higher thermal conductivity of the sapphire substrate compared with Ga_2O_3. Thus, this fabricated Sn-doped β-Ga_2O_3 SBD on sapphire demonstrates great potential for high-power and high-temperature applications.

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