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Spiral WSe_2 with Interlayer Twist for Memristive and Neuromorphic Device Applications

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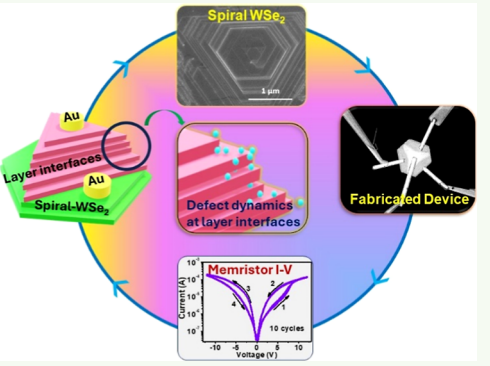
ABSTRACT: Two-dimensional transition metal dichalcogenide (2D-TMDC) layered materials have shown great potential in emerging memristor technologies for neuromorphic computing applications. Often, most of the stoichiometric TMDC materials do not show any memristor hysteresis, and modulation of structural defects and compositional variations are much needed to promote the memristor characteristics. Herein, we investigate a multilayer WSe_2 with spiral topology and twisted interface for memristor switching device applications. We explore a twisted multilayered WSe_2 memristor device and its potential application as a synaptic candidate for neuromorphic computing applications. The fabricated device reports cyclic stability over 200 cycles and data retention of 10^3 s. We also discuss the conduction mechanism using edge and terrace defects across the interfaces of the twisted layers. These results provide a wide range of possibilities for improving the memristor switching behavior and will help us utilize twisted flakes for emerging neuromorphic device applications.



KEYWORDS: *memristor, twisted 2D materials, chemical vapor deposition, point defect, neuromorphic devices*

INTRODUCTION

Layered two-dimensional transition metal dichalcogenides (2D-TMDCs) remain the most interesting and emerging material in the field of neuromorphic computing applications.[1−4] For example, 2D memristive devices can offer scaling, integration with standard complementary metal oxide semiconductor technology, and nonvolatile memory capabilities and show a greater potential to overcome the bottleneck of conventional Von-Neumann computing architecture.[1,5−9] Typically, in memristor devices, the memristive switching originates from the generation, recombination, and destruction of defects at nanoscale.[10] Structural defects such as vacancies and grain boundaries in 2D-TMDCs play a crucial role in memristive switching.[11−14] Recently, 2D materials constructed out of one or more layers have occupied the center of attraction due to the consequent changes associated with the electronic structure. The ab initio band structure calculations clearly show that high-symmetry stacking of the TMDC layers results in weak interlayer couplings and changes in electronic structure.[15] However, twisted and stacked TMDC layers have been found to exhibit new quantum observations such as superconductivity with vanishing electrical resistance, tunable Mott insulators, and moiré excitons.[16] Twisted spiral structures of TMDCs are induced by screw-dislocation-driven growth.[17] During chemical vapor deposition (CVD) growth, the incorporation of threading dislocation acts as a driving force to break the symmetry. The devices on the 2D layered structures have been realized by lateral geometry, as well as vertical geometry. In the lateral structures, the memory window is observed to open at a relatively large voltage for gaps of several micrometers between the two electrodes.[18] It will be interesting to fabricate a planar memristor with such a twisted spiral structure to investigate the memristor performance and establish some insights into the conduction mechanism. In particular, such twisted layers may accommodate a large number of defects and twist boundaries and can help in reducing switching voltages for low-power memristor applications.

Here, we report the planar multilayer WSe_2 memristor device, with a spiral structured WSe_2 as active channel and inert Ti/Au as top electrodes, one lying on top of the spiral surface and the other at the bottom of the spiral structure. The observed memristor behavior is likely due to formation and annihilation of selenium point defects across the spiral layer interfaces and associated electron hopping between the layers. Memristor response reveals superior electrical conduction and repeatable hysteresis in $I-V$ curves over a period of around 200 cycles and a data retention of 1×10^3 seconds. This work could open wide opportunities in using twisted, layered

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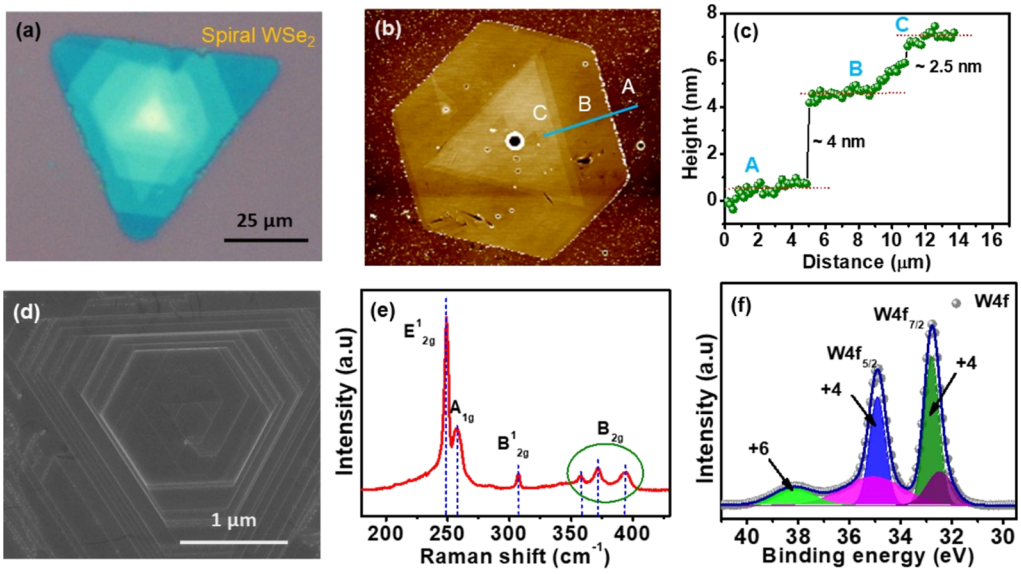

Figure 1. Microscopy and spectroscopy analysis of spiral WSe_2 layers. (a) Optical microscopy image of twisted flake with hexagonal and triangle twisted layers. (b) AFM surface image. (c) Height profile line scan plot. (d) FE-SEM image of twisted flake showing the dense stacking of WSe_2 layer with truncated triangular to hexagonal morphology. (e) Raman spectrum with observed E_{2g}^1, A_{1g}, and B_{2g} modes. (f) XPS data of W 4f showing the primary +4 oxidation state of WSe_2 with minor presence of +6 state.

materials application in the area of neuromorphic electronics and computing hardware.

EXPERIMENTAL SECTION

WSe_2 multilayers with a spiral topology were grown on Si/SiO_2 substrate by the CVD technique at atmospheric conditions. Briefly, 100 mg of WO_3 (99.9%, Sigma-Aldrich) and 10 mg of NaCl (99.9%, NaCl) powder precursors were mixed well and placed in an alumina boat, and the boat was kept inside a 1 in. diameter quartz tube. Another alumina boat was used for selenium precursor of 100 mg powder toward upstream direction of carrier gas at ~250 °C. The distance between two precursors were maintained such that they maintain their respective temperatures for reaction. A mixture of Ar + H_2 (95% + 5%) was used as the carrier gas and is supplied continuously throughout the reaction. A precleaned Si/SiO_2 (285 nm) substrate was placed on an alumina boat with face down. Ramp rate was maintained 50 °C/min and after growth natural cooling was allowed. Twisted WSe_2 was characterized by scanning electron microscopy (SEM), atomic force microscopy (AFM), Kelvin probe force microscopy (KPFM), and X-ray photoelectron spectroscopy (XPS).

Device Fabrication and Characterization. The flakes have been inspected in the optical microscope, and their location has been noted down. Thereafter, the electrodes' patterns with a channel length of 20 μm (width ~50 μm) were patterned on a WSe_2 multilayer flake by spin-coating a positive photoresist (950 K PMMA-A2/EL-9). The targeted flake patterning is accomplished by EBL tool (Raith e-line) after the write field correction and alignment of the beam using 3-point coordinates' correction with the prefabricated metal alignment marks on the wafer. The targeted flake electrode area has been further approached using local coordinates' alignment.[19] The electrodes have been patterned in PMMA/EL-9 with a highly collimated e-beam accelerated at 18 keV and 10 μm aperture, 6 mm working distance, at dose of 80 $\mu C/cm^2$. Furthermore, 3 nm Ti (adhesion layer) and 40 nm Au metals have been deposited by DC magnetron sputtering. After that extra metal was lifted off in the NMP solvent at 70 °C. The memristor electrical measurements were performed using a Keysight source measure unit (SMU)- B2902A model.

RESULTS AND DISCUSSION

Figure 1a reveals the morphological information on twisted WSe_2 layers, showing a large number of layers with triangle and hexagonal shapes. Optical contrast in monolayer and multilayer TMDCs is sensitive to thickness, and thickness differences enable the visible optical contrast from the WSe_2 flake. The topographic image of twisted WSe_2 with step-like repeated edges was captured using an AFM imaging as shown in Figure 1b. The line profile drawn between points A and C is shown in Figure 1c, indicating that initially the flat base layer has a thickness of ~4 nm, and then, on top of the flat base layer twisted layers started growing, and the thickness of top layers becomes incremental in steps. The high-magnification SEM image in Figure 1d shows a flat triangle base following the hexagonal layers on top. The representative microscopy images show more complex features that support the twisted layered growth. It is known that the introduction of new screw dislocations results in the complex stacking and morphology transition from triangular to hexagonal and vice versa.[17,20,21] Raman spectroscopy is a sensitive and nondestructive technique to study the twisted layers, since interlayer shearing and breathing modes of layered materials are sensitive to interlayer coupling. Figure 1e shows the spectrum with Raman active modes at 249.05 cm^{-1} (E_{2g}^1), 256.7 cm^{-1} (A_{1g}), 307.4 cm^{-1} (B_{2g}^1), and between 358 and 393 cm^{-1} (B_{2g}), where E_{2g}^1 and A_{1g} are the in-plane and out-of-plane vibrational modes having W−Se atoms and Se−Se atoms vibrating against each other, respectively. However, all the B_{2g} modes arise due to interlayer interactions in out-of-plane mode, having W and Se atoms vibrating against each other with 180° phase difference with reference to the vibration of adjacent layer.[22] It has also been observed in previous reports that the vibrational modes around 358−393 cm^{-1} are correlated with the evolution of moiré superlattice in twisted WSe_2 layered material.[17,23] In the presented Raman spectrum, the modes (encircled region with the green color) can be corroborated with moiré superlattice.[22]

The surface composition of twisted WSe_2 layers was investigated using XPS analysis. Figure 1f shows the core

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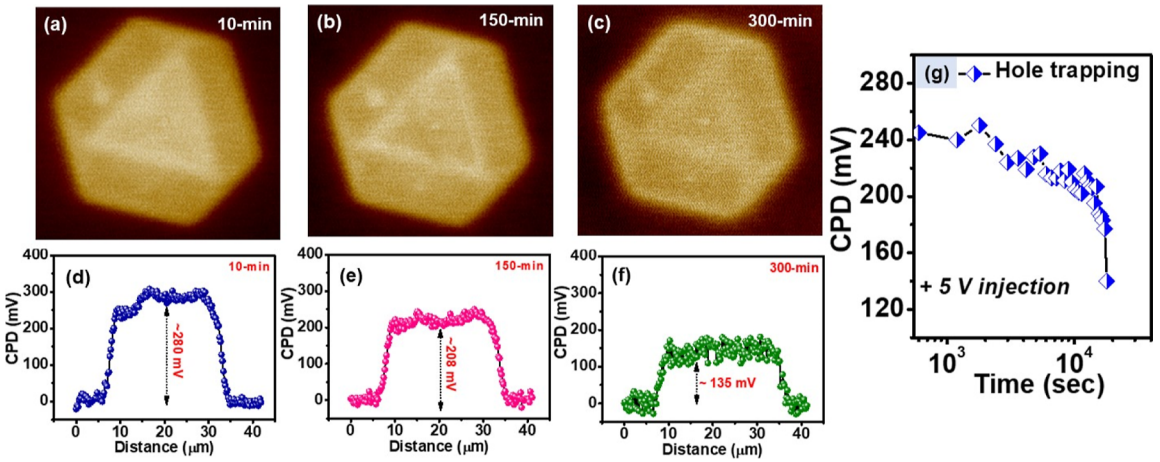

Figure 2. KPFM measurements of the spiral WSe_2 flake. (a−c) KPFM surface images were taken after different intervals of time from initial (0 min) to 300 min. Here, the tip bias is +5 V. (d−f) Contact surface potential difference plot for various timings. (g) Potential drop over a period of time.

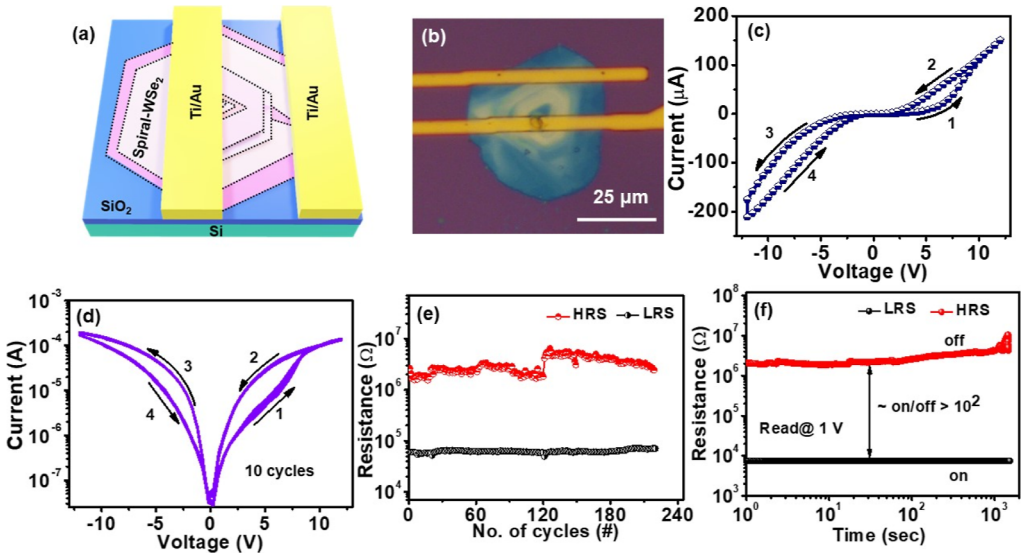

Figure 3. Performance characteristics of the WSe_2 memristor device. (a) Schematic of the device. (b) Optical image of the fabricated device with Ti/Au electrodes. (c) *I*−*V* hysteresis plotted in a linear graph. (d) *I*−*V* hysteresis with current in a logarithmic coordinate and voltage in a linear coordinate. (e) Endurance of the memristor device. (f) Retention characteristics of the memristor.

level high-resolution XPS spectra of W 4f of WSe_2 with doublets at 32.78 and 34.88 eV. These doublets correspond to the $4f_{7/2}$ and $4f_{5/2}$ lines of the W^{4+} oxidation state of pristine WSe_2 layers. The observed additional peak at 38.08 eV is assigned to the W^{6+} oxidation state of WSe_2 with surface oxidation or edge-terminated oxides of interlayers. For all XPS analyses, adventitious carbon C 1s is considered at 284.8 eV, and binding energies for other core level peaks were adjusted. Supporting Information, Figure S1a shows the survey spectrum, and Figure S1b,c shows the C 1s and O 1s core level spectra of carbon and oxygen, respectively. Figure S1d shows the Se 3d core level spectrum having a doublet at 55.06 ($3d_{5/2}$) and 55.84 eV ($3d_{3/2}$).

A noncontact mode KPFM technique was employed to investigate the quality of the semiconductor and simultaneously unveil the topographic information on spiral structures and their defects at a nanoscale level in layered WSe_2. This technique enables the direct measurement of both surface potential and work functions, providing valuable insights into the charge trapping and detrapping behavior within the material. Choudhary et al. demonstrated the application of KPFM for analyzing the quality of oxide and semiconductor interfaces through charge trapping studies.[24] Building on their work, we utilized KPFM to investigate the time-dependent decay of the contact potential difference (CPD) in spiral WSe_2. The CPD values were measured after every 10 min interval over a longer period of time (up to ∼5 h.). All the KPFM measurements were carried out at +5 V injection. Figure 2a−c shows the surface potential images of a flake at different time intervals: 10, 150, and 300 min, respectively. The CPD spectra from the full flake area are shown in Figure 2d−f. Figure 2g shows the decay of the CPD values, which is proportional to the decay in trap charges over time. The observed CPD values initially after 10 min show +280 mV, and after 300 min, it drops down to +130 mV; this initial high CPD values signify the high density of holes trapping.[25] From the recorded images, it is also clearly visible that there is a change in the brightness of the flake. The center of the WSe_2 flake (triangular

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edges) with a greater number of layers shows higher brightness than that of the outer surface with a low number of layers. From topographic images, it is evident that with increase in number of layers, the CPD value increases, which is consistent with the literature.[26−29] As previously reported for MoS_2 and layered graphene, the observed spread of surface potentials across the entire 2D flake could be due to uneven distribution of charge carriers attributable to its 2D nature, trapped charges, or environmental adsorbates.[30,31] The irregular distribution of surface potentials observed in the CPD maxima depicted in Figure 2d−f may suggest the presence of chalcogen defects, the influence of grain boundaries, and imperfections within the layered structure.[32]

Lateral geometry-based two-terminal memristor devices were fabricated on the twisted WSe_2 flake with Ti/Au as electrodes on a Si/SiO_2 substrate, as shown in Figure 3a schematic. The actual fabricated device optical microscope image is shown in Figure 3b. Initially, before forming the process with low voltages, no memristive switching was observed. Once the voltage reaches an SET or forming voltage, the device starts switching from the initial high resistance state (HRS) to the final low resistance state (LRS). The typical bipolar memristive switching in linear and semilogarithmic scale is shown in Figure 3c,d, respectively. The direction of the current flow was marked with arrow numbers. In this memristive switching, during forward and reverse scanning, the current flow is a gradual process unlike abrupt in threshold switching memristors, and the current flow depends on the applied field. From Figure 3c, it is difficult to precisely pinpoint the threshold voltage value directly, and hence, we have extrapolated toward positive voltage and negative voltages, and their intersecting points were assumed as starting points of forming and rupturing processes. The forming process starts at about +6 V during forward bias, and at +12 V, it fully turns from HRS to LRS, and this process is called SET. During reverse bias, the memristor switches back to its virgin state, i.e., HRS from LRS at −12 V; this process is termed as RESET. This basic $I-V$ pinched hysteresis showed that twisted WSe_2 layers generate nonvolatile memristive switching in a planar device with a channel length of 10 μm. To check cycle-to-cycle variation, large number of $I-V$ cyclic loops were performed, which was termed an endurance test. Figure 3d shows the endurance for the first 10 cycles. During the endurance test, the device showed almost a constant LRS but a small deviation in HRS with an ON/OFF ratio of ∼40, as shown in Figure 3e. The constant SET/RESET operation of $I-V$ cyclic loops can result in the development of defects, which is one of the potential causes of HRS deviation during the endurance test. The memristor data retention characteristics were carried out as shown in Figure 3f at a read voltage of 1 V. The memristor device shows stable retention up to 10^3 seconds, and the ON/OFF ratio of LRS/HRS is $>10^2$.

In spite of extensive experimental work, the precise mechanisms responsible for switching in 2D-TMDC) materials across various device configurations remain poorly understood. In general, the most dominant switching process is governed by the generation and annihilation of chalcogen vacancies in the 2D-TMDCs. These vacancies or point defects migrate under the influence of an applied electric field. Recent studies have shown that sulfur vacancies and antisites substitutions (S replaced by Mo) are the most commonly occurring point defects in MoS_2. Specifically, in lateral monolayer MoS_2 devices, sulfur vacancies have been observed to drift along grain boundaries within the conducting channel.[33] These vacancies can act as n-type dopants, altering the bulk conductivity and modifying the potential energy barrier at the semiconductor−metal interfaces. Moreover, point defects can also introduce additional electronic states. While trap-state-based hysteresis is commonly accepted as the main explanation for resistive switching in lateral devices, recent research suggests that the drift of charged point defects may also play a significant role, potentially even dominating the hysteresis in certain scenarios. Ab initio investigations have revealed varying activation energies for the diffusion of sulfur vacancies in MoS_2, with a notable dependence on the spatial arrangement of the point defects. It is anticipated that this energy barrier would be lowered along grain boundaries or interfaces.[34] Spetzler et al. discuss the importance of vacancies in TMDC devices and provide insights into the switching mechanisms of memristor devices. Their analysis encompasses the origin of hysteresis, the impact of vacancy dynamics, and the lowering of the charge-induced Schottky barrier in lateral memristive devices. Experimental and simulation studies conducted by Spetzler et al. suggest that the observed hysteresis in current−voltage ($I-V$) curves, both with and without significant Schottky barriers, is driven by the dynamics of mobile charged vacancies. Specifically, the formation and annihilation of a vacancy depletion region locally reduce the conductivity, ultimately limiting device conductivity. The dynamics of the depletion region formation and annihilation are influenced by operating frequency, vacancy mobility, and the asymmetry of contact potentials. These parameters critically determine the direction and symmetry of hysteresis in the $I-V$ curve.[35] Bisht et al. also reported on how electrical bias in one junction affects neighboring junctions due to graded point defects and their distribution in the inhomogeneous medium of hydrogen-doped nickelate films.[36]

Raman, XPS, and KPFM investigations demonstrate the underlying nonhomogeneity and point defects (selenium vacancies) in WSe_2. Our memristor design, having one electrode atop a multilayer spiral stack and another on a flat layer, allows for a multitude of places for point defects across interfaces. Compared to monolayer structures, the multilayer, in particular, the spiral architecture, facilitates many vacancy sites at the interfaces and boundaries. We also made patterns on different flakes to take advantage of studying variations within the flake by having electrodes with different channel lengths and electrodes at different locations. The device which is shown in the zoomed area of Figure S2a indicates the electrodes with, namely, A, B, C, and D. All the electrodes are chosen such that one electrode lies on top of the spiral layer, and rest all are on a flat bottom layer. It was observed that as shown in Figure S2b−g, all the devices are giving memristor response; however, their behaviors are different in terms of symmetry, on-state currents, and switching directions. This clearly suggests that the variation in layer number, twist angle, and defect distributions at interface boundaries affects the conduction behavior. In addition, we found nonmonotonous resistance variation with respect to the channel length in WSe_2 devices. It is known from the literature that as the channel length decreases, the resistance also decreases, and vice versa. Contrary to this expectation, our study observed a nonlinear trend in resistance with varying channel lengths, as shown in Figure S3a−c. This nonlinear trend implies that the spirality or twist angle effect plays a critical role in the overall conduction of the spiral flake. The above observations clearly indicate the

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role of interlayer hopping and the twist angle effect in the transport properties of spirally grown WSe_2 multilayers. Also, unlike unipolar n-type MoS_2 (due to sulfur vacancies), multilayer WSe_2 shows an ambipolar transport behavior with an indirect band gap of ~1.38 eV.[37] Consistent with literature, the energy band diagram drawn between Au and WSe_2 shows a theoretical Schottky barrier of 0.55 eV.[38] The details of the energy band diagram are provided in Figure S4. We believe that the conductivity change in memristor switching is attributed to the dynamics of point defects across the interfaces and the associated hopping of charge carriers. Further investigation is necessary to identify the dominant conduction mechanism in this unique memristor architecture. Employing complementary techniques, such as temperature-dependent conductivity measurements and advanced spectroscopic analysis, will shed light on the precise charge transport pathways and optimize this novel memristor design.

Our planar twisted WSe_2 memristor device was tested for an artificial synapse for neuromorphic computing applications. Sequential voltage pulses are applied to the two terminals of the device as presynaptic input while continuously recording output current as postsynaptic current (PSC). The schematic of the biological synapse is shown in Figure 4a. The pulse

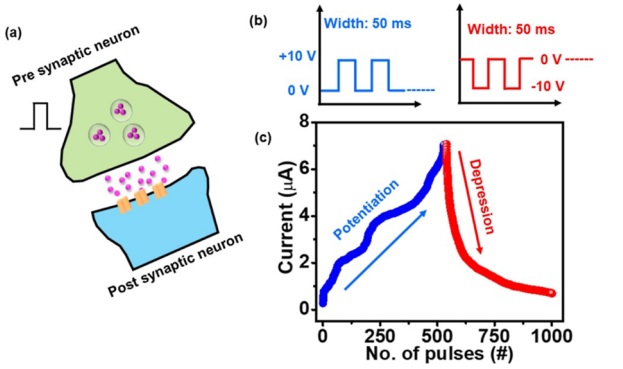

Figure 4. Synaptic measurements of the twisted WSe_2 memristor. (a) Actual biological synapse schematic. (b) Pulse scheme schematic. (c) Change in synapse conductance as a function of pulse voltage with an amplitude of +10 and −10 V. Synaptic characteristics showing long term potentiation (LTP) and long term depression (LTD) over 1000 pulses.

scheme applied is shown in Figure 4b. The potentiation and depression are demonstrated in Figure 4c. A positive and negative voltage pulse sequence of +10 and −10 V is applied with a pulse width of 50 ms, which induces an exponential increase in PSC and an exponential decrease in PSC, respectively.

CONCLUSIONS

This work demonstrates the fabrication and characterization of a two-terminal memristive device based on a novel spiral WSe_2 architecture. While prior studies have explored multilayered memristive systems, our design uniquely incorporates specific electrode placements to probe the influence of grain boundaries and carrier transport mechanisms. The fabricated spiral WSe_2 device exhibits significant current modulation, suggesting an underlying memristive behavior. Notably, the observed high current levels within a layered structure incorporating inert electrodes point toward the potential contribution of grain boundaries and the impeded transport of carriers across the spiral geometry. Further investigations are necessary to elucidate the precise conduction mechanism responsible for the observed memristive behavior. Furthermore, the promising results obtained in this study highlight the potential of spiral WSe_2 as a promising candidate for synaptic devices in neuromorphic computing applications.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.3c01810.

XPS survey spectra; C 1s, O 1s, and Se 3d spectrum; memristor characteristics; channel length effects; and energy band diagram (PDF)

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Author Contributions

B.R.N. performed all the experimental analyses and characterization and prepared the original manuscript. S.C. performed electron beam lithography for device fabrication. S.K.S. provided critical comments, and V.B. coordinated the entire work. All authors have contributed equally in writing the manuscript.

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Notes

The authors declare no competing financial interest.

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