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Application of high-k dielectric stacks charge trapping for CMOS technology

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ABSTRACT

The effect of constant negative voltage stress on charge trapping and interface states of Al/HfO_2/SiO_xN_y/Si structures are investigated. The reduction in the capacitance of *C–t* characteristics and a significant shift in *C–V* curves towards negative voltage axis reveal that the charge trapping/detrapping occurs at the Si/SiO_xN_y/HfO_2 interface and HfO_2 bulk. However, there is a relative increase in gate leakage current as a function of the voltage stress and time, owing to the trap-assisted tunnelling. It is suggested that these traps are probably Hf–OH neutral centers, originating from the breaking of bridging Si–OH and Si–NH bonds by mobile H^+ protons. This has potential application in non-volatile CMOS memory devices.

1. Introduction

The scaling of ICs can be defined as the process of reducing the size of both active and passive devices in order to improve the packing density on a chip so it performs more functions with faster speed and at lower power consumption [1]. With the continuous scaling of CMOS memory devices, charge retention, sub-threshold voltage, threshold voltage instability, gate leakage current, etc. have started dominating and are expected to increase with the technology scaling. Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from substrate to gate [2–5]. Therefore, to sustain the benefits of scaling with acceptable power consumption and reliability for the non-volatile semiconductor memory, there is a need to understand these new phenomenon like sub-threshold leakage, threshold roll off, charging/discharging, velocity saturation, gate leakage current, tunneling current, etc. and remedial steps to be undertaken [6,7]. Significant efforts have recently been dedicated to the investigation of high-k based non-volatile memory systems. Key issues like charge trapping, specially at bulk and interface possess a serious threat to long term operation of non-volatile semiconductor memory devices. Therefore, the innovative solution, such as the introduction of high-k materials and charge trapping layers into the gate dielectric stack will probably overcome this bottleneck in the scaling nodes [8]. Currently, high-k materials such as HfO_2, ZrO_2 and Y_2O_2 are being intensively investigated as a replacement for SiO_2 gate insulator [9,10]. High-k stack dielectric must have reproducible and controllable characteristics during whole CMOS processing, in terms of longer charge retention time, thermal stability and electronic properties [11]. Introduction of high-k materials cause high drive current, crystallization at lower temperatures, severe carrier mobility degradation, etc. Degradation of mobility attributed to scattering caused by phonon modes is inherent in high-k materials, including hafnium-based dielectric films [12–14]. To eliminate this, a thin oxynitride interface layer must be maintained between the silicon and high-k material. This extends the optimized oxynitride–silicon interface that provides the excellent voltage stability, carrier mobility, interface stability and device reliability required in advanced transistors for the future non-volatile memory devices [13,15]. Charge retention time can be improved by intentionally generated traps under constant voltage stress. In this work, the constant negative voltage stress-induced trapping/detrapping of HfO_2/SiO_xN_y gate stacks is investigated and seen that charge retention can be enhanced under constant voltage stress.

2. Experimental

RCA cleaned p-type silicon wafers of ⟨1 0 0⟩ and 1–10 Ω-cm were used for MIS structures fabrication. After drying in the nitrogen ambient, wafers were loaded into the PECVD system (Plasma Lab Technology, UK). A thin SiO_xN_y film of (1.5 ± 0.1 nm) was deposited using: nitrogen (N_2) 310 sccm, silane (SiH_4) 5.4 sccm, NITRIOUS Oxide (N_2O) 255.5 sccm, and ammonia (NH_3) 109.5 sccm, at temperature of 300 °C, pressure 0.4 Torr and power 80 W, respectively. After deposition of SiO_xN_y thin films sintering of these films were performed at 400 °C for 30 min. HfO_2 films of 4.2 ± 0.1 nm were deposited on SiO_xN_y films by RF Sputtering system (Material Research Corporation, USA) from HfO_2 target at applied voltage (0.8 kV RF) at deposition pressure (3.4×10^{-3} Torr) for 3 min and followed by sintering at 600 °C for half an hour. Thicknesses of

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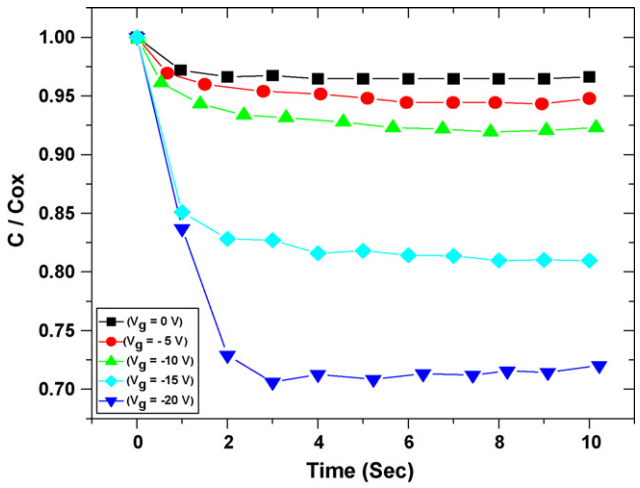

Fig. 1. *C–t* curves of Al/HfO_2/SiO_xN_y/Si gate stacks for different voltages stresses.

above deposited films were measured by Nanofilm ellipsometer at different angles of incidence with wavelength ranging from 300 to 1000 nm. Aluminum (Al) gate electrodes of area 100 μm^2 were defined by standard photolithography and chemical etching techniques. Effect of constant negative voltage stresses on fabricated MIS structures were electrically characterized by *C–t*, *C–V*, *G–V* and D_{it} technique at 100 kHz using the KEITHLY MODEL-82 simultaneous system and *I–V* measurements were performed using KEITHLY MODEL-2602 voltage source at room temperature.

3. Results and discussion

Fig. 1 shows the graph of capacitance as a function of time at the different constant negative voltage stresses (0–20 V). All the curves demonstrate a decrease in the accumulation capacitance and then an asymptotic approach to the saturation value as a function of time. This effect was not significant in the SiO_2 based MOS structures [9]. It is attributed to the detrapping of negative charges in MIS structures. The fact that such *C–t* transients are measured on a time scale of seconds suggest that the charge is trapped inside the HfO_2 layer with in HfO_2/SiO_xN_y/Si structure, away from the Si substrate. The convolution of charge trapping/detrapping in Al/HfO_2/SiO_xN_y/Si structures was further investigated by *C–V* measurements as shown in Fig. 2(a) and (b). Note that from 0 to −20 V stress *C–V* curves gradually shift towards negative voltage axis. Even after the application of large stress voltage ∼−20 V, it remains in a region of negative voltage axis. It is important to note that the shifts of flat-band voltage are quite stable, even at high voltage stress at room temperature.

Therefore, the significant shift towards the negative voltage axis as a result of negative voltage stress is attributed to the positive charge generation with in MIS structures. The stable flat-band voltage shift point out that the positive charges generated probably during *C–V* measurements, do not conflict with the electron trapping within the dielectric stacks [16].

The charge closer to the SiO_xN_y/Si interface, contribute to a significant shift in *C–V* curves as shown in Fig. 2(a) and inset of Fig. 2(b), as well as those nearer to the cathode contribute to the gate leakage current. Hence, the positive charges are most probably located closer to the Si/SiO_xN_y interface, while the negative charges because of electron trapping are to be found nearer to the HfO_2 interface. Shift in *C–V* characteristics is direct evidence for the reduction in capacitance obtained from *C–t* measurements, as shown in Fig. 1.

The conductance technique is considered to be one of the most sensitive techniques for the measurement of interface state density

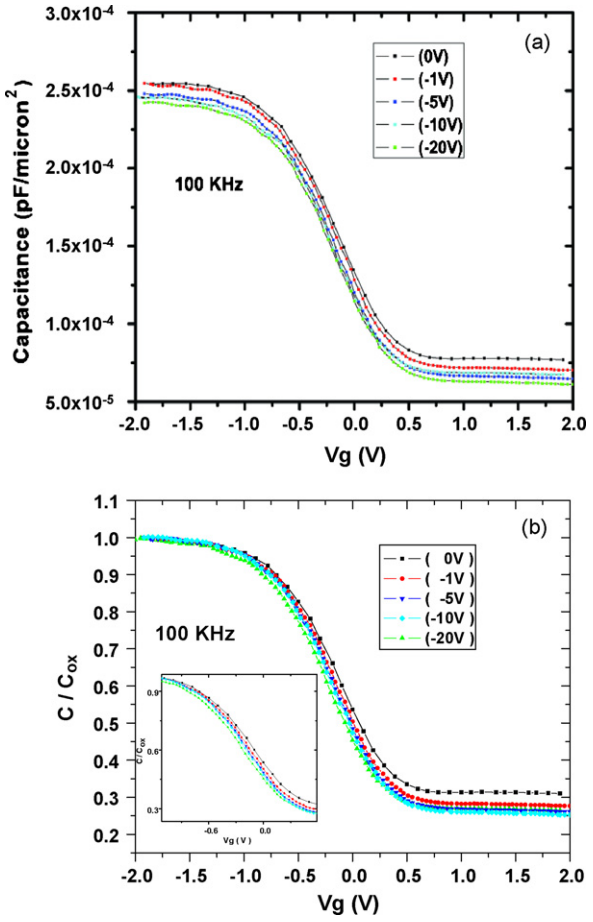

Fig. 2. *C–V* characteristic of Al/HfO_2/SiO_xN_y/Si structure at different negative voltage stresses [capacitance density (a) and normalized capacitance for flat-band voltage shift in (b)].

[17]. Fig. 3 shows the variation in conductance for without voltage stress and after application of constant negative voltage stresses at the dual stack gate dielectric based MIS devices.

As indicated in Fig. 3, the magnitude of conductance computed without voltage stress is 1.26 μS, while after application of constant

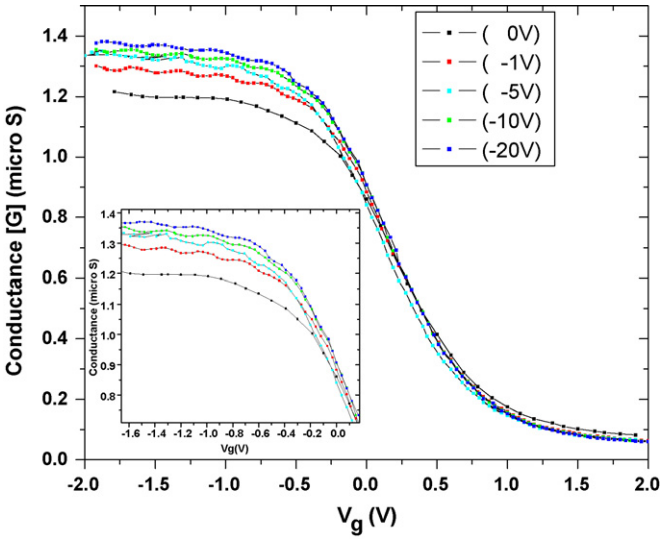

Fig. 3. Conductance (G) vs gate voltage (V_g) without and with constant voltage stresses at 100 KHz frequency.

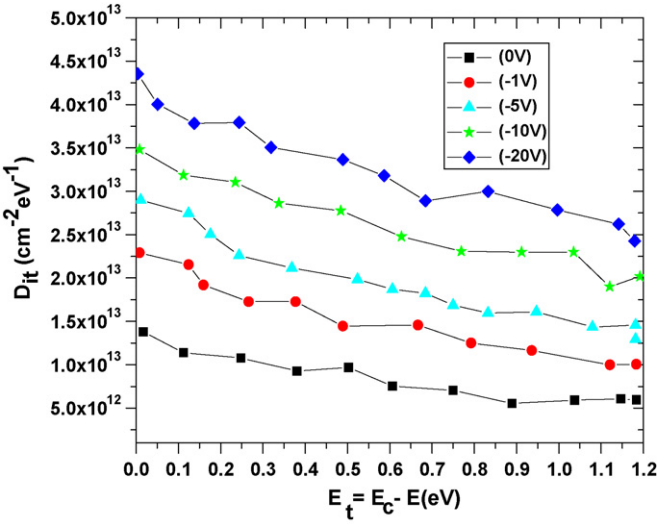

Fig. 4. The interface state density D_{it} at Si/SiO_xN_y/HfO_2 interface of without and with constant voltage stress.

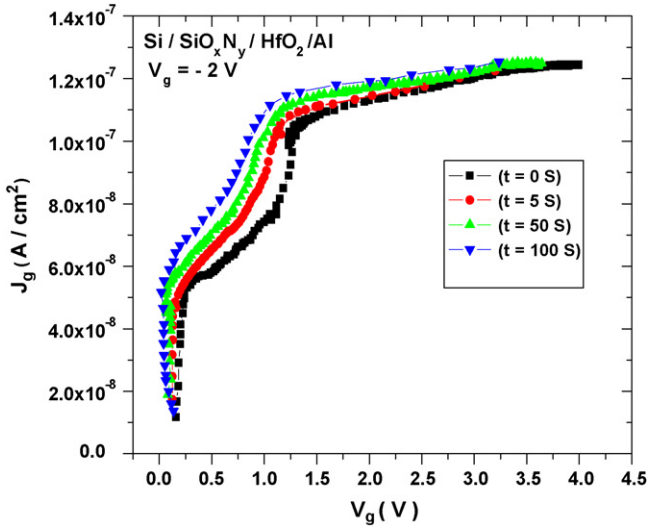

Fig. 5. J_g–V_g characteristics of Al/HfO_2/SiO_xN_y/Si structure after different times of constant gate voltage stress at −2 V.

negative voltage stress (−5 to −20 V), it varies from 1.33 to 1.42 μS. The high conductance values indicate the higher densities of interface traps at the interface after the constant voltage stresses. The variation in number of traps at HfO_2/SiO_xN_y/Si interfaces after constant voltage stress indicates the variation of memory window for non-volatile semiconductor memory (NVSM) device application.

The interface trap density (D_{it}) vs mid band-gap energy (E_t) curve examines the trap densities near the HfO_2/SiO_xN_y/Si interface. When the interface traps started to responding, the relation between the measured apparent accumulation capacitance (C), the admittance of the interface states (C_{it}) (which includes the equivalent parallel interface capacitance and conductance), the true accumulation capacitance (C_s) and the insulator capacitance (C_i) is given by the standard model for MIS diodes [18].

$$\frac{1}{C} = \frac{1}{C_i} + \frac{1}{C_{it} + C_s} \tag{1}$$

If the semiconductor can be biased far enough into accumulation then accumulation capacitance (C_s) can be made very large and C_{it} can be ignored. The effect of shallow states is twofold near accumulation, they contribute to the interface state capacitance and they prevent full accumulation from being reached by pinning the Fermi level [17,18].

The interface traps density of HfO_2/SiO_xN_y/Si interface as shown in Fig. 4 vary more rapidly towards the mid band-gap.

After constant negative voltage stress the interface state density (D_{it}) is significantly increased—an order of two as compared to without any voltage stress. However, it is evident that the interface state densities are higher near the conduction band for the highly negative voltage stressed samples. While, in case of without voltage stress interface states are more diffused [19]. These results support our previous observation C–t, C–V and G–V measurements, after application of constant voltage negative stresses.

However, the leakage current after the negative voltage stress is an amalgamated effect of neutral trap generation, positive charge generation, electron trapping, barrier height of semiconductor, the insulator interface, etc. [20]. The variation of gate leakage current as a function of different negative voltage stress and time are shown in Figs. 5 and 6. As observed, at low field, the gate leakage current increases with stress time, because of the trap-assisted tunnelling. This is analogous to the stress-induced leakage current (SILC). It has become a major phenomenon of concern for the reliability of dual stack gate dielectric based MIS structures. When a voltage stress is applied across a dual dielectric stack based MIS capacitor, the oxides suffer from several degradation mechanisms [21,22]. Figs. 5 and 6 indicate the increase in time-dependent current density at CVS (−2 and −5 V).

All samples were stressed in the depletion and onset of inversion regime, which includes gate depletion effects. Initially, the HfO_2/SiO_xN_y gate dielectric stacks have their own as-grown traps, which play an important role in dielectric wear out. However, as stress time progresses, the applied stress voltage also generates enormous amount of traps in the insulator layers. These traps act both as coulombic scattering centers and as pathways for increased local leakage current, usually known as SILC [22]. SILC contribution has been demonstrated to be due to trap-assisted tunnelling through neutral electron traps generated in the dielectric layer during electrical stress [23,24]. Hence, the time-dependent gate current density ($J^*(t)$) as a function of gate voltage stresses and time can be given by following relation [25–27]:

$$J^*(t) = A\left[1 - \exp\left(-\frac{t}{\tau}\right)\right] + \beta(V_g)t^{\delta} \tag{2}$$

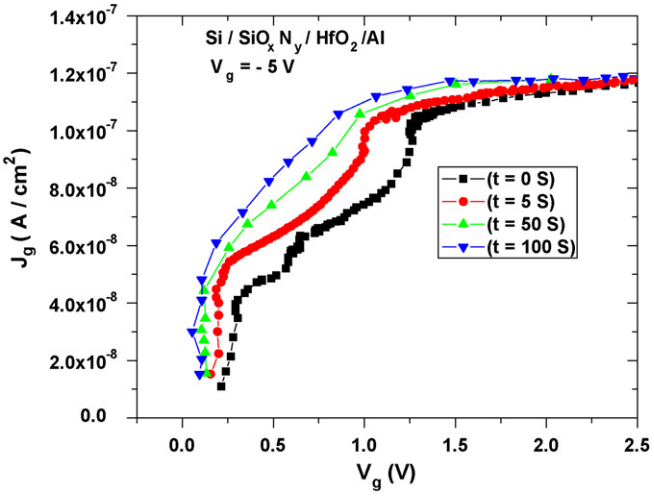

Fig. 6. J_g–V_g characteristics of Al/HfO_2/SiO_xN_y/Si structure after different times of constant gate voltage stress at −5 V.

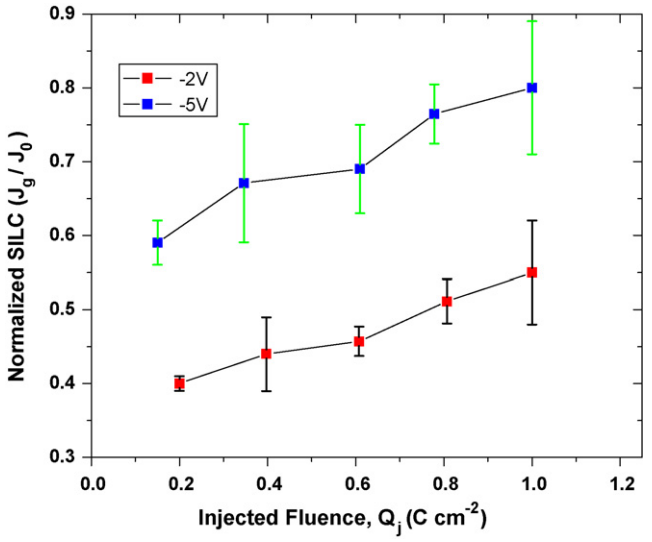

Fig. 7. Normalized SILC as a function of injected fluences at constant negative voltage stress (−2 and −5 V).

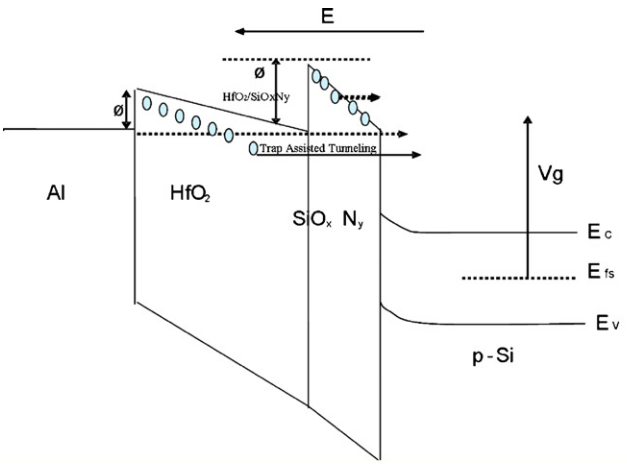

Fig. 8. Schematic energy band diagram of the trap-assisted tunnelling process between conduction bands of Al/HfO_2/SiO_xN_y/Si structure.

Here A and β are constants derived from the plot of bulk traps vs stress time, t is time duration of the applied stress and δ is the trap generation rate.

While τ is given by the following relation:

$$\tau = \frac{q}{\sigma J_g} \tag{3}$$

where q, σ, and J_g are electron charge, trap cross-section and mean current density injected into gate dielectric respectively during the electrical stress. The second term in Eq. (2) accounts for SILC contribution for gate leakage current.

Fig. 7 shows the normalized SILC variation (J_g/J_0) as a function of injected fluences (Q_j) under constant stress voltages at room temperature. It can be seen from curves that there is an increase in the charge trapping, as a function of negative voltage stress.

The generated traps drift into the bulk stack layer via a random hopping mechanism [28,29]. Which results higher SILC and as a function of injected fluence. These outcomes help us in the estimation of time-dependent breakdown voltage of SiO_xN_y/HfO_2 gate dielectric stack and trapping/detrapping of charges for NVSM devices. The neutral traps generated during electrical stress on SiO_xN_y/HfO_2 dielectric stack could be introduced by mobile H^+, which corresponds to Si–OH, Hf–OH trapping centers. The presence of protons in the gate stack is a result of hydrogen containing reacting species, used for the deposition of PECVD based SiO_xN_y films. Therefore, the trapping of H^+ originates from the breaking of bridging Si–OH and Si–NH bonds by mobile H^+ and subsequent trapping of these protons at the HfO_2 sites. The SILC in MIS structures is a corollary of an electron tunnelling between the gate and substrate conduction bands via a stress-induced trap in the gate dielectric stacks.

The complexity in mechanism of trap-assisted tunnelling and the neutral trap generation with in the MIS structures is shown in Fig. 8. It shows that the electron trapping take place closer to the HfO_2 layers. While, the positive charges generates close to the HfO_2/SiO_xN_y interface, where a lot of defects might be present. The positive charges may be because of the trapping of holes or the hydrogen induced [$Si_2 = OH^+$] and/or [$Hf_2 = OH^+$] centers due to the transport of H^+ in the gate stacks.Conclusions

In summary, the reduction in the capacitance of C–t characteristics and a significant shift in C–V curves towards negative voltage axis reveal that the charge trapping/detrapping occurs at the $Si/SiO_xN_y/HfO_2$ interface and HfO_2 bulk. Further more the programming time of NVSM devices with stacked charge trapping layer can be improved. The increase in gate leakage current, after the negative voltage stress is probably due to the trap-assisted tunnelling within the gate dielectric stacks. These SiO_xN_y/HfO_2 gate stacks based devices are promising candidates for the future NVSM device application.

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