Low-Temperature Processed Ni/GeSn Optimal Contacts for Junctionless GeSn-on-Si FinFETs

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Abstract—For junctionless FETs (JLFETs), an optimal ohmic contact is needed to achieve maximum drive current. The scaling of the source/drain (S/D) contact area impacts the contact resistivity ($\rho_{c}$) of FETs, which limits their on current and switching speed. Minimizing the S/D series resistance along with ohmic contacts is the critical factor in JLFET design due to moderate doping levels at S/D. The Ni and GeSn contacts optimized at a low temperature of 200°C by forming gas annealing (FGA) process and the computed contact resistance ($R_{c}$), sheet resistance ($R_{sh}$), and contact resistivity ($\rho_{c}$) for Ni/p-GeSn contacts are 2.04 × $10^{-3}$ Ω cm, 63.96 Ω/□, and 6.18 × $10^{-8}$ cm$^2$, respectively. The impact of capping metal resistance ($R_{m}$) is analytically examined for Ni/p-GeSn contacts using the modified circular transmission line model (cTLM). Furthermore, to study the metal cap resistance ($R_{m}$) effect pragmatically, the optimized GeSn channel FinFET with width/length (W/L) 20/90 nm is analyzed by incorporating an extra metal cap at contacts and its electrical characteristics were compared with the control sample. The result demonstrates that the effect of metal resistance is very significant in low sheet resistance ($R_{sh}$) materials, where $R_{sh}$ is close to $R_{m}$.

Index Terms—Contact, circular transmission line model (cTLM), depletion FET, FinFET, germanium, GeSn, junctionless FETs (JLFETs), metal resistance, resistivity.

I. INTRODUCTION

Following Moore’s law, the aggressive decrease in CMOS feature size and downscaling of MOSFET contacts is causing issues in precise junction formation and dopant activation. For semiconductor devices, especially junctionless FETs (JLFETs), an optimal ohmic contact between the electrode and the semiconductor layer is needed to achieve maximum current density [1]. JLFETs have simplified fabrication process and reduced thermal budget as a result of the exclusion of S/D doping activation.

With the aggressive downscaling of FET dimensions, the source/drain (S/D) contact resistance ($R_{c}$) becomes the bottleneck that limits the FETs performance. For nanoscale devices, the total resistance of transistors is determined by the pad and metal–semiconductor (MS) contact resistance. Higher resistance at the S/D interface can decrease the ON-state current, and a moderate level of doping in JLFETs can make it challenging to form ohmic S/D contacts. Hence, minimizing the series resistance and achieving suitable ohmic contacts at the S/D are crucial factors in JLFET design [2], [3], [4]. To achieve volume depletion in the channel region of JLFETs during the OFF-state, it is necessary to carefully design the doping concentration of the channel and active channel thickness. Nevertheless, in JLFETs with realistically achievable channel film thicknesses, volume depletion can only be attained when the channel region is moderately doped [5], [6]. A higher doping level in the channel region requires an ultrathin semiconductor channel for volume depletion and causes a decline in mobility due to increased ionized impurity scattering effects.

However, MS interfaces exhibit fermi-level pinning that becomes the dominant cause of parasitic resistance at transistor source and drain contacts. With the downscaling of the contact area, the contact resistance increases unless the specific contact resistivity is reduced to meet the ON current ($I_{on}$) [7]. Accounting the effects of contact resistance is necessary because it can lead to high power consumption and compromise the performance of devices. An optimal specific contact resistivity ($\rho_{c}$) is essential to alleviate the impact of contact resistance ($R_{c}$) in the source/drain (S/D) regions. In GeSn FinFETs, another critical concern is that the increased exposed surface area of fins may decline their thermal stability, making it crucial to use a fabrication method with a low thermal budget to preserve the quality of the GeSn fin channels [8]. To maximize the exceptional charge transportation capabilities of germanium, it is necessary to develop a low-resistance contact method using metal germanides at low process temperatures. This approach will resemble the utilization of self-aligned...
metal silicides in the conventional CMOS process, currently employed for Si technology [9]. Furthermore, to realize high-performance FETs, it is necessary to have high levels of doping and precise dopant active regions at the contact metal interface. Due to the shrinking thickness of source/drain regions and the concentration of implanted dopants that is high at a certain depth, the drain–source electrodes need to be recessed into the semiconductor at a high concentration region [10]. Alternatively, molecular beam epitaxy (MBE) offers to grow thin Ge epitaxial layers on Si substrates, doping them with groups III and V elements beyond the equilibrium maximum solid solubility of $1.2 \times 10^{19}$ cm$^{-3}$ [11].

The germanium-tin (GeSn) is a promising potential candidate because it allows for direct integration on Si with significantly higher carrier mobility. Incorporating Sn into Ge to form GeSn reduces the effective mass and enhances carrier mobilities [12], [13], [14], [15] and its ability to seamlessly integrate with the standard Si CMOS manufacturing process [16]. Numerous studies for low contact resistivity have been proposed for metal/Ge contacts [9], [17], [18], [19], [20]. However, fewer experimental studies have been published on the metal/semiconductor contact resistivities for p-GeSn JLFEETs devices, while considering moderate doping limitations.

Numerous metals have been analyzed with germanium to create a low contact resistance. Among these metals, nickel (Ni) stands out as the most promising candidate for microelectronic contact formation applications [21]. Furthermore, various techniques such as hydrogen (H$_2$) forming gas annealing (FGA) treatments, postoxidation annealing (POA) treatments, and solution-based treatments, have been investigated for use in Ge technology for high-$κ$/Ge interface passivation. Additionally, H$_2$-based methods may be employed in the MS structure to facilitate NiGe formation at low temperatures, which inhibits the formation of GeO$_x$ and results in improved contact resistivity [22]. In this work, N$_2$ and H$_2$ mixture with 10% H$_2$ is employed for the germanides reaction formation at 350 °C.

The circular transmission line model (cTLM) is the most commonly used method in the semiconductor industry to determine the contact resistivity $ρ_c$. For low $ρ_c$ cases, neglecting the metal resistance can result in an incorrect interpretation of effective $ρ_c$ and inaccurate extraction. Marlow and Das [23] developed an analytical model approach that accounts for the metal resistance role in transmission line model (TLM). Furthermore, Dormaier et al. [24] and Yu et al. [25] proposed a refined TLM structure to minimize the influence of metal resistance. The cTLM extraction is a more straightforward process as compared to TLM [26]. This offers a self-isolating structure that obviates the need for MESA etching to prevent current crowding as shown in Fig. 1(a)–(d). In cTLM structures, the transfer length, contact resistance, and sheet resistance can be extrapolated and used to calculate the value of $ρ_c$ [27], [28].

In this work, we have grown the epi-GeSn active layers over a Si wafer using an improved MBE process. The p-GeSn/n-Ge/Si has been grown by a prior optimized process. After that, the Ni metal was sputtered to fabricate cTLM structures using a standard photolithography technique. The structures were optimized at low annealing temperatures under the ambient of FGA (H$_2$+N$_2$) to achieve low contact resistivity, keeping the concerns for the low thermal budget of GeSn fins for FinFET devices. Ni/p-GeSn stack was further analyzed by X-ray photoelectron spectroscopy (XPS) depth profiling. We have utilized the cTLM alongside improved techniques for extracting the accurate $ρ_c$ [25]. Furthermore, to study the impact of capping metal resistance by modified TLM model to compute the effective contact resistivity, finally, the width/length (W/L) 20/90-nm GeSn channel FinFETs were fabricated using the prior optimized process stated in our previous reports [29] to demonstrate the effect of metal capping resistance at S/D contacts.

II. EXPERIMENT

A. Ni/p-GeSn and Ni/p-Ge Contacts

The Si (100) wafer is used for MBE growth with a specific resistance of around 20 $Ω$·cm. A 50-nm-thick Si buffer layer was deposited after annealing, followed by the growth of a virtual Ge substrate (Ge-VS) [29], [30], [31] with a thickness of 100 nm on top of it. The Ge-VS was annealed at 850 °C for 5 min to reduce the threading dislocation density [32], [33]. A n-Ge buffer layer with 400 nm thickness was grown on the Ge-VS, with an antimony (Sb) concentration of 1E16 cm$^{-3}$ at 250 °C [34]. On the n-Ge layer, a 30-nm p-GeSn channel layer was grown with a boron (B) concentration of 1E18 cm$^{-3}$ with 8% tin (Sn) at growth temperature ≤170 °C [35]. Similarly, p-Ge/n-Ge$_{0.96}$Si and n-Ge$_{0.96}$Si samples were grown but without Sn doping. The samples were cleaned in a dilute 2% HF solution for a 30-s dip, followed by 5-min immersion in 10% HCL solution. The cTLM patterns were fabricated by lithography with circle inner radii ($r = 50 \text{ μm}$) and gap spacing ($d$) ranging from 4 to 48 $\text{μm}$ as illustrated in Fig. 1(d). After exposure and resist development, the scum removal was carried out by using the reactive ion etching (RIE) tool under O$_2$ plasma for 10 s and power of 60 W. Around ~60-nm-thick
Ni metal was sputtered over all sets of devices, with a dc power of 8 W, Ar gas flow of 70 sccm, base pressure of 9E-7 mbar, and process pressure of 5E-3 mbar. Thereafter residual metal was removed by the liftoff method. A set of devices undergo optimized RTA treatment under H2/N2 (1:10) ambient for 1 min at 350 °C to form the Ni germanide (NiGe) layer. The samples were characterized by using the Keithley 4200 SCS system cascaded with four probe station.

### B. P-GeSn FinFET

The FinFET devices were fabricated by the prior optimized process over the same sample wafers [29], [30]. The key fabrication process flow is represented in Fig. 2(a). The micrograph of the fabricated device is depicted in Fig. 2(b). The FinFET configuration includes the p-GeSn channel and underneath the n-Ge layer creates the p-n diode between both layers [29], [30]. The device cross sections and layer details are depicted in Fig. 2(c) and (d). The FinFET contacts were optimized by FGA at 350 °C. Moreover, the S/D contacts were capped with Ti metal on one set of devices to perceive the metal resistance effect.

### III. RESULTS AND DISCUSSION

#### A. cTLM Contact Resistivity Measurements

The extraction of contact resistivity of p-GeSn/n-Ge/Si FinFETs has been done using the cTLM architecture as standard rectangular TLM structures are subject to the current crowding effects. The rectangular TLM structures are subject to the higher current density at the contact rectangle edges, whereas in cTLM, current is evenly distributed around the circle circumference. Furthermore, the cTLM structures are patterned in the single-step lithography, whereas MESA structures are required for the counterpart rectangular TLM to avoid current crowding. The current versus voltage (I–V) and current density versus voltage (J–V) characteristics were measured by applying the voltage at the inner metal contact to the outer metal contact. The total resistance was measured by a four-probe current–voltage measurement setup connected to the characterization system to avoid the probe wire and contact resistance effects. The schematic shown in Fig. 1(a) depicts the linear model, the transfer lengths, probe placement, and circular gap spacing between contacts along with energy band modulation. The SEM micrograph, optical profilometer, and 3-D structure view of the fabricated devices are depicted in Fig. 1(b)–(d), respectively.

For the resistance measurement, the outer end probes were used to drive the current from the inner circular contact to the outer contact, whereas the inner two probes (one on inner contact, while the other one at outer contact) were used for the voltage difference measurement, as shown in Fig. 1(d). The same measurement procedure was repeated on structures with different spacings 4–48 μm. The total resistance, $R_{\text{total}}$, between the inner and outer contact is described by the following relation:

$$R_{\text{total}} = \frac{R_{\text{sh}}}{2\pi r} [d + 2L_T] \cdot C \tag{1}$$

$$C = \frac{r}{d} \ln \frac{r + d}{r}. \tag{2}$$

The top p-type germanium thin layer sheet resistance is given by $R_{\text{sh}}$, and $r$ is the radius on the inner contact. Spacing between inner and outer contacts is denoted by $d$, and $C$ is the correction factor defined by (2). The correction factor $C$ is used as a compensation to distinguish between the TLM and the cTLM approach, which is employed for a linear approximation of the experimental data. In the absence of $C$, cTLMs may undervalue $\rho_c$. The cTLMs structure featured an inner contact radius of 50 μm

$$L_T = \sqrt{\rho_c / R_{\text{sh}}} \tag{3}$$

$$\rho_c \approx R_{\text{sh}} \cdot L_T^2 \tag{4}$$

Transfer length is denoted by $L_T$, the effective contact length contributed to the current conduction. $L_T$ would be higher for higher contact resistivity of the contact and low sheet resistance ($R_{\text{sh}}$) of the semiconductor. The current–voltage ($I–V$) curves were plotted for Ni/p-GeSn and Ni/p-Ge contacts for both 250 °C and 350 °C annealed contacts under FGA ambient, as described in Fig. 3(a)–(d), respectively. The results from Fig. 3(a) and (b) clearly show that the contacts are ohmic in both samples. However, the current has significantly increased in the 350 °C annealed sample, which demonstrates the NiGe germanide formation at the interface, which possibly overcomes the hole barrier at the valence band edge. Fig. 3(c) demonstrates the current density versus applied voltage profiles for different temperature-treated samples. The inset of Fig. 3(c) describes the significantly improved current levels for the 350 °C processed sample even at the low voltage. The current density in the sample annealed at 350 °C is significantly enhanced, approaching $10^5$ A/cm² as compared to $3 \times 10^2$ A/cm² in the sample annealed at 250 °C, both measured at 1 V. The 350 °C sample’s $I–V$ curves meet the system current compliance of 0.1 A, as shown in Fig. 3(c). The hole Schottky barrier height ($q\phi_{\text{bh}}$) lowering and reduction in the tunneling distance by high semiconductor doping are

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**Fig. 2.** (a) Process summary of p-GeSn/n-Ge/Si FinFETs. (b) Illustrates the SEM micrograph of the FinFET device. Inset: magnified version depicts the fins. (c) and (d) Depicts the cross-sectional cut schematics along source to drain and across gate, respectively [5], [29].
two effective methods for decreasing $\rho_c$. Fig. 3(c) reveals that temperature treatment at 350 °C leads to the formation of germanide described by ohmic nature of $I$–$V$ curves. The boron (B) doping at $1 \times 10^{18}$/cm$^3$ further decreases the tunneling region at the valence band edge. Moreover, the Sn (8%) doping reduces the barrier height [36] is illustrated in Fig. 1(a). The reduction of the hole barrier height ($q\phi_B$) due to Sn incorporation has been verified through the electrical characterizations. The performance of the Ni/p-GeSn device was compared with that of the Ni/p-Ge (control sample) with similar doping concentration and process conditions but without Sn doping, as illustrated in Fig. 3(d)–(f). In Fig. 4, total resistance versus spacing results of Ni/p-GeSn were compared with the control sample (Ni/p-Ge) and (Metal cap/Ni/p-Ge). The computed contact resistance ($R_c$), sheet resistance ($R_{sh}$), and contact resistivity ($\rho_c$) for Ni/p-GeSn are $2.04 \times 10^{-3}$ Ω·cm, 63.96 Ω/□, and $6.18 \times 10^{-8}$ Ω·cm$^2$, respectively. Similarly, the computed $R_c$, $R_{sh}$, and $\rho_c$ for Ni/p-Ge are $9.73 \times 10^{-3}$ Ω·cm, 117.18 Ω/□, and $7.40 \times 10^{-7}$ Ω·cm$^2$, respectively. Table I compares the specific contact resistivity with different doping levels and process temperatures in the literature.

Furthermore, the Ni/n-Ge, Ni/p-Ge, and Ni/p-GeSn contacts have been optimized by measuring the reverse current density ($J_R$) at 0.5 V·s at different process conditions, such as annealing temperature and H$_2$:N$_2$ gas flow, as depicted in Fig. 5(a) and (b), respectively. The Ni/p-Ge and Ni/p-GeSn contacts are ohmic even at low temperatures 250 °C – 350 °C, but the reverse current improves with increasing temperature. This study aims to achieve low contact resistivities at low temperatures, keeping the concerns for the low thermal budget of GeSn fins, so no further temperature was increased for the Ni/p-Ge and Ni/p-GeSn contacts. However, the Ni/n-Ge contacts are observed Schottky in nature up to 375 °C (results not shown here). This is possibly due to strong Fermi-level pinning at the metal/n-Ge interface, where the metal Fermi level is pinned to the valence band edge of the Ge, irrespective of metal work function, and leads to a high $e^-$ Schottky barrier height [22], [42]. Furthermore, the Ni/p-GeSn contacts were analyzed by the XPS depth profiling, as shown in Fig. 6. In XPS depth analysis, the surface was etched using an Ar$^+$ ion (1 KeV) plasma for around 15 s for each cycle. XPS data were collected with $<2$ nm per cycle resolution depth. Thereafter, several etch cycles were run until the GeSn layer was not reached. The Ni2p, Ge3d, and Sn3d atomic concentrations were measured as a function of etch levels (etch time). Fig. 6 shows the trace element (normalized scale atomic percentage)

<table>
<thead>
<tr>
<th>Structure</th>
<th>Doping</th>
<th>$\rho_c$ (Ω·cm$^2$)</th>
<th>Treatment</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni/n-GeSn</td>
<td>$7.7 \times 10^{17}$</td>
<td>$1.5 \times 10^{-7}$</td>
<td>RTA, 400 °C</td>
<td>[37]</td>
</tr>
<tr>
<td>Yb/GeSn</td>
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<td>$1 \times 10^{-6}$</td>
<td>RTA, 500 °C</td>
<td>[38]</td>
</tr>
<tr>
<td>Ni/n-GeSn</td>
<td>$5 \times 10^{20}$</td>
<td>$1.3 \times 10^{-6}$</td>
<td>RTA, N$_2$, 400 °C</td>
<td>[39]</td>
</tr>
<tr>
<td>Ni/p-GeSn</td>
<td>$2 \times 10^{18}$</td>
<td>$6.4 \times 10^{-6}$</td>
<td>RTA, 350 °C</td>
<td>[40]</td>
</tr>
<tr>
<td>Ti/Au/p-Ge</td>
<td>$4 \times 10^{20}$</td>
<td>$7.7 \times 10^{-8}$</td>
<td>RTA, N$_2$, 400 °C</td>
<td>[16]</td>
</tr>
<tr>
<td>NiGe/p-Ge</td>
<td>$8.4 \times 10^{20}$</td>
<td>$4 \times 10^{-8}$</td>
<td>RTA, N$_2$, 350 °C</td>
<td>[41]</td>
</tr>
<tr>
<td>Ni/p-Ge</td>
<td>$1 \times 10^{18}$</td>
<td>$2.5 \times 10^{-6}$</td>
<td>RTA, N$_2$H$_4$, 350 °C</td>
<td>[38]</td>
</tr>
<tr>
<td>Ni/p-GeSn</td>
<td>$1 \times 10^{18}$</td>
<td>$6.18 \times 10^{-8}$</td>
<td>RTA, N$_2$H$_4$, 350 °C</td>
<td>[38]</td>
</tr>
</tbody>
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across the Ni/p-GeSn structures depth as well as the variation in atomic percentage across individual layers. In Fig. 6(b), the energy level at 852.6 eV signifies the presence of Ni (metal), whereas the energy level at 853.6 eV signifies NiO\textsubscript{x} formation. Fig. 6(c) and (d) displays the Ge3d and Sn3d energy spectra at 29.3 and 485.2 eV, respectively. The XPS results reveal that FGA effectively suppresses the GeO\textsubscript{x} formation at the Ni/GeSn interface.

B. Effect Metal Capping Over Contact Resistivity

The metal resistance plays a significant role in the accurate estimation of $\rho_c$ and $R_{sh}$. The placement of probes at a distant location, contact metal aging (formation of oxides), and capping metals is also attributed to additional metal resistance ($R_m$) [23]. Therefore, the metal resistance ($R_m$) effect also needed to be incorporated and accounted. Otherwise, the cTLM’s $R_{total}$ versus gap spacing relation yields deviation and inaccuracy in the extraction of $\rho_c$, $R_m$, and $R_{sh}$ due to the effect of $R_m$. The high-temperature metal processing to achieve ohmic contacts also leads to metal oxide formation, resulting in $R_m$ variation. Furthermore, if additional capping metals have been deposited, it results in additional series resistance. For such high $R_m$ values, significant voltage drops occur in the metal itself, which suppress the voltage drop between the metal contacts. Consequently, overall $R_{total}$ increases and intercepts at a higher $R_c$ value. Hence, it is essential to examine how the presence of a non zero metal resistance affected $\rho_c$. An analytical model incorporating the influence of $R_m$ has been developed by Marlow [23]. Another simplified cTLM lump model was proposed with an incorporated metal resistance effect [25]. The model suggests that the metal resistance effect can be seen at the metal contact edge by current distribution within the metal contact. When $R_m$ is neglected ($R_m \ll R_{sh}$), the current crowding length is equal to the well-known transfer length ($L_T$). To demonstrate current crowding at the metal edge, the normalized current distribution is plotted against the metal contact edge distance using (5)–(9). The current crowding as a function of distance from contact edge for p-GeSn, p-Ge, and n-Ge devices is depicted in Fig. 7(a).

Fig. 4. Total resistance cTLM measurements for gap spacing 4–48 μm. The upper three data points represent Ni/p-Ge and lower three for Ni/p-GeSn for 250 °C, 300 °C, and 350 °C annealing, respectively. Mid data points represent metal cap/Ni/p-GeSn annealed at 350 °C.

Fig. 5. (a) and (b) Optimized contacts reverse current density ($J_R$) at different annealing temperatures and H\textsubscript{2}:N\textsubscript{2} (1:10) gas flow for Ni/n-Ge, Ni/p-Ge, and Ni/p-GeSn contacts.

Fig. 6. (a) Depicts the Ni/GeSn stack analyzed by the XPS depth profile. (b) Depicts the descend etch levels for Ni. (c) and (d) Demonstrates Ge and Sn ascend etch levels with etch time, respectively.

Fig. 7. (a) Normalized current distribution along the contact edge in the semiconductor for Ni/p-GeSn, Ni/p-Ge, and Ni/n-Ge contact resistivities of $6.18 \times 10^{-8}$ Ω · cm\textsuperscript{2}, $7.40 \times 10^{-7}$ Ω · cm\textsuperscript{2}, and $2.52 \times 10^{-5}$ Ω · cm\textsuperscript{2}, respectively. Inset (b) shows the cTLM model schematic for considering $R_{sh}$ and $R_m$. (c) Depicts the 3-D plot of normalized current distribution along the metal contact edge with variation in the contact resistivity.
have been demonstrated. The results reveal that for Ni/p-GeSn contact having low $\rho_c$ ($6.18 \times 10^{-8} \, \Omega \cdot \text{cm}^2$), the maximum current flows and crowds near the edge of metal contact, while the Ni/n-GeSn contact with a high $\rho_c$ ($2.52 \times 10^{-5} \, \Omega \cdot \text{cm}^2$), the current flows/distributes far from the metal edge. Inset Fig. 7(b) depicts the cTLM model schematic for considering $R_{sh}$ and $R_m$. Fig. 7(c) shows the 3-D plot demonstrating the current distribution along the metal edge, corresponding to the contact resistivity. This indicates that the current flow within the semiconductor spacing is the same, but the current distribution under metal contact is influenced by the contact resistivity

$$I(x) = C_1 + C_2 \exp\left(\frac{r-x}{\alpha}\right) + C_3 \exp\left[-\frac{r-x}{\alpha}\right]$$

$$\alpha = \sqrt{\frac{\rho_c}{R_{sh} + R_m}}$$

$$C_1 = \frac{R_m}{(1/L_m)}(0)/(R_m + R_{sh})$$

$$C_2 = C_1 \left(\frac{R_{sh}}{R_m}\right) \exp\left(-\frac{d}{\alpha}\right)$$

$$C_3 = -C_1, \quad \text{When} \quad r/4 \gg \alpha$$

$$L' = \frac{a}{R_m} + \frac{R_m(r-a) + aR_{sh}^2}{R_m + R_{sh}}$$

$$\rho'_c = \frac{R_{sh}L'^2}{C_R}.$$ 

In laboratory extraction, the metal/semiconductor contact resistivity is measured using a four-probe setup to nullify the probe contact resistance effects. However, in integrated circuits, the contact metal is capped with other metals, interconnects, and metal plugs. These additional metals also contribute to the metal series resistance. When the capping metal resistance is high, $R_m (\geq 1 \, \Omega \Box$), it plays a significant role in the accurate estimation of the contact resistivity, especially when $R_{sh}$ is close to $R_m$.

The TLM methods only utilize $L_T$ and $R_{sh}$ for the interpretation of $\rho_c$ through the interpret method. To compute the effective contact resistivity ($\rho'_c$), the experimentally extracted $\rho_c$ and $R_m$ parameters from the cTLM measurement structures (Ni/p-GeSn, Ni/p-Ge, and Ni/p-Ge) are entered into a modified TLM extraction model [(10) and (11)] [23]. Furthermore, the former equations were computed with nonzero metal resistance to demonstrate the effect of additional capping metal resistance on $\rho'_c$. When $R_m = 0 \, \Omega \Box$, $\rho_c = \rho'_c$. To demonstrate the effective resistivity variation, the set of metal cap resistance values (0–40) $\Omega \Box$ was taken as variables to analytically solve the equations and to perceive the effect of metal cap resistance over $\rho'_c$. The results in Fig. 8 reveal that capping metal resistance ($R_m$) affects the low contact resistivities more as compared to high contact resistivities. For instance, $\rho'_c$ (p-GeSn) is changed from $6.18 \times 10^{-8} \, \Omega \cdot \text{cm}^2$ ($R_m = 0$) to $2.10 \times 10^{-6} \, \Omega \cdot \text{cm}^2$ ($R_m = 2 \, \Omega \Box$) as compared to $\rho'_c$ (n-Ge) that is changed from $2.52 \times 10^{-5} \, \Omega \cdot \text{cm}^2$ ($R_m = 0$) to $3.42 \times 10^{-5} \, \Omega \cdot \text{cm}^2$ ($R_m = 2 \, \Omega \Box$). This signifies that if the impact of the metal resistance is not considered, the $\rho_c$ values may be overestimated, particularly when dealing with low resistive contacts and high $R_m (\geq 1 \, \Omega \Box)$. Therefore, the effective contact resistivity $\rho'_c$ should be regarded when contact is capped with high $R_m$ metal.

C. Junctionless p-GeSn Channel FinFET Device Characterization

The implemented Ge channel depletion mode junctionless FinFET design exhibits the device’s high $I_{ON}$ while maintaining $I_{OFF}$. To ensure precise electrostatic control by the gate, it is essential to maintain the fin width lowest possible. $W_{fin}$ should be less than 2/3 of $L_f$ (the gate length). The effective width, denoted as $W_{eff} = n(2H_{fin} + W_{fin})$, $n$ is the number of fins. Here, $W_{fin}$, $H_{fin}$, and $L_f$ were kept at 20, 30, and 90 nm, respectively. For FinFET devices, the optimized Ni/GeSn contact formation was implemented as discussed in the previous sections. To study the effect of capping metal (Ti) over the drain–source pads, Ti metal was additionally deposited over the Ni contacts. Metal cap device samples were processed at 350 °C RTA for 1 min.

The transfer characteristics of the implemented GeSn FinFET ($W/L = 20/90$ nm) are shown in Fig. 9. The improved characteristics and enhanced FinFET device performance as a result of optimized process achieved by tuning the annealing conditions. The device demonstrates $I_{ON}$ of 52 $\mu A/\mu m$ and $I_{OFF}$ of 36 nA/\mu m at drain voltage ($V_d = -0.1$ V),
transconductance \( (g_m) \) of 98 \( \mu S/\mu A \), and subthreshold swing SS of 116 mV/dec, measured at \( V_g = -0.1 \) V. The inset of Fig. 9 depicts that the \( I_{ON} \) current is significantly reduced to 46 \( \mu A/\mu m \) in the metal-capped contacts demonstrated by the dotted line. The short channel effects (SCEs) in the devices, where only Ni metal is used for S/D contacts, have significantly improved. The transconductance \( (g_m) \) is one of the prime metrics to measure the transistor performance. The transconductance \( (g_m) \) was tremendously improved to 98 \( \mu S/\mu A \) in the Ni/GeSn devices, possibly due to the optimized metal contacts, which results in reduced device’s external resistance. However, \( g_m = 87 \mu S/\mu A \) was measured for the Ti (metal cap)/Ni/GeSn devices, as shown in Fig. 10(a). Furthermore, the subthreshold swing for both devices was recorded SS = 120 and 116 mV/dec for Ni/GeSn and Ti (metal cap)/Ni/GeSn devices, respectively, as depicted in Fig. 10(b). To further confirm the degradation in the SCEs due to capping metal resistance, the device’s internal resistance, \( R_{ON} \equiv (V_{DS}/I_{DS}) \), was measured as the function of the gate overdrive voltage [43], as illustrated in Fig. 10(c). The internal resistance in both Ni/GeSn and Ti/Ne/GeSn devices is nearly matched. However, the transfer characteristics exhibit significant variation. This obliquely signifies that the degradation of the SCE is due to external capping metal resistance.

IV. CONCLUSION

The optimization of Ni/p-GeSn contacts for junctionless GeSn FinFETs has been successfully demonstrated. The \( H_2:N_2 \) FGA effectively achieved the ohmic Ni/p-GeSn contacts for moderately doped drain and source regions at low process temperatures. This meets the concerns for the low thermal budget of GeSn fins for FinFET device development. The impact of metal resistance has been demonstrated by using the cTLM lumped model over the extracted contact resistivities for Ni/p-GeSn, Ni/p-Ge, and Ni/n-Ge contacts. The results reveal that even low metal resistance significantly affects contact resistivity. Finally, the effect of capping metal resistance has been demonstrated by analyzing the Ni/GeSn FinFET characteristics. It is concluded that for low \( R_{th} \) semiconductors and at low contact resistivities, the selection and processing of drain–source contact metals are very crucial.

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