A Switch-Capacitor DAC Successive Approximation ADC Using Regulated Clocked Current Mirror

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***Abstract*—This paper presents a novel design of switch capacitor DAC successive approximation analog to digital converter (SAR-ADC) using regulated clocked current mirrors. The regulated clocked current mirror (RCCM) design is introduced to source (and sink) the constant current to (and from) the only capacitor in the circuit. The RCCM functions dynamically providing invariable current when required. Moreover when active, RCCM is capable of stabilizing the output current even in presence of voltage variations at its output. DC reference current from RCCM, charging or discharging the single capacitor in the circuit, is controlled by pulse width modulated signal to realize switch-capacitor DAC. Verilog-A script is written for switch control scheme to generate the control signals for RCCM. A dynamic latched comparator is employed to reduce the power consumption in circuit. An 8-bit SAR ADC that exhibits a maximum sampling frequency of 100 kHz is designed in 90 nm CMOS technology and its working is verified through circuit level simulations. This ADC achieves signal to noise and distortion ratio (SNDR) of 45.62 dB which corresponds to effective number of bits (ENOB) of 7.3 bits. At 1 V supply and 100 kS/s, power consumption in ADC is 6 µW while the calculated peak values of DNL and INL are +1.06/-0.40 LSB and +0.53/-1.33 LSB respectively.**

***Index Terms*—SAR ADC, switch-capacitor DAC, regulated clocked current mirrors, Verilog-A, dynamic comparator**

I. Introduction

SAR ADCs have various multipurpose applications in sensor interface circuits, biomedical devices, portable electronics etc. [1]. Further, due to addition of interpolative 2-bit/cycle architecture, SAR ADCs are being used in high bandwidth communication areas [2]. Although SAR ADCs are power efficient compared to other ADC architectures, the chip size and switch control complexity significantly increases with the resolution [3]. Moreover, the capacitor matching that can be realized in the process affects the achievable ENOB, limiting the resolution of ADC. The primary limitation of conventional SAR ADC comes from the requirement of the large layout area needed by high resolution ADC. Additionally, for conventional SAR ADCs having array of capacitor as a DAC, the capacitor area, corresponding number of switches and their control is still an issue for the design. Thus, to realize the various different applications on a single chip, an energy efficient SAR ADC architecture demands small layout area and simple SAR logic regardless of ADC resolution.

Switch-capacitor DAC SAR ADC has this advantage over existing architecture and can be considered for such applications. In this type of ADC, dc reference current, charging or discharging the only capacitor in the circuit is controlled by the pulse width modulated signal, to realize the switch-capacitor DAC. It results, a SAR ADC that can be realized by only a single capacitor, current source and sink, a comparator and a control logic, which will lead to substantial area reduction. Besides this, only one capacitor and optimum switches in the circuit will reduce SAR logic complexity irrespective of the resolution of ADC.

The most crucial part of such ADC is to design current source and sink providing invariable current over the required range of frequency albeit the voltage changes at output (source/sink) node, with minimum mismatch in source and sink currents. Earlier Zhang [4] demonstrated a 6 bit ADC in 350 nm technology using cascode current mirror which has a drawback, that the current mirrors are not able to supply constant current when required. This results in mismatch between source and sink current, degrading the performance of ADC. Furthermore the finite output impedance of the standard current mirror cannot accommodate voltage change at its output when, implemented in 90nm technology node and introduce variability in current thereby increasing the non-linearity errors in ADC.

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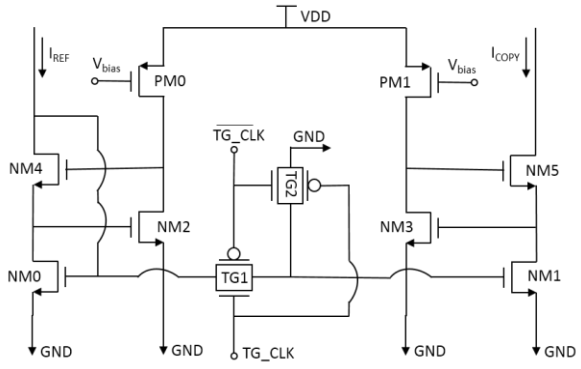

Figure 1. NMOS RCCM (Current Sink).

In this work, a SAR ADC using switch-capacitor DAC is proposed, that uses current source and sink with minimum current mismatch. For this a regulated clocked current mirror (RCCM) has been designed to source/sink invariable current even if voltage at its output node changes regularly. As a result, this ADC approach can be a good solution for low/medium speed applications such as MEMS sensor interface circuits, where the layout area of ADC is required to be kept small while preserving the other design parameters.

The paper organization is as follows. Section II presents the design of ADC circuit components. Section III describes switch-capacitor DAC SAR ADC design and architecture. The simulation results are shown in section IV, followed by conclusion in section V.

II. ADC Circuit Components

A. Regulated Clocked Current Mirror

This type of SAR ADC demands current mirror to work dynamically. It must source/sink constant current when required and be inactive otherwise. Although active loads in standard cascode current mirror increases output resistance of the mirror, the current doesn't remain constant over voltage change at sourcing/sinking node. Increasing the transistor size in standard cascode current mirror doesn't help as it hampers the transient response of the mirror.

Fig. 1 shows the transistor level implementation of NMOS RCCM (Current Sink).

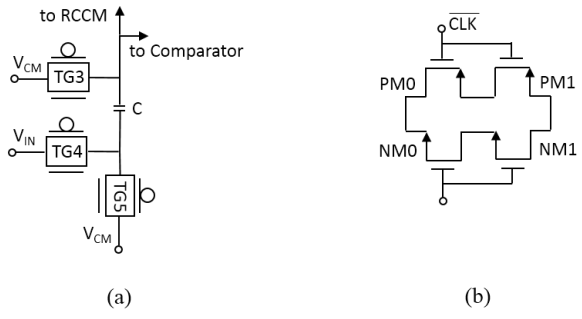

Figure 2. (a) Input Sampling Implementation, (b) Stacked Transmission Gate.

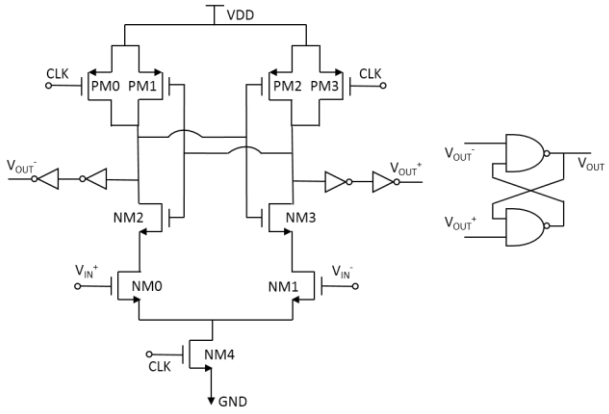

Figure 3. Dynamic Latch Comparator.

It has buffer placed between copying and reference circuit which holds the drain potential of NM1 to a fixed value. Doing so reduces the channel length modulation effect and increases the output impedance of the mirror so that the drain current change with respect to change in voltage at source/sink node is minimized [5]. Transmission gate switches TG1 and TG2 are used to provide dynamic functionality to the mirror. Instead of placing switch between the current mirror and the capacitor, it is incorporated within the current mirror itself. This helps to minimize the major predicament of channel charge injection in scaled down switched capacitor circuits.

As observed, the output current I_{COPY} is controlled by gate voltage of NM0 as well as terminal voltage V_{DS1}. Transistor NM3 and NM5 provide the feedback to regulate the V_{DS1} over required voltage range. When TG_CLK goes high the current mirror is enabled and sinks constant current I_{COPY} from the capacitor. Transistors PM0 and PM1 are biased such that transistors NM2 and NM3 operate in saturation, when the mirror is active. Transistor NM1 is turned off and the mirror is disabled as soon as TG_CLK goes low.

Similar current mirror is designed using PMOS transistors to yield the current source that sources constant current to the capacitor whenever required.

B. Input Sampling Block

Fig. 2(a) shows the input sampling block. Transmission Gate switch is used to obtain full range input sampling. As shown in Fig. 2(b) stacked transistor transmission gate is utilized in the design to reduces the leakage current and improve the conversion accuracy [6]. The switch is designed so as to restrict the settling error of sampled voltage to less than half of the LSB. Transistor sizes are designed considering the short channel effect (SCE) and reverse short channel effect (RSCE) in MOS devices [7].

During input sampling switches TG3 and TG4 are enabled and voltage across capacitor is set to $V_{CM} - V_{IN}$. TG3 and TG4 are disabled for rest of the period except the sampling period. On the other hand TG5 is disabled during input sampling and enabled for rest of the period.

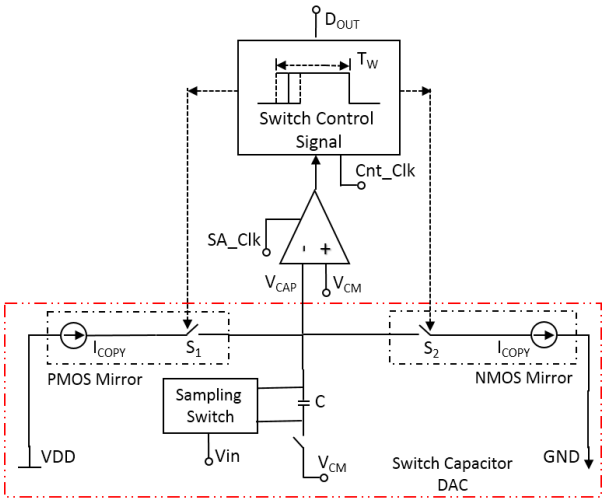

Figure 4. Switch-capacitor DAC ADC architecture.

This scheme allows keeping common mode voltage of comparator (V_{CM}) as threshold voltage to generate ADC output bits.

C. Comparator

Dynamic sense amplifier that combines high positive feedback with resistive input and the output latch which stores the digital output for one bit cycle is shown in Fig. 3. Output buffers are added to make output loading indistinguishable and obtain rail to rail output. The circuit converts small difference of current through input transistors to a large output voltage. During reset phase when CLK = 0V, output is set to VDD through reset transistors. Whereas during evaluation phase when CLK = 1V, the two cross coupled inverters initiate positive feedback and convert small input difference to large full scale value. For this type of ADC, offset voltage will affect the conversion accuracy and decrease the input voltage range, degrading the SNR of ADC. The transistor NM4 is made slightly wider to reduce the delay; while the PMOS transistors are designed to optimize the offset voltage of the comparator [8].

III. ADC Design and Architecture

Fig. 4 shows architecture of switch-capacitor DAC SAR ADC using regulated clocked current mirror. Analog part includes the charge/discharge current mirror, input sampling block that consists of transmission gate switches and a comparator. Digital control block that generates control pulses for current source/sink consists of counter, flip flop and switch control logic. Verilog A script has been written to build this digital control block and is interfaced with analog part of ADC.

The operation of 8-bit SAR ADC consists of total 10 cycles. First cycle is for sampling where the capacitor is pre-charged with value corresponding to input sample ($V_{CM} - V_{IN}$) and final one is for ADC output latch. Bit cycling is performed in remaining 8 cycles to generate 8 digital output bits, one bit per cycle. During the 1st-bit cycling, it is not required to charge or discharge the capacitor, only voltage across the capacitor V_{CAP} is compared with common mode voltage V_{CM} to generate the MSB bit.

In remaining 7 bit cycling, along with V_{CAP} and V_{CM} comparison, certain amount of voltage will be added to (charge) or subtracted from (discharge) the pre- charged voltage across the capacitor. If the comparator output in previous cycle is high (bit 1), charging is performed, and if it is low (bit 0) discharging is performed. The voltage across the capacitor can be controlled by controlling the charge (T_C) or discharge (T_D) period. This can be achieved by controlling ON/OFF period of switches S_1 & S_2 (Fig. 4). Charge operation is enabled by S_1 whereas discharge operation is enabled by S_2. Switches S_1 and S_2 work complementary to each other so that only one of them will be enabled in one cycle. Partial charge or discharge voltage corresponding to the switch control signal pulse width T_W can be obtained by,

$$\Delta V_{CAP} = \frac{I_{copy} \cdot T_W}{C} \quad (1)$$

$$\Delta V_{CAP} = \frac{V_{FS}}{2^{N-i}} \quad (2)$$

where V_{FS} is full-scale input voltage, I_{COPY} is constant reference current, T_W is the ON period of S_1 or S_2, C is the only capacitor in DAC circuit and N is number of resolution bits.

As SAR ADC employs binary search algorithm in feedback loop, the width T_W is reduced by half every bit cycle. Therefore, this simple charging and discharging circuit can be used as a DAC for SAR ADCs by combining the charge and discharge operation.

To obtain full range input conversion (0V to 1V) using a 7.7 pF capacitor and I_{COPY} of 2 µA, T_W for each cycle corresponding to required ΔV_{CAP} is as shown in Table I.

The period of each cycle is set to 1 µs (which is greater than the maximum T_W of 960 ns) leading to a sampling frequency of 100 kHz. Note that, the achievable minimum width T_W at a chosen value of current and the transient response of the current mirrors will limit the resolution of this ADC.

TABLE I. Change In Capacitor Voltage with Control Pulse Width (T_w) for Every Bit Cycle

Cycle Number	Output Code	ΔV_{CAP} (mV)	T_W (ns)
1	-	-	-
2	MSB (7^{th} Bit)	-	-
3	6^{th} Bit	250	960
4	5^{th} Bit	125	480
5	4^{th} Bit	62.5	240
6	3^{rd} Bit	31.25	120
7	2^{nd} Bit	15.62	60
8	1^{st} Bit	7.81	30
9	LSB (0^{th} Bit)	3.90	15
10	-	-	-

IV. Simulaton Results

This 8 bit, switch-capacitor DAC SAR ADC is designed in 90 nm CMOS and verified through circuit level simulations using cadence design tools.

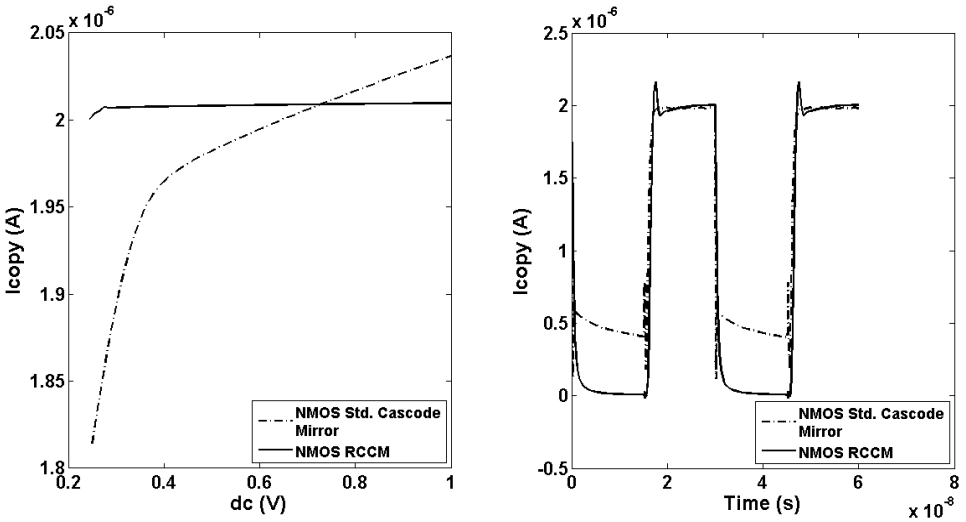

Figure 5. DC and transient analysis of standard NMOS Cascode mirror and NMOS regulated clocked current mirror..

Fig. 5 shows the comparison of standard NMOS cascode current mirror and NMOS RCCM. Both designed to sink constant current of 2 μA and are clocked at 33.33 MHz (frequency corresponding to lowest control signal pulse width T_W). Voltage at output (sinking) node is swept from 250mV to 1V to obtain the dc characteristics. It can be seen that RCCM performs far better than standard cascode current mirror. Variation of current with dc voltage is reduced to great extent while maintaining the good transient response.

To calculate DNL and INL error, slow ramp is applied at the ADC input. Fig. 6 shows the low frequency (near dc) DNL and INL error of ADC with respect to output code. The peak DNL error is +1.06/-0.40 LSB and peak INL error is +0.53/-1.33 LSB. Non linearity error is slightly high on positive side for DNL and on negative side for INL.

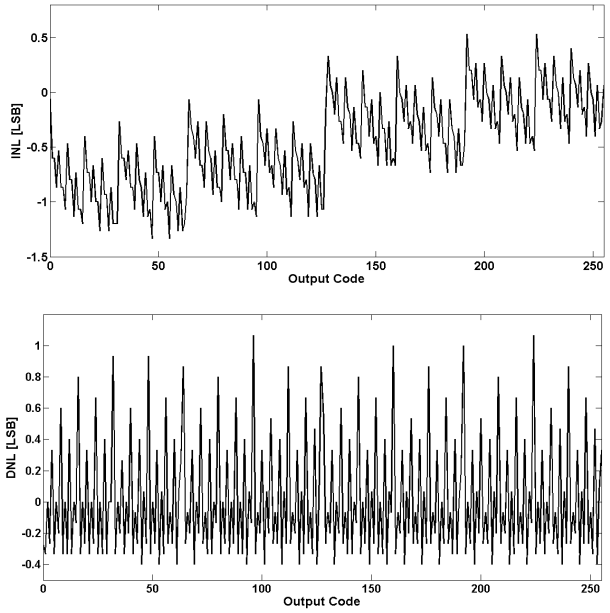

Figure 6. DNL and INL error.

Possible reasons for this could be offset voltage of comparator and channel charge injection in switch-capacitor DAC. At a supply voltage of 1V, the power dissipation in core ADC, when full scale sinusoidal near nyquist is applied at ADC input, is only 6 μW since the current flow across the capacitor is present only during the charging or discharging period. The typical low frequency FFT output spectrum at 1V supply, for full scale sinusoid input having dc offset of 0.5V and near nyquist frequency (44.63 kHz), sampling rate 100 kHz and 1024 sample points is shown in Fig. 7. The calculated SNDR is 45.62 dB providing effective number of bits (ENOB) of 7.3 bits.

Switch control signal and capacitor voltage V_{CAP} for minimum (0V) and maximum (1V) input are shown in Fig. 8. For every bit cycle, V_{CAP} varies proportionally with control signal which reduces to half of its value in previous cycle. For 1V input only the PMOS RCCM (switch S_1) is on which charges the capacitor, leading to a digital output of 11111111. On the other hand, for 0V input only the NMOS RCCM (switch S_2) is on which discharges the capacitor, leading to a digital output of 00000000. As observed V_{CAP} change for maximum input is exact mirror image of the V_{CAP} change for minimum input, which proves the working of pulse width to analog switch-capacitor DAC.

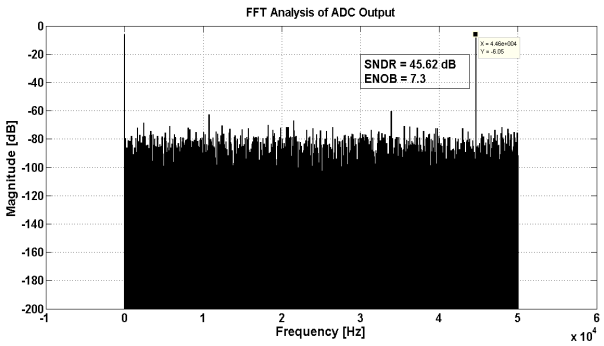

Figure 7. FFT Spectrum (1024 points) at 100 kS/s for input frequency of 44.63 kHz and supply voltage of 1V.

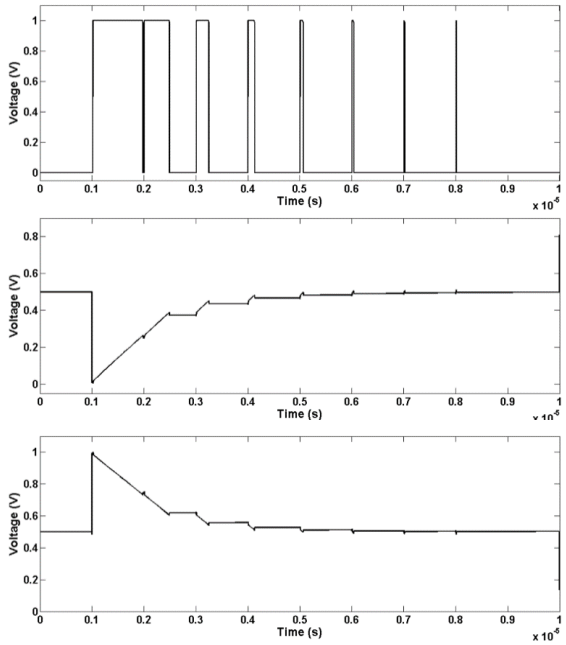

Figure 8. ADC Control Signal, V_{CAP} when V_{IN} = 1 and V_{IN} = 0.

Table II summarizes the performance of designed ADC.

TABLE II. ADC PERFORMANCE SUMMERY

Technology	90nm CMOS
Sampling Rate	100 KHz
DNL	+1.06 /-0.40 LSB
INL	+0.53 /-1.33 LSB
SNDR	45.62 dB
ENOB	7.3 Bits
Power	6 μW

V. CONCLUSION

In this paper, we have presented the design of 8 bit, switch-capacitor DAC successive approximation ADC in 90 nm CMOS technology using regulated clocked current mirror (RCCM). This is for the first time that a RCCM design has been introduced and used to build the SAR ADC. The RCCM works dynamically while providing constant current albeit the voltage variations at its output node. As only single capacitor has been used in the ADC design, this ADC can reduce the capacitor area and simplify switch control scheme to a great extent, regardless of its resolution. The ADC achieves SNDR of 45.62 dB, effective number of bits (ENOB) of 7.3 bits and a power consumption of 6 μW. Therefore, this ADC can have potential advantages in various MEMS sensor interface circuits where the layout area of ADC is to be kept small as compared to the MEMS components in the system.

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