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Multiple thickness gate oxides with fluorine implantation for system on chip applications

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ABSTRACT

Integrating digital, analog, I/O and memories onto a single chip is a great challenge to the design and process engineers. From the process engineers' point of view, integrating these modules with conflicting requirements needs a lot of innovation in the process technology. One such requirement is the need of having multiple gate oxide thickness on the same chip. Fluorine implantation of variable doses is explored to achieve this goal. It has been found that by varying the implanted dose of the fluorine in silicon, the oxidation rate and thereby the oxide thickness can be varied. The electrical characterization of the fluorine-implanted silicon based MOS structures using *C–V* and *J–E* measurements is reported here. It has been found that one can control the oxide thickness, interface properties and threshold voltage that could be vital in the SOC level integration.

1. Introduction

Driven by Moore's Law microelectronics has gone through many integration levels in the last many decades [1]. At present, the level of integration is such that it is not the integration of single function circuits on a chip but instead the integration of multi function circuits i.e. system on chip (SOC). In SOC, it is required to integrate various modules such as digital, analog, I/O, RAM and power management circuits etc [2]. In coming years, the challenge to the design and the process engineer will be to integrate not only the electronic modules but also the integration of mechanical parts in SOC constituting MEMS (Micro-Electro-Mechanical Systems) [3].

Integrating these diverse modules on the same chip is understandably a challenging task for technology. One such challenge is the ability to grow varying thicknesses of the gate dielectric films such as silicon dioxide on a single chip. Fukasaku et al. has reported triple gate technologies where a thin gate oxide is grown for the core logic and pass transistors, a thicker oxide for the lower power CMOS areas and an even more thicker gate oxide for the I/O modules [4]. Analog circuit requirements are very often conflicting with the digital circuit requirements [2]. All these demand the ability to grow the gate oxides of multiple thicknesses. Different techniques have been proposed to grow multiple gate oxide thicknesses in literature over the last many years [5–8]. One such technique is to grow the gate oxide throughout the water surface and etch back the gate oxide where thin oxides are required for masking the thicker oxide regions [5]. The advantage of this technique is that it can be easily implemented with the existing processing technology. However, such oxides may be contaminated during the etching and also sometime from the residual resist on the masked portions. Further, the repeated resist removal and etching may become infeasible as the integration level increases. SiO_2 and Si–O–N layers have been deposited by chemical vapor deposition (CVD) especially for the preparation of "stacked" oxide multilayers [7]. Such films may have improved dielectric reliability, but their application to ultra-thin gate dielectrics will be limited due to difficulties in controlling uniformity of dielectric layers across large areas. For altering the oxidation rate, the implantations of various ion species have been explored by various research groups [8]. Brian Doyle have demonstrated the retardation of oxidation rate of silicon using nitrogen implantation and proposed this method to grow multi-thickness gate oxides [5]. They have reported that oxides of 30–70 Å could be grown with a nitrogen implantation of doses in the range of 3×10^{14}–3×10^{15} ions/cm^2 [9,10]. Togo et al. proposed the implantation of argon and nitrogen for dual gate CMOS field-effect transistor in SOC fabrication [11]. Unlike nitrogen, argon implantation was found to enhance the oxidation rate [12]. The argon implantation at a dose of 1×10^{15} ions/cm^2 was found to increase the leakage current and the decrease in time to breakdown (T_{BD}). In the case of nitrogen

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implantation, it has been found that there is a trade off between the amount of nitrogen incorporation, which in turn decides the gate oxide thickness, and the gate oxide reliability. The higher implants doses of nitrogen give better thickness control but cause degradation of gate oxide reliability [13].

Hinriches and Preikszat [14] supports the previous results of Badawi and Anand [15]. Badawi and Anand attempted oxygen implantation and demonstrated that severe damages occur in the substrate, casting oxygen implantation as an unsuitable technique for forming gate oxides. However more recent studies have indicated that oxygen implantation could be used for sub-5 nm oxide technologies [16]. Enhancement in the oxidation rate due to different halogens (fluorine, iodine) and xenon species was compared for different oxidation and implant conditions [17,18]. Chlorine implantation in silicon has been found to enhance the oxidation rate and decrease the generation of stacking faults during thermal oxidation [19]. Fluorine-implanted silicon after annealing is expected to leave less residual damages due to its smaller size as compared to the other halogens. Not much attempt has been reported in the literature on fluorine implantation with a view of changing the oxide thickness for SOC applications.

Therefore, if the fluorine implantation alters the oxidation rate of silicon, then might be one of the possible applications in controlling the threshold voltage in addition to the channel doping. Woerlee et al. demonstrated the ultra-thin silicon on insulator (SOI) device behavior compared with that bulk device for a 0.5-μm CMOS technology. The most important deviations from bulk devices were a strong reduction of the breakdown voltage, enhanced hot carrier degradation, shift in threshold voltage as a function of gate length as well as stress time for SOI system. The main advantage of SOI seems to be the improved circuit properties and the simplified fabrication technology. However, for the high gate bias a negative differential output conductance was observed in NMOS/PMOS devices. This effect may be because of two possible origins; one is self-heating of the SOI devices and second is the change in charge state of trap levels near the drain for a drain bias above pinch off. Therefore, further work is needed to clarify the origin of this behavior of SOI devices for implementation in CMOS technology [20]. In the present work, the low energy fluorine ions have been implanted at varying doses to control the oxidation rate and thereby the thickness of the grown ultra-thin oxides. This technique could be used to grow multiple thickness gate oxides for SOC applications.

2. Experimental

RCA cleaned p-type silicon wafers of 10–30 Ω cm resistivity and <100> orientation were used for these experiments. The temperature–time cycle of furnace used for the oxidation to achieve a good thickness control and uniformity is shown in Fig. 1. One SLM (standard liter per minute) of oxygen was added to 19 SLM of nitrogen during ramping up to avoid the nitride micro-cluster formation. Wafers were loaded at 800 °C and furnace temperature was raised to 900 °C at a ramp rate of 10 °C/min up to 890 °C and at 3 °C/min to the final temperature as shown in Fig. 1. The thickness of oxide grown during this cycle was found to be 8.1 nm. After oxidation, wafers were spun coated with positive photoresist and masked to expose 3/4th part of wafer towards major flat. After developing, the wafers were dipped in 1:50 (40%HF + H_2O) for 20 s to etch oxide from 3/4th part of wafer.

The pre-grown oxide portion and the portion where no implantation was to be made were masked with photoresist. The unmasked portions were implanted with $^{19}F^{+}$ at a dose of 1×10^{14} ions/cm^2 (implant-1) at 10 keV. The 3/4th portion (pre-grown oxide layer + the un-implanted and a portion implanted

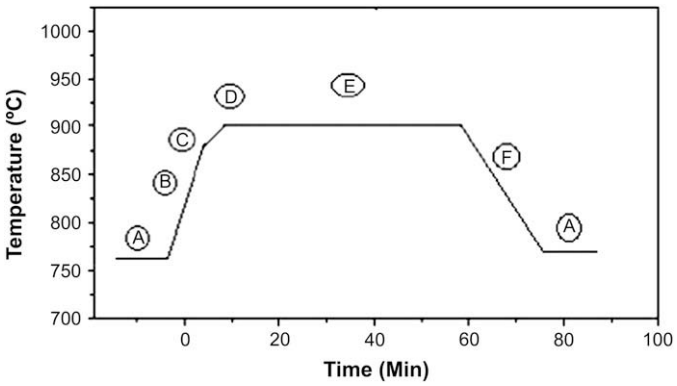

Fig. 1. Details of furnace oxidation annealing cycles. A: standby temperature, B: 10 °C/min heating ramp-1, C: 3 °C/min heating ramp-2, D: 1 °C/min heating ramp-3, E: annealing cycle, F: 10 °C/min cooling ramp.

with 1×10^{14} ions/cm^2 dose) of the wafers were masked. The unmasked 1/4th portions were implanted with $^{19}F^{+}$ at a dose of 2×10^{14} ions/cm^2 (implant-2). Thus the wafers were split into four sets – pre-grown, un-implanted, implanted with $^{19}F^{+}$ at 1×10^{14} ions/cm^2 dose (low dose), implanted with $^{19}F^{+}$ at 3×10^{14} ions/cm^2 dose (high dose) at 10 keV as shown in Fig. 2. Then oxidation was carried out in the furnace at 900 °C for 5 min and obtained thicknesses of 1.9 nm, 2.2 nm and 2.5 nm as measured using Rudolf Research's Ellipsometer (Auto EL-III). After the removal of the backside oxide, a thick layer of aluminum film was deposited for back contact. In the front side, gate electrodes of 100 μm × 100 μm area were patterned using photolithography and wet etching technique. Aluminum metal films for front and back contacts were deposited using DC sputtering. The MOS capacitors thus obtained were electrically characterized at room temperature by capacitance–voltage (C–V) at 1 MHz frequency and current–voltage (I–V) measurements using a Keithley 590C-V Analyzer, 230 Voltage Source and 617 programmable electrometer.

3. Results and discussions

Fig. 3 indicates the C–V characteristics of MOS devices measured for pre-grown and for oxide films grown on p-type silicon before and after fluorine implantation at a dose of 1×10^{14} and 3×10^{14} ions/cm^2 respectively. The gate voltage was swept from inversion to accumulation [+5 V to −5 V] during these measurements. For pre-grown oxide of 8.1 nm, C–V characteristics of MOS device show that the maximum and minimum values of capacitance are approximately 46 pF and 1.5 pF. In the case of un-implanted region with an oxide thickness of 2 nm, the maximum and minimum values of capacitance are 165 pF and 0.7 pF

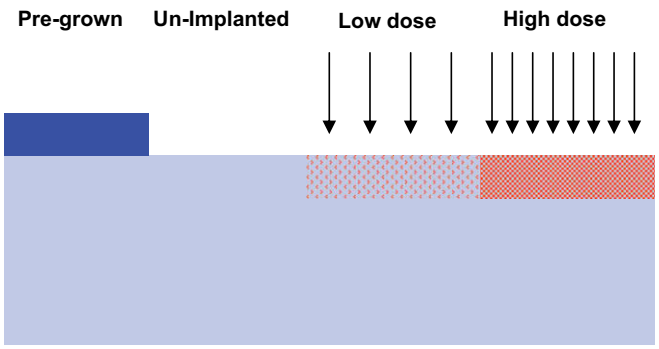

Fig. 2. Cross-sectional view of the wafers implanted with different fluorine doses.

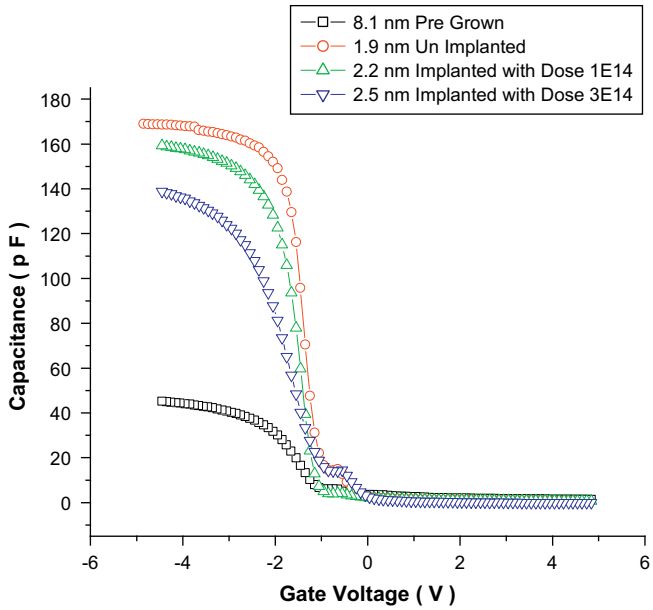

Fig. 3. *C–V* characteristics of MOS devices measured at 1 MHz for pre-grown and oxide films grown on p-type silicon before and after fluorine implantation at the doses 1×10^{14} ions/cm^2 and 3×10^{14} ions/cm^2.

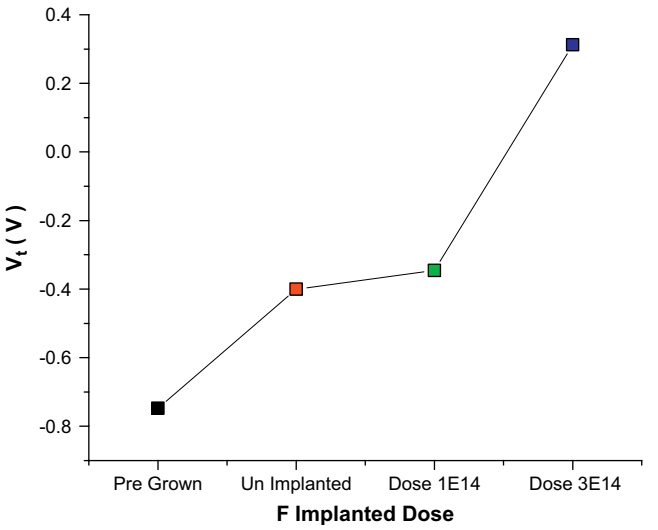

Fig. 4. Threshold voltage (V_t) variation for pre-grown, un-implanted, implanted with low and high fluorine ions implantation dose for MOS structure.

respectively. *C–V* characteristics of MOS device for low dose fluorine-implanted silicon grown oxide of 2.2 nm thickness indicate that the maximum and minimum values of the capacitance are 158 pF and 1.1 pF respectively. The same for high dose fluorine-implanted silicon based grown oxide of thickness 2.5 nm shows that the maximum and minimum values of the capacitance are 138 pF and 1 pF respectively. The different values of capacitances for these samples may be attributed to the difference in oxide thickness or due to a possible change in the dielectric constant of grown oxide due to the incorporation of fluorine. However, the second possibility was ruled out by measuring the oxide thickness using ellipsometry [18]. Table 1 compares the oxide thickness measured from the ellipsometry and obtained using the *C–V* measurements. The results clearly indicate that within the experimental error, the measured thicknesses are same. So, we conclude that the change in capacitance is due to the change in oxide thickness rather than due to the change in the dielectric constant. This clearly indicates that the oxidation rate has increased after fluorine implantation. However, the energy losses because of low energy $^{19}F^{+}$ ions implanted within the silicon substrate at 10 keV were estimated by simulated TRIM (Transport of Ions in Matter). The corresponding electronic and nuclear losses were 3.3506×10^{-1}, 9.245×10^{-1} MeV/(mg/cm^2) respectively, which has maximum simulated projected range 24.9 nm and longitudinal straggling 13.8 nm [21]. Thus, the fluorine ions were distributed in more deep regions in the silicon substrate. Therefore, the degree of damage becomes lesser per unit area as lighter ions move deeper in the silicon, yet decrease in oxidation rate is less as compared to the increase in straggle. However, $^{19}F^{+}$ ions are lighter in nature and hence they can easily diffuse out from the Si–Si network and acts as network terminator. This mechanism of fluorine ions distribution within the silicon leads to the maximum damage closer to the surface than distribution of ions itself, which results in the enhancement of oxidation rate. Therefore, low energy fluorine ion implantation enhance the oxidation rate of silicon. It results multiple ultra-thin gate oxides thickness with differential capacitance for SOC system.

Capacitance–voltage (*C–V*) curve of MOS based on pre-grown oxide indicates a flat band voltage (V_{FB}) shift of 1.7 V along the negative voltage axis indicating the presence of high density of fixed positive charges (+Q) in the pre-grown silicon oxide film. Un-implanted region shows the flat band voltage shift of 1.3 V along the negative axis. The pre-grown SiO_2 layer was etched using HF based etchant. This treatment forms Si–F (silicon-fluorine) network as previously observed by Kasi et al. [22] and results in a significant shift of the flat band (V_{FB}) voltage due to the reduction of fixed oxide charges within the thin dielectric films. After low energy (10 keV) fluorine ions implantation at 1×10^{14} and 3×10^{14} ions/cm^2 doses, the flat band voltage has been shifted by 1.2 V and 0.2 V respectively along the negative voltage axis. So a flat band voltage shift of 1.5 V from pre-grown oxides to the fluorine-implanted gate oxides indicates the flexibility of altering the flat band voltage (V_{FB}) with low energy fluorine ion implantation. Similar results have also been reported by Perera Rohana [23] and were attributed to the reduction of the positive charges in the thin oxides.

Table 1
Measured parameters of MOS devices with ultra-thin SiO_2.

Parameters	Wafers oxidized at 900 °C for 5 min			
	Samples			
	Pre-grown	Un-implanted	Dose 1×10^{14} ions/cm^2	Dose 3×10^{14} ions/cm^2
Oxide thickness measured by *C–V* (nm)	8.3	2.0	2.3	2.7
Oxide thickness measured by ellipsometer (nm)	8.1	1.9	2.2	2.5
Threshold voltage [V_t] (V)	−0.74	−0.40	−0.34	0.3
Effective oxide charges [Q_{EFF}] (C/cm^2)	5.9	5.0	3.8	−7.7
Interface state density [D_{it}] (1/cm^{2}eV)	1.6×10^{13}	8.1×10^{12}	9.2×10^{11}	1.1×10^{11}

As indicated in the Fig. 4, there is a significant change in the threshold voltage (V_t) of pre-grown, un-implanted and fluorine-implanted samples. There could be fixed positive charges within the pre-grown oxide and the incorporation of fluorine is expected to compensate the fixed positive charges and hence results in the change of threshold voltage. Even in the case of un-implanted samples, there could be significant fluorine incorporation due to HF treatment [24]. The threshold voltage (V_t) is calculated by the following relation:

$$V_t = \left[\pm \frac{A}{10^{12} C_{ox}} \sqrt{4\varepsilon_s q |N_{BULK}||\phi_B|} + 2|\phi_B| \right] + V_{FB}$$

Here V_t, C_{ox}, ϕ_B, V_{FB}, ε_s, q, N_{BULK} and A are threshold voltage, oxide capacitance, bulk potential, flat band voltage, permittivity of silicon, electronic charge, bulk doping concentration and electrode area respectively [25].

Further, Fig. 5 shows the effective oxide charge (Q_{EFF}) variation with the fluorine incorporation [26]. The effective oxide charge is calculated by the relation:

$$Q_{EFF} = \frac{C_{ox}(W_{MS} - V_{FB})}{A}$$

Here Q_{EFF}, C_{ox}, W_{MS}, V_{FB} and A are effective oxide charges, oxide capacitance, metal semiconductor work function difference, flat band voltage and electrode area respectively. There is a decrease in the effective oxide charge due to fluorine incorporation in the oxide. The shift in the flat band voltage in the positive direction with fluorine ion implantation and reduction in the oxide charges implies that fluorine implantation contributes negative charges. Maegawa et al. have reported the similar behavior of fluorine ion implantation in gate oxides [24].

Fig. 6 shows the gate leakage current density of MOS capacitors, as a function of gate electric field (E). As evident from the figure, there is significant reduction in the gate leakage current with the electric field for increased dose of fluorine ions. It is attributed to the reduction of the gate oxides defects [27]. Fig. 7 shows the distribution of interface state density (D_{it}) in the Si band gap before and after fluorine incorporation within the oxide. The interface trap density vs. energy curve examines the trap densities near the mid gap (E_t). The interface trap energy from mid gap, E_t, is measured as the difference of silicon surface potential (ψ_s) and bulk potential (Φ_B) [28]. The interface trap

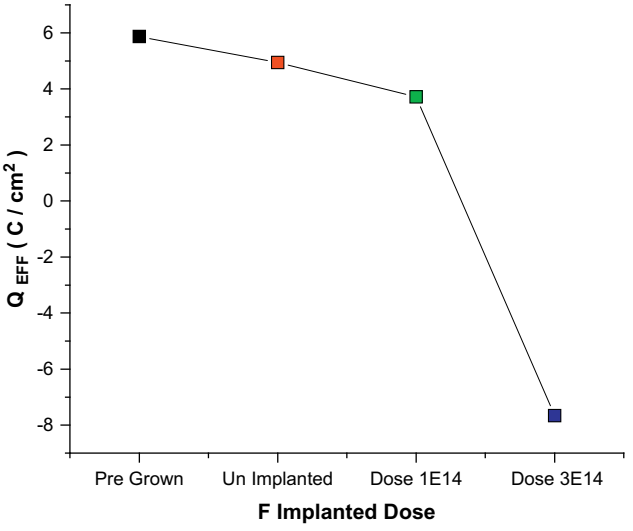

Fig. 5. Effective oxide charges (Q_{EFF}) variation for pre-grown, un-implanted, implanted with low and high fluorine ions implantation dose for MOS structure.

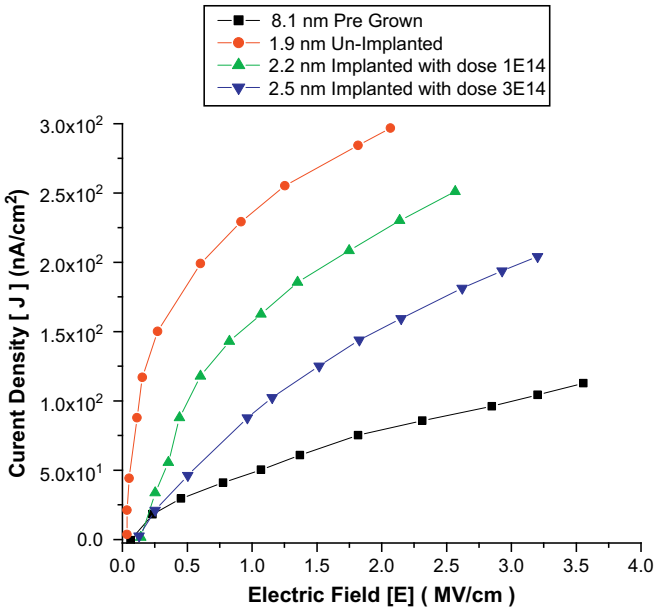

Fig. 6. Gate leakage current density (J) vs. gate voltage for pre-grown, un-implanted, implanted with low and high fluorine ions implantation dose for MOS structure.

density (D_{it}) is calculated from the interface state capacitance (C_{it}) using the following relation:

$$D_{it} = \frac{\left(1 \times 10^{-12}\right) C_{it}}{Aq}$$

and C_{it} is given by

$$C_{it} = \left[\frac{1}{C_q} - \frac{1}{C_{ox}}\right]^{-1} - \left[\frac{1}{C_H} - \frac{1}{C_{ox}}\right]^{-1}$$

where C_q, C_H, D_{it} and A are quasi-static capacitance, high frequency capacitance, interface state density and electrode area respectively. C_q and C_H are obtained from C–V data experimentally. The interface trap density of fluorine ion-implanted samples was less than that of un-implanted oxides samples as shown in Table 1. This

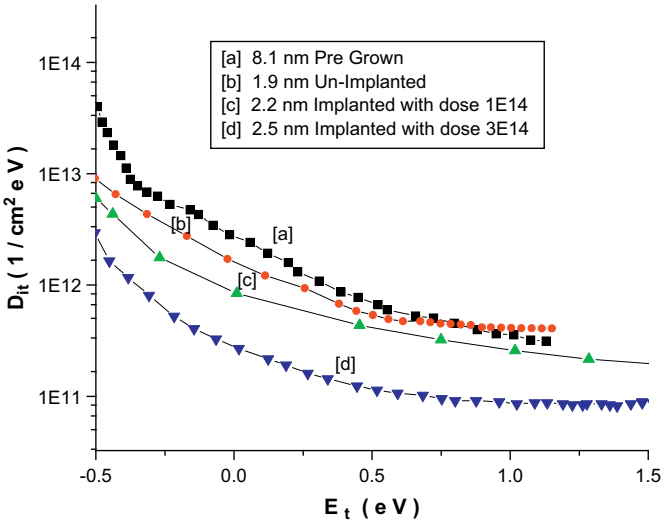

Fig. 7. The interface state density (D_{it}) vs. energy from mid gap (E_t) at Si/SiO_2 interface of pre-grown, un-implanted, implanted with low fluorine dose and higher dose for MOS structure.

measurement also implies the improvement in oxide quality due to the reduction of interface state density by two orders of magnitude.

4. Conclusion

This paper describes a novel technique to grow the ultra-thin multiple gate oxides using low energy fluorine ion implantation for SOC technologies. It is found that the oxidation rate increases with fluorine ion dose. The threshold voltage has been found to vary with the dose, which could have possible applications in controlling the threshold voltage. There is a marked improvement in the quality of gate oxide as shown by the results of effective oxide charges, gate leakage current and the interface trap density. So, fluorine implantation could be a useful alternate technique of growing varying oxide thicknesses especially ultra-thin oxides for SOC technology.

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