Effect of electrical stress on Au/Pb (Zr\textsubscript{0.52}Ti\textsubscript{0.48}) O\textsubscript{3}/TiO\textsubscript{x}N\textsubscript{y}/Si gate stack for reliability analysis of ferroelectric field effect transistors

Cite as: Appl. Phys. Lett. 105, 152907 (2014); https://doi.org/10.1063/1.4897952
Submitted: 08 July 2014 . Accepted: 27 September 2014 . Published Online: 16 October 2014

Robin Khosla, Deepak K. Sharma, Kunal Mondal, and Satinder K. Sharma

ARTICLES YOU MAY BE INTERESTED IN

Frequency dispersion and dielectric relaxation in postdeposition annealed high-κ erbium oxide metal–oxide–semiconductor capacitors
Journal of Vacuum Science & Technology B 36, 012201 (2018); https://doi.org/10.1116/1.4995809

Ferroelectricity in hafnium oxide thin films

High performance Au/PZT/TiO\textsubscript{x}N\textsubscript{y}/Si MFIS structure for next generation ferroelectric memory applications
AIP Conference Proceedings 1661, 060007 (2015); https://doi.org/10.1063/1.4915377
Effect of electrical stress on Au/Pb (Zr0.52Ti0.48) O3/TiOxNy/Si gate stack for reliability analysis of ferroelectric field effect transistors

Robin Khosla,1 Deepak K. Sharma,1 Kunal Mondal,2 and Satinder K. Sharma1
1School of Computing and Electrical Engineering, Indian Institute of Technology (IIT), Mandi 175001, India
2Department of Chemical Engineering, Indian Institute of Technology (IIT), Kanpur 208016, India

(Received 8 July 2014; accepted 27 September 2014; published online 16 October 2014)

Metal-Ferroelectric-Insulator-Semiconductor (MFIS) structure with 20 nm thin lead zirconate titanate (PZT) ferroelectric film and 6 nm ultrathin high-κ titanium oxynitride (TiOxNy) insulator layer on p-Si substrate were fabricated. Effect of constant voltage stress (CVS) on electrical characteristics of MFIS structure was investigated to study the reliability of fabricated devices. The experimental results showed trivial variation in memory window (ΔW) from 1.05 to 1 V under CVS of 0 to 15 V (5.76 MV/cm) at sweep voltage of ±5 V. Also, leakage current density (J) reduced from 5.57 to 1.94 μA/cm2 under CVS of 5.76 MV/cm, supported by energy band diagram. It signifies highly reliable TiOxNy buffer layer for Ferroelectric Random Access Memory. After programming at ±5 V, the high (C_H) and low (C_L) capacitances reliability remains distinguishable for 5000 s even if we extrapolate measured data to 15 years. Microstructures analysis of XRD reveals the formation of (100) and (111) orientation of PZT and TiOxNy, respectively. Thus, Au/PZT/TiOxNy/Si, MFIS gate stacks can be potential candidate for next generation reliable Ferroelectric Field Effect Transistors. © 2014 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4897952]

Non-Volatile memories are classified into charge storage memories NAND, NOR FLASH and non-charge storage memories Ferroelectric Random Access Memory (FeRAM), Magnetic RAM (MRAM), Phase Change RAM (PCRAM), and Resistive RAM (ReRAM). The next generation scaling of charge storage devices in sub-nano-metric regime is hampered by availability of inadequate number of electrons. Therefore, the memory devices with memory states, but devoid of charges, are prospective contenders for next technology node.1 In recent years, FeRAM has attracted much attention due to its fast access time, low power consumption, high security, excellent retention, and endurance time.2 Current commercial applications of FeRAM include Radio-Frequency Identification (RFID) card, Identity (ID) card, smart card, and various other low density embedded applications.1 The performance of ferroelectric field effect transistors (FeFET) with metal-ferroelectric-semiconductor (MFS) structure is hampered by interdiffusion and interface reaction between silicon substrate and ferroelectric thin film. This degrades the device performance resulting in process integration problems and degradation of retention time.3–9 This problem was resolved by depositing an insulating layer between silicon substrate and ferroelectric thin film forming MFIS structure, which results in improved retention time.10–12 The insulating material for this structure should have relatively high dielectric constant, good interface with silicon substrate, low leakage, and good thermal stability.13,14 While, ferroelectric materials in aforesaid structure should have high-κ, low leakage, long data retention time, high Pr value, low Ec, and low crystallization temperature.13,14 Numerous attempts have been made to make FeRAM using ZrO2,3,15 HfO2,5,16,17 Al2O3,18 Y2O3,12,18 Dy2O3,19 MgO,20 La2O3,21 TiO2,22 and TiAlO223 as insulator and Pb(Zr0.52Ti0.48)O3 (PZT),9,18–21 SrBiTaO6 (SBT),2 BiFeO3,3,12 as ferroelectric material in MFIS structures. However, there is very limited work on MFIS structure with thin ferroelectric films thinner than 60 nm. Recently, the ability to engineer ferroelectricity in HfO2 (10 nm)24 has motivated the scientific community to scale FeRAM further, but this 1T-1C structure requires separate switching (1T) and storage circuit (1C), hence demands additional area as compared to 1T-MFIS structure.3 Moreover, the 10 nm Si-doped HfO2 in MFIS structure was also investigated but showed a much lower fatigue of ~104 cycles25,26 as compared to PZT. In fact for FeRAM to be the strong candidate for future universal memory,2 it is necessary to accomplish the high density projected goals for next generation FeRAM technology node.1 Thus, it becomes imperative to study the characteristics of MFIS structures with thin ferroelectric layers and ultrathin buffer layers for next technology node. However, the ferroelectric materials are unfamiliar and might be degraded by the conventional CMOS processing. Thus, the buffer, ferroelectric materials, and device processing conditions for FeRAM are still being refined.1

Recently, metal-ferroelectric-nitride-semiconductor (MFNS) structure showed its strong candidature for FeRAM device applications as compared to metal-ferroelectric-oxide-semiconductor (MFOS) structure.27 However to achieve future scaling, nitride layer must be replaced by a high-κ dielectric. Formerly, TiOxNy films showed higher resistance to interfacial oxide formation, an excellent diffusion barrier28,29 and high dielectric constant, which allows proportionally higher voltages to be applied across ferroelectric layer.19 Still, there is very limited effort on the investigation of ultrathin (~6 nm) TiOxNy as an alternate buffer material and thin (~20 nm) PZT layers in MFIS structure for next generation FeRAM device applications to the best of authors knowledge. High dielectric constant, high Pr value, and low crystallization temperature of PZT make it suitable for FeRAM application as compared to other ferroelectrics.13 MFIS structures with BFO(250 nm)/TiO2(150 nm),30 SBT(300 nm)/
HfO$_2$(6 nm),$^5$ and PZT(160 nm)/La$_2$O$_3$(16 nm)$^{21}$ have been reported with $\Delta W$ of 0.5 V at $\pm 5$ V, 1.1 V at $\pm 5$ V, 0.65 V at $-2$ to $+6$ V, and 0.7 V at $\pm 7$ V, respectively. The leakage current density ($J$) reported in BFO(250 nm)/TiO$_2$(150 nm)$^{30}$ is of order $10^{-7}$A/cm$^2$ at $+5$ V. The most advanced MFIS structure till date is Metal/SBT(300 nm)/HfO$_2$(6 nm)/Si with $\Delta W$ of 0.65 V at $-2$ to $+6$ V cyclic sweep and 10 years extrapolated retention time.$^5$ Previous experimental results show that stress$^{31}$ has significant effect on polarization of ferroelectrics.$^{17}$ Thus, it becomes necessary to study the behaviour of MFIS structures under CVS to check reliability of FeRAM devices especially at lower ferroelectric and buffer layer thicknesses. In this letter, first time employed ultrathin 6 nm TiO$_x$N$_y$ as buffer and thin 20 nm PZT as ferroelectric films were chosen for fabrication of MFIS structure of FeRAM deposited by RF magnetron sputtering. The $\Delta W$, retention analysis, and $J$, of fabricated devices were investigated with and without stress by Capacitance-Voltage (C-V), Capacitance-Time (C-T), and Leakage Current Density-Voltage (J-V) characteristics, respectively, supported by proposed model. The crystallinity of deposited ultrathin and thin films was analyzed by X-ray diffraction (XRD).

The MFIS capacitors were fabricated on 2-in. P-type (100) oriented silicon wafers (1–10 $\Omega$ cm). After standard RCA cleaning, deposition of TiO$_x$N$_y$ films was carried out by radio frequency (RF) magnetron sputtering at RF power 90 W, 3.9 x 10$^{-2}$ Torr, pressure of Ar/N$_2$ (60:19 sccm), and temperature of 300 K. These ultrathin films of TiO$_x$N$_y$ deposited Si wafers were annealed at 873 K for 30 min in N$_2$ ambient. Subsequently, the deposition of PZT thin films was followed by RF magnetron sputtering at RF power 120 W, 1.8 x 10$^{-2}$ Torr pressure of Ar and temperature of 300 K. The PZT deposited samples were annealed at 973 K for 60 min in inert ambient. For gate electrodes, Au thin film (~100 nm) was deposited by RF magnetron sputtering at 3.9 x 10$^{-2}$ Torr pressure of Ar and gate electrodes of area 3.85 x 10$^{-3}$ cm$^2$ are patterned through the standard photolithography and chemically etching techniques. The thickness of deposited TiO$_x$N$_y$ and PZT thin films was measured by Accurion EP3 imaging ellipsometer. The C-V, C-T, and J-V, without and with CVS were carried out at room temperature using KEITHLEY 4200 SCS system. The C-V characteristics are taken at 1 MHz frequency and 0.01 V/s sweep rate. The orientations and crystallinity of the deposited thin films were analyzed using XRD with Cu-K$_\alpha$ radiation.

Figure 1: The cyclic C-V characteristics of Au/PZT (20 nm)/TiO$_x$N$_y$ (6 nm)/Si, MFIS structures at different stress voltages. Inset shows C-V characteristics of Au/PZT (20 nm)/TiO$_x$N$_y$ (6 nm)/Si (MFIS) devices at different frequencies (a) and at different sweep rates (b).

![Image](image_url)

FIG. 1. Normalized C-V characteristics of Au/PZT (20 nm)/TiO$_x$N$_y$ (6 nm)/Si, (MFIS) structure at different stress voltages. Inset shows C-V characteristics of Au/PZT (20 nm)/TiO$_x$N$_y$ (6 nm)/Si (MFIS) devices at different frequencies (a) and at different sweep rates (b).

The experimental memory window width is close to the theoretical results obtained from

$$\Delta W \approx 2d_fE_C - \Delta V_{FB,ci},$$

(1)

where $d_f$ is the thickness of PZT, $E_C$ is the coercive electric field, and $\Delta V_{FB,ci}$ is flat band voltage shift caused by charge injection. The voltage drop across ferroelectric is given by

$$\frac{V_f}{V_i} = \frac{D_f}{D_i},$$

(2)

where $V_f$, $V_i$ are the voltage across ferroelectric and insulator, respectively. $D_f$, $\varepsilon_f$, and $D_i$, $\varepsilon_i$ are the thickness, dielectric constant of ferroelectric and insulator thin films, respectively. The calculated $\Delta W$ (~1.05 V) of fabricated devices with PZT(20 nm)/TiO$_x$N$_y$(6 nm) is certainly comparable to 1.1 V with BFO(250 nm)/TiO$_2$(150 nm) reported by Xie et al.$^{30}$ at ±6 V sweep voltage. The $V_{fb}$ of FeRAM memory calculated for forward $-5$ to $+5$ V gate voltage sweep along with external stress voltage of 0, 5, 10, and 15 V are 0.55, 0.68, 0.70, and 0.80 V, respectively. There is insignificant variation in $V_{fb}$ (~0.25 V) noticed under CVS as shown at (i) and (j) of Figure 1. This shift in $V_{fb}$ as a result of CVS may be attributing to the presence of fairly significant number of defects at the TiO$_x$N$_y$/Si interface. Additionally, the cyclic C-V hysteresis curves at (i) and (j) of Figure 1 show the variation of FeRAM memory window ($\Delta W$) ~0.05 V with increase in stress voltage from 0 to 15 V. The observed variation in hysteresis may be attributed to the trapping and de-trapping mechanism at the TiO$_x$N$_y$/Si system and not due to dielectric polarization or ionic displacement (e.g., Na$^+$, K$^+$, etc.).$^{32}$ When the gate voltage approaches the weak inversion region, de-trapping of the trapped charges occurs by charge exchange with the Si substrate. The proposed structure at the weak inversion does not favour strong intrinsic trapping sites in TiO$_x$N$_y$ of TiO$_2$/Si system. However, the amount of charge de-trapped at TiO$_x$N$_y$ should be sufficient to cause the shift in $V_{fb}$ as observed in the curve after CVS as depicted in the cyclic C-V curve at (i) and (j) of Figure 1. Therefore, the
reduction in memory window after CVS indicates the reduction in traps at the Si/TiOxNy system. Further, there is an interesting hump noticed in all reversed C-V curves as shown at (k) in Figure 1, signifying the strong de-trapping of intrinsic trapped charges of TiOxNy/Si structure during reverse sweep. As conveyed by the C-V curves, this hump vanishes after CVS. It indicates the traps at TiOxNy/Si system get reduced upon increasing the CVS. The interface traps, mobile ions, bulk traps, and impurities in high-κ layer can also cause charge effect and hence hysteresis in C-V curves. Thus, frequency dependent measurements are performed on Au/PZT(20 nm)/TiOxNy(6 nm)/Si, MFIS structure as shown in Figure 2 that signify the strong de-trapping of intrinsic trapped charges and interfacial polarization on hysteresis, memory window shows an insignificant change with frequency variation from 0.1 MHz to 1 MHz. Thus, memory window is due to polarization of PZT thin films and not due to interface traps. To confirm the effect of mobile ionic charges and interfacial polarization on hysteresis, memory window is observed with variation in sweep voltage from 0.01 to 0.1 V/s. The inset (b) of Figure 1 shows the C−V characteristics of FeRAM devices with Au/PZT(20 nm)/TiOxNy(6 nm)/Si, MFIS structure with different sweep rates. The memory window of Au/PZT(20 nm)/TiOxNy(6 nm)/Si, MFIS structure remains consistent around ~1 V regardless of variation in sweeping speed. This confirms that memory window is primarily determined by the ferroelectric polarization of PZT thin film and other factors have minor impact.

For real FeRAM device applications, it is essential to check retention time behaviour of FeRAM MFIS structures. Figure 2 shows the retention characteristics of Au/PZT(20 nm)/TiOxNy(6 nm)/Si, FeRAM MFIS structures, characterized through the C−T analysis. The inset of Figure 2 shows the experimental data in linear time scale. In this systematic investigation, the proposed MFIS device is applied a write pulse of ±5 V in height and 100 ms in duration, followed by a read voltage near flatband voltage of 1.5 V. Here, the write pulse of −5 V corresponds to CH and that of +5 V correspond to CL. For the first 1000 s, exponential decay and rise was observed in CH and CL, respectively. After this, the capacitance values decay linearly w.r.t time. Thus, linear extrapolation is done after 1000 s. As shown in Figure 2, the difference in capacitance magnitudes (ΔC = C_H − C_L) is evidently distinguishable for 5000 s even if we extrapolate the experimental data to 15 years, which is desired for next generation non-volatile memories. It is clearly seen in inset of Figure 2 that the slope of CH (Figure 2(a)) becomes positive and CL (Figure 2(b)) becomes negative, i.e., ΔC increases under CVS, hence result in improvement of retention time of FeRAM devices, which is in agreement with the leakage current density results with CVS shown in Figure 3.

Figure 3 shows the gate leakage current density (J) as a function of gate sweep voltage (V_g). The low leakage current density (J) of 55.7 × 10^7 A/cm² of fabricated devices with 6 nm TiOxNy is greatly superior to 150 nm TiO2 reported by Xie et al. with J of order 10^7 A/cm² at +5 V sweep voltage. The measured gate leakage current for Au/PZT(20 nm)/TiOxNy(6 nm)/Si, FeRAM MFIS structures at dc voltage of 5 V along with stress voltage of 0, 5, 10, and 15 V are 5.57, 2.41, 2.22, and 1.94 μA/cm², respectively. It is apparent that with the variation in stress voltage from 0 to 15 V, there is an enduring reduction in gate leakage current by a factor 3.63 μA/cm², which is probably because of decrease in the intrinsic trapping sites in TiOxNy of TiOxNy/Si system. Clogging of neutral defects may result in deep trap so that electrons are no longer available for conduction. This considerable higher strength to stress voltage is an indication of the elevated reliability and feasibility to use Au/PZT(20 nm)/TiOxNy(6 nm)/Si, MFIS structures for FeRAM device applications.

Figure 4(a) shows the XRD pattern of ultrathin TiOxNy films deposited on Si, followed by annealing at 873 K. The TiOxNy thin films exhibited a high (111) orientation with relatively small (220), (304), and (400) peaks. The most stable tetragonal rutile phase of TiO2 (110) is also observed along with small peak of anatase TiO2 (111). Figure 4(b) shows the XRD pattern of PZT-Si structure annealed at 873 K, which confirms the presence of perovskite phase of PZT film, which is one of prime importance for the excellent remanent polarization. The PZT thin film exhibited (100) along with (220) preferred orientation, which are the best phases for good fatigue endurance and higher remanent polarization,
respectively, along with relatively small (110), (111) peaks. Figure 5 shows the energy band diagram of Au/PZT(20 nm)/TiOxNy(6 nm)/Si, MFIS structure, using the work function of Au as 5.1 eV, PZT electron affinity as 2.15 V, PZT energy band gap as 3.4 V and assuming the TiOxNy energy band gap as 2 eV. In Figure 5(a), when $V_g < 0$, device is in accumulation and traps are occupied in TiOxNy due to stress voltage. In Figure 5(b), when $V_g > 0$, device is in onset of inversion region with small barrier height at TiOxNy/Si interface. The charge carriers trapped in TiOxNy result in the decrease of J with increase of stress due to decrease in intrinsic trapping sites in TiOxNy of TiOxNy/Si system and clogging of oxide neutral traps, which do not participate in conduction.

In Summary, MFIS-structure of FeRAM was fabricated using ultrathin 6 nm TiOxNy buffer and thin 20 nm PZT ferroelectric films on p-Si by RF-magnetron sputtering and annealed in N2 ambient. The electrical characteristics of fabricated devices were analyzed under CVS to test their reliability. It is shown that with the variation in CVS from 0 to 15 V, there is trivial alteration in $V_{fb}$ and $D_W$ showed insignificant variation in C-V characteristics with variation in frequency and sweep rate. This signified the excellent TiOxNy/Si interface and confirms that memory window is due to polarization of PZT thin films and other factors like interface traps, mobile ions have minor impact. The reduction in gate leakage current by a factor of 3.63 $\mu$A/cm$^2$ under CVS suggests the decrease in intrinsic trapping sites and clogging of neutral defects in TiOxNy and hence the improvement of retention characteristics of fabricated Au/PZT(20 nm)/TiOxNy(6 nm)/Si, MFIS FeRAM devices extrapolated beyond 15 years. Thus, MFIS FeRAM gate stacks with TiOxNy as buffer layer and PZT as ferroelectric layer is a potential candidate for long retention FeFET.

The authors are grateful to Professor Ashutosh Sharma, Department of Chemical Engineering, Indian Institute of Technology (IIT)-Kanpur, for the use of samples preparation facility at NanoSciences, IIT-Kanpur, India.

30D. Xie, X. Han, R. Li, T. Ren, L. Liu, and Y. Zhao, Appl. Phys. Lett. 97, 172901 (2010).