

Contents lists available at ScienceDirect

Microelectronics Journal



journal homepage: www.elsevier.com/locate/mejo

An 8 bit, 100 kS/s, switch-capacitor DAC SAR ADC for RFID applications



Ashish Joshi^{a,*}, S.K. Manhas^b, Satinder K. Sharma^a, S. Dasgupta^b

^a School of Computing and Electrical Engineering, Indian Institute of Technology (IIT) Mandi, Mandi, Himachal Pradesh 175001, India. ^b Electronics and Communication Engineering, Indian Institute of Technology (IIT) Roorkee, Roorkee, Uttarakhand, India.

ARTICLE INFO

Article history: Received 23 April 2014 Received in revised form 2 January 2015 Accepted 18 March 2015 Available online 13 April 2015

Keywords: Regulated dynamic current mirror (RDCM) SAR ADC Switch-capacitor DAC

ABSTRACT

An 8 bit switch-capacitor DAC successive approximation analog to digital converter (SAR-ADC) for sensor-RFID application is presented in this paper. To achieve minimum chip area, maximum simplicity is imposed on capacitive DAC; replacing capacitor bank with only a one switch-capacitor circuit. The regulated dynamic current mirror (RDCM) design is introduced to provide stabilized current. This invariable current from RDCM, charging or discharging the only capacitor in circuit is controlled by pulse width modulated signal to realize switch capacitor DAC. The switch control scheme is built using basic AND gates to generate the control signals for RDCM. Only one capacitor and reduced transistor count in digital part reduces the silicon area occupied by the ADC to only 0.0098 mm². The converter, designed in GPDK 90 nm CMOS, exhibits maximum sampling frequency of 100 kHz & consumes 6.75 μ W at 1 V supply. Calculated signal to noise and distortion ratio (SNDR) at 1 V supply and 100 kS/s is 48.68 dB which relates to ENOB of 7.79 bits. The peak values of differential and integral nonlinearity are found to be +0.70/-0.89 LSB and +1.40/-0.10 LSB respectively. Evaluated figure of merit (FOM) is 3.87 × 10²⁰, which show that the proposed ADC acquires minimal silicon area and has sufficiently low power consumption compared to its counterparts in RFID applications.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

Recently Radio Frequency Identification (RFID) system has shown its potential candidature as a unique identification and sensing system in the area of manufacturing and supply chain, human identification, monitoring and tracking system and healthcare etc. [1–4]. In general, RFID is an identification system, similar to classic barcodes and biometrics, but has many advantages over aforesaid systems [5,6]. In modern RFID systems, christened as sensor-embedded RFID (SE-RFID), a sensor is embedded into a RFID transponder (TAG) to enable sensing capabilities along with identification [7,8]. Such RFID TAGs are either active or passive. Active TAGs take energy from a battery while passive TAGs draw their own energy from radiation field of the interrogator. As shown in Fig. 1, the architecture of sensor TAG consists of four main components: a sensor, ADC interface and digital processing block, analog RF front end and an antenna.

Although RFID is better choice over state of art identification systems, it is not perfect in all aspects and has some security issues such as eavesdropping, spoofing, denial of service etc. [9–11]. These security issue in RFID can be dealt with the help of digital processing block. Digital processing makes system more capable and enhance the ability of performing more sophisticated processes, mitigating the

* Corresponding author.

E-mail addresses: ashish_j@students.iitmandi.ac.in (A. Joshi), satinder@iitmandi.ac.in (S.K. Sharma).

security issues. Thus integrating an ADC and digital processor in architecture of RFID sensor TAG is unavoidable. However the electromagnetic waves emitted by interrogator does not have infinite energy and therefore power consumption in the embedded digital processing block must be kept low as possible.

ADC interface could become the major source of power consumption and therefore it must be designed to dissipate approximately 10 μ W or less while achieving the required conversion rate. Among different types of ADCs, Successive Approximation Register (SAR) ADC is preferred for medium resolution, low power and moderate-speed applications [12–14].

With only one comparator in the system, SAR can achieve the demand for low power consumption but the capacitor matching which can be achieved in the process affects the attainable effective number of bits (ENOB) and limits the resolution of ADC. Moreover reducing the number of capacitors to shrink the size of ADC can



Fig. 1. Block diagram of Sensor RFID TAG in weather monitoring system.

improve functionality of RFID TAG. In spite of this, very less efforts have been reported on reducing the multiple-capacitor-DAC to single-capacitor-DAC ADC design. J. Marjonen et al. [15,16] presented SAR ADC for RFID applications in 180 nm technology node using resistive DAC, works at low frequency of 1 kHz and consumes 5.1 μ W power. De Venuto et al. in [17] reported 6.25 kS/s SAR ADC for RFID application which acquires 0.35 mm² on silicon chip. Rail-to-rail SAR ADC demonstrated by Kim et al. in [18] utilizes C-2C capacitor array, dissipates 13 μ W and occupies 0.45 mm² on wafer. Similarly, other various architectures have been proposed by various researchers that employ MOS based resistor structure or dual string resistor structure as DAC, has drawback of either slow speed or high power consumption or it acquires higher portion of the chip [19].

Therefore, to realize the several different applications on a single chip, an energy efficient SAR ADC architecture demands small layout area and simple SAR logic along with low power consumption.

Switch-capacitor DAC successive approximation ADC has number of advantages over the existing architecture. DC reference current, charging or discharging the only capacitor in the circuit is controlled by the pulse width modulated clock to realize the switch-capacitor DAC in the ADC. Only single capacitor and reduced complexity of SAR logic significantly minimizes the area acquired by the ADC; eventually increasing the functionality of overall chip. Therefore, instead of multiple-capacitor DAC and a complex SAR logic, a SAR ADC is realized by only a single capacitor, constant current mirrors, dynamic latch-comparator and a simplified SAR logic.

As the limit to the ADC's accuracy depends mainly on the accuracy of the DAC, performance of current mirror determine the quality of this ADC. Designing current source and sink which provide stabilized current over the required range of frequency with minimum mismatch in their currents is the most critical part in this ADC. Moreover the current mirror must not react to voltage fluctuations at its output (sourcing/sinking node) and function dynamically to provide constant current whenever required. Literature survey reveals only one effort that is reported in this direction. Zhang and Lee [20] designed an ADC using cascode current mirrors. However, the cascode mirrors are unable to supply invariable current when required; resulting in mismatch between source and sink currents

and affecting the performance of ADC. While, the similar design implemented in 90 nm CMOS, because of the finite output impedance of cascode current mirror, voltage variation at its output introduce variability in current thereby increasing the non-linearity errors in ADC. Moreover, this reported work is only limited to circuit simulations, presents no information about circuit components, and lacks in providing evidence of performance parameters such as area occupied by ADC, SNDR, ENOB and FOM. Without post layout simulations, the performance of reported work is unpredictable in presence of parasitic components.

This work, for the first time demonstrates a switch-capacitor DAC successive approximation ADC which is designed in 20 times lesser area than a conventional SAR ADC would acquire. Noting that current mirror has overall control over performance of this ADC, the novel idea to utilize Regulated Dynamic Current Mirrors (RDCM) to build the ADC is implemented in this design. RDCM has better performance in terms of stability and is highly immune to channel charge injection issue as compared to cascode current mirror. Mismatch in source and sink current of RDCM is also minimized dramatically, improving conversion accuracy and linearity of the ADC. This 100 kS/s ADC consumes only few microwatts of power and provide better ENOB than state-of-the-art counterparts; making it an optimum solution for moderate speed sensor-embedded RFID applications.

The paper organization is as follows. Section 2 presents the switch-capacitor DAC SAR ADC design and architecture. Section 3 describes design of ADC circuit components. The simulation results are shown in Section 4, followed by conclusion in Section 5.

2. ADC design and architecture

The architecture of switch-capacitor DAC successive approximation analog to digital converter (SAR ADC) using regulated dynamic current mirror is shown in Fig. 2. Analog part includes an input sampling block which consists of transmission gate switches, a dynamic latch comparator and the charge/discharge current mirrors. Control signal for current source/sink are generated by digital circuit that comprises of switch control logic implemented using basic AND gates.



Fig. 2. Architecture of switch capacitor DAC successive approximation ADC.

The operation of 8-bit SAR ADC comprises total of 10 cycles. In first cycle, sampling is performed and capacitor is pre-charged with value equivalent to input sample $(V_{CM}-V_{IN})$ while the final one is used for ADC output latch. In remaining 8 cycles, bit cycling is performed to generate 8 bit digital output. During the 1st-bit cycling, voltage across the capacitor V_{CAP} is compared with common mode voltage V_{CM} to get the most significant bit (MSB) without charging or discharging the capacitor. However during next 7 bit cycles, depending upon V_{CAP} and V_{CM} comparison the capacitor will be charged or discharged by certain amount of voltage which is decided by control pulse width T_W . High (bit 1) at comparator output initiates charging whereas low (bit 0) enables discharging. As depicted in Fig. 2, the voltage across the capacitor is controlled by controlling the charge (Charge $_T_W$) or discharge (Discharge $_T_W$) period of capacitor which actually is achieved by controlling ON/OFF period of switches S₁ and S₂.

The switches S_1 and S_2 are forced to work complementary to each other, allowing only one of them to conduct in one cycle. The partial charge or discharge voltage corresponding to the switch control signal pulse width T_W are given by following equations:

$$\Delta V_{CAP} = \frac{I_O \times T_W}{C}.$$
(1)

$$\Delta V_{CAP} = \frac{\pm V_{FS}}{2^{N-i}}.$$
(2)

where, V_{FS} is full-scale input voltage, N is number of resolution bits, i is assigned cycle count, I_0 is constant reference current, T_W is the ON period of S₁ or S₂ and C is the only capacitor in DAC circuit.

The width T_W of control signal is reduced by half in every bit cycle to employ the binary search algorithm in feedback loop; utilizing this precisely organized switch-capacitor charging and discharging circuit as a DAC for SAR ADC. The transient response of

Table 1 Variation in T_W for every bit cycle and corresponding ΔV_{CAP}

the current mirrors and attainable minimum width T_W at chosen value of current limits the resolution of this ADC. Generally, ultra high speed ADCs are not required in RFID systems, as the timing requirements are restricted by the communication protocol used. RFID systems usually make use of the EPC global class1 gen2 UHF protocol [21]. This protocol stipulates a timeout of 11.28 µs which corresponds to requirement of 88.6 kS/s ADC. To achieve full scale input conversion (0–1V) using a single 7.7 pF capacitor and constant current of 2 µA, the variation in T_W for each cycle mandatory to get corresponding ΔV_{CAP} is presented in Table 1. The period of every cycle is set to 1000 ns (> max T_W of 960 ns) to obtain the 100 kS/s sampling rate which is sufficient enough to sample the data sensed by RFID TAG in low-medium speed applications such as healthcare, manufacturing and supply chains, monitoring and tracking applications etc.

3. ADC circuit components

3.1. Regulated dynamic current mirror

Current mirrors in this category of SAR ADC are required to work dynamically to obtain precise voltage change across DAC-capacitor. In addition to this, output current of the mirror should remain stable all the time when mirror is active. Standard cascode current mirror fails to fulfill this requirement and current does not remain constant over the voltage variations at its output terminal. Up-scaling the active loads transistors in cascode mirror to overcome this issue impedes the transient response of the mirror.

Therefore Regulated Dynamic Current Mirror (RDCM) are designed to achieve the above mentioned performance. Current source implemented using PMOS transistors is shown in Fig. 3. To hold the drain

	Output bit	i	ΔV_{CAP} (mV)	$T_W(\mathrm{ns})$
1	-	_	-	-
2	7th (MSB)	7	_	-
3	6th	6	250	960
4	5th	5	125	480
5	4th	4	62.5	240
6	3rd	3	31.25	120
7	2nd	2	15.62	60
8	1st	1	7.81	30
9	Oth (LSB)	0	3.90	15
10	-	-	-	-
	1 2 3 4 5 6 7 8 9 10	Output bit 1 - 2 7th (MSB) 3 6th 4 5th 5 4th 6 3rd 7 2nd 8 1st 9 0th (LSB) 10 -	Output bit i 1 - - 2 7th (MSB) 7 3 6th 6 4 5th 5 5 4th 4 6 3rd 3 7 2nd 2 8 1st 1 9 0th (LSB) 0 10 - -	Output bit i ΔV_{CAP} (mV) 1 - - - 2 7th (MSB) 7 - 3 6th 6 250 4 5th 5 125 5 4th 4 62.5 6 3rd 3 31.25 7 2nd 2 15.62 8 1st 1 7.81 9 0th (LSB) 0 3.90 10 - - -



Fig. 3. PMOS regulated dynamic current mirror (P-RDCM) utilized in the ADC to source constant current to DAC-capacitor.

potential of transistor PM_6 to a fixed value, this mirror circuit has buffer placed between reference and copying sub-circuits. Compared to output impedance of cascode mirror, output impedance of the RDCM increases by the gain of the added buffer amplifier. This translates into decrease in channel length modulation effect and drain current variation as a function of voltage at source/sink node reduces drastically [22].

As portrayed in Fig. 3, the output current I_0 is controlled by gate voltage of transistor PM₅ and terminal voltage V_{DS6} . Transistor PM₂ and PM₄ provide the essential feedback to regulate the voltage V_{DS6} over desired voltage range. With the arrangement of the transistors as shown in Fig. 3, suppose $|I_0|$ falls down from required value, $|V_{DS6}|$ will decrease and so does the $|V_{GS4}|$; reducing the current through PM₄. But the current through biased transistor NM₁ and therefore PM₄ is fixed. This causes $|V_{GS4}|$ to increase. Since $|V_{GS4}| = |V_{DS6}|$, $|V_{DS6}|$ will is stabilized, allowing larger current to pass through PM₂. And hence I_0 is stabilized.

Assuming transistors PM_2 and PM_4 operate in saturation the gain of feedback loop (consisting of PM_2 and PM_4) is given as,

$$G = g_{m2} \cdot r_{o2} \cdot g_{m4} \cdot r_{o4} \tag{3}$$

The output resistance Rout therefore becomes,

 $R_{out} = g_{m2} \cdot r_{o2} \cdot g_{m4} \cdot r_{o4} \cdot r_{o6} \tag{4}$

where g_{m2} , g_{m4} are the respective transconductance of PM₂ and PM₄; r_{o2} , r_{o4} and r_{o6} are the output resistances of PM₂, PM₄ and PM₆ respectively. The values of g_m and r_o are obtained as

$$g_{m2} = \sqrt{2 \cdot |I_0| \cdot \beta \cdot (1 + \lambda \cdot |V_{DS2}|) \cdot \left(\frac{W_2}{L_2}\right)}$$
(5)

$$g_{m4} = \sqrt{2 \cdot |I_{bias}| \cdot \beta \cdot (1 + \lambda \cdot |V_{DS4}|) \cdot \left(\frac{W_4}{L_4}\right)}$$
(6)

$$r_{02} = \frac{1 + \lambda \cdot |V_{DS2}|}{\lambda \cdot |I_0|} \tag{7}$$

$$r_{o4} = \frac{1 + \lambda \cdot |V_{DS4}|}{\lambda \cdot |I_{bias}|} \tag{8}$$

$$r_{o6} = \frac{1 + \lambda \cdot |V_{DS6}|}{\lambda \cdot |I_0|} \tag{9}$$

where W_2/L_2 and W_4/L_4 are aspect ratios of PM₂ and PM₄ respectively, λ is channel length modulation factor and $\beta = \mu_p C_{ox}$.

From Eq. (3) through Eq. (9), loop gain *G* and output resistance R_{out} can be calculated as

$$\begin{split} G &= 2 \cdot \beta \sqrt{\frac{(1 + \lambda \cdot |V_{DS2}|)(1 + \lambda \cdot |V_{DS4}|)}{|I_0| \cdot |I_{bias}|}} \binom{W_2}{L_2} \binom{W_4}{L_4}} \cdot \\ &\frac{1 + \lambda \cdot |V_{DS2}|}{\lambda \cdot |I_0|} \cdot \frac{1 + \lambda \cdot |V_{DS4}|}{\lambda \cdot |I_{bias}|} \\ R_{out} &= 2 \cdot \beta \sqrt{\frac{(1 + \lambda \cdot |V_{DS2}|)(1 + \lambda \cdot |V_{DS4}|)}{|I_0| \cdot |I_{bias}|}} \binom{W_2}{L_2} \binom{W_4}{L_2}} \cdot \\ &\frac{1 + \lambda \cdot |V_{DS2}|}{\lambda \cdot |I_0|} \cdot \frac{1 + \lambda \cdot |V_{DS4}|}{\lambda \cdot |I_{bias}|} \cdot \frac{1 + \lambda \cdot |V_{DS6}|}{\lambda \cdot |I_0|} \end{split}$$

Therefore, in order to obtain highly stabilized current (higher loop gain and output resistance), the aspect ratios for PM_2 and PM_4 should be high along with small value of I_{bias} . In fact, it is observed that increasing width of the transistor also increases the capacitance associated with it and there exists a trade-off between allowable current variation and required transient response of the mirror.

Transmission gate switches TG_1 and TG_2 , as shown in Fig. 3, are deployed to provide dynamic functionality to the mirror. To minimize the major difficulty of channel charge injection in scaled down

switched capacitor circuits, instead of inserting switch between the current mirror and the capacitor, the proposed scheme incorporates these transmission gate switches within the current mirror itself. For the period TG_CLK is high the current mirror is enabled and sources constant current I_o from the capacitor. On the other hand, transistor PM₅ is turned off and the mirror is disabled when TG_CLK goes low. Similar RDCM is designed using NMOS transistors to sink the constant current from the DAC-capacitor.

3.2. Input sampling block

Fig. 4 presents the input sampling block implemented using stacked transmission gates. Here, the two- transistor stack transmission gate (TG) switch is utilized to obtain full range input sampling. Use of stacked transistor transmission gate in the design reduces the leakage current and improves the conversion accuracy especially at small values of inputs [23]. Also, the designed switch limits the settling error of sampled voltage to less than half of the LSB. Besides this, the transistors in this design are sized by considering the short channel effect (SCE) and reverse short channel effect (RSCE) in MOS devices [24]. During input sampling, voltage across capacitor is set to $V_{CM}-V_{IN}$ by enabling switches TG₃ and TG₄. Switches TG₃ and TG₄ are disabled for rest of the period except the sampling period. On the other hand TG₅ is deactivated during input sampling and activated for rest of the period. This arrangement allows to keep the common mode voltage of comparator (V_{CM}) as the threshold voltage to generate digital output.

3.3. Dynamic latch comparator

Sense amplifier (adapted from [25]) combines positive feedback with resistive input and the output latch stores the output bit for one bit cycle. In addition to this, current design of sense amplifier is supplied with output buffers to make output loading identical and achieve rail to rail output. Fig. 5 illustrate the Dynamic latch comparator used in this ADC. While CLK=0 V during reset phase, output is pulled up to VDD through reset transistors PM₁ and PM₄. Whereas during evaluation phase when CLK=1 V, the two oppositely coupled inverters initiate positive feedback and convert small difference of current through input transistors to large full scale value. Offset voltage of the comparator will play the role in deciding conversion accuracy of this ADC. Offset will decrease the input voltage range, degrading the signal to noise ratio (SNR) of ADC. For this reason, PMOS transistors are designed to optimize the offset voltage of ADC whereas transistor NM₅ is made slightly wider to reduce the delay of the comparator [26].



Fig. 4. Input Sampling Block employing stacked transmission gate.



Fig. 5. Dynamic latch comparator used in proposed ADC architecture.



Fig. 6. Switch control scheme to generate control pulses for switches S₁ and S₂.

3.4. Switch control logic

In a significant departure from convention, a new SAR logic scheme, which does not employ counters, flip flops and complex routing, is described here. Control of switches S₁ and S₂ is provided by switch control block. Fig. 6 shows the gate level implementation of switch control scheme constructed using two and three input AND gates. The output of latch comparator is applied at the respective input of control block. The pulse width modulated (PWM) signal with ON period for corresponding cycle as mentioned in Table 1 is assumed to be provided by an external clock source, for example analog and digital PWM controller IC reported in [27], and is fed to Cnt_Clk pin of the control logic. Fig. 7 shows the logic timing waveforms for switch control circuit. If the output of latch comparator is high (output bit 1), Charge $_T_W$ is enabled to charge the capacitor through P-RDCM. Similarly, Discharge $_T_W$ is enabled to discharge the capacitor through N-RDCM if comparator output is low (output bit 0). Both Charge $_T_W$ and Discharge $_T_W$ are disabled for rest of the period.

As seen from Fig. 6, the digital part of ADC is very simple in architecture, unfussy and acquires minimal area of the chip. Note that this type of ADC spit out data serially, a serial to parallel converter could be used to convert data into parallel, in case required.

4. Post-layout simulation results

8 bit, switch-capacitor DAC SAR ADC is implemented in GPDK 90 nm CMOS process using cadence design tools. DAC consists of only single 7.7 pF metal-insulator-metal (MIM) capacitor. After considering different layout designs for capacitor, the DAC capacitor is built in ring shaped structure. As remaining circuitry is fitted into this ring to obtain symmetric layout, area occupied by the capacitor is the area acquired by the ADC on the chip. The photograph of ADC layout is shown in Fig. 8. This enormously hardware efficient ADC occupies only 0.0098 mm² of silicon chip area. This compactness facilitates to assign additional memory space and functionality to RFID TAG.

To obtain more realistic results, parasitic components extracted from layout are considered in specter simulations while evaluating static and dynamic performance of ADC. Fig. 9 shows the comparison of PMOS standard cascode current mirror and regulated dynamic current mirror (P-RDCM) when both the mirrors are designed to source constant current of 2 µA to the capacitor. The transient analysis of the mirror circuit shows the capability of the mirror to switch between ON and OFF state. To find transient response, both the mirrors are clocked at 33.33 MHz which is the frequency corresponding to lowest control signal pulse width T_W (Charge $_T_W$ =15 ns). It is observed that the buffer placed between reference and copying circuit of the mirror does not affect the transient response and RDCM is able to switch between the two states with settling time of 0.3 ns. The voltage at output node of mirrors is swept from 0 V to 750 mV, to obtain the dc characteristics. From Fig. 9 it is evident that the RDCM performance is superior to that of standard cascode current mirror. Variation in current of cascode current mirror is between 1.98-2.22 µA however, it is only between 2.0-2.02 µA in case RDCM.

In addition to this, Table 2 compares the output impedance of standard cascode current mirror and RDCM when both mirrors are conducting 2 μ A current. Also, linearity is calculated for ADC with two different mirrors and the comparison is shown in Table 2. For ADC with cascode mirrors, the value of DNL on positive side is double that of DNL for ADC with RDCM and DNL of -1 clearly shows that one of the code is missing from the digital output. INL value is still on higher side for cascode mirror ADC producing diverse linearity pattern. Compared to output impedance of standard cascode mirror, average 10 times increment is obtained in RDCM output resistance. Almost 10 times reduced variation in current and equally good transient response leads to better ENOB, improved accuracy and linearity in ADC output.



Fig. 7. Logic timing diagram of switch control circuit.



Fig. 8. ADC Layout in GPDK 90 nm CMOS.

For an 8 bit ADC, to obtain 1 LSB change in digital output, there must be 3.9 mV change in analog input. Therefore, to obtain less than a half LSB error in the output, offset of the comparator should be very small compared to 1.9 mV. Offset voltage of the dynamic latch comparator used in this design is found to be 220 μ V and is considerably small as compared to analog resolution of the ADC.

The DNL and INL error, calculated by applying slow ramp (near DC signal) at ADC input are shown in Fig. 10. Peak DNL and INL error is +0.70/-0.89 and +1.40/-0.10 LSB respectively. The major error in DNL occurs in the middle of MSB transition while worst case INL is observed between the output codes 180 and 245.

Though there is a satisfactory improvement in linearity, it is still amendable in future iterations of the ADC.

Signal to Noise and Distortion ratio (SNDR) of ADC is measured by calculating FFT spectrum of ADC output for full scale input voltage at 781 Hz and sampling rate of 100 kHz using 128 sample points (Fig. 11). The calculated SNDR is 48.68 dB providing effective number of bits (ENOB) of 7.79 bits. Improved SNDR shows that this innovative ADC design is resistant to disturbance and empower accurate conversion of sample detected by RFID TAG in noisy environment.

In addition to this, Fig. 12 shows the switch control signal and capacitor voltage V_{CAP} for minimum (0 V) and maximum (1 V)



Fig. 9. Comparison of PMOS standard cascode and RDCM, when both the mirrors are designed to source 2 µA current.

Table 2Cascode current mirror and RDCM Rout comparison.



Fig. 10. Differential and Integral Non linearity of the ADC.



Fig. 11. FFT Spectrum (128 points) at 100 kS/s for input of 781.25 Hz and supply of 1 V.



Fig. 12. Switch control signal and capacitor voltage VCAP for minimum (0 V) and maximum (1 V) input signal

Table 3ADC power breakdown at 1 V supply.

ADC component	Power consumption			
Sampling circuit	78.9232 nW			
Latch comparator	1.155 μW			
N-RDCM	2.4639 μW			
P-RDCM	1.6259 μW			
Switch control logic	1.4279 μW			
Total	6.751 μW			

input. In every bit cycle, control signal reduces to half of its value in previous cycle, and so does the voltage change made in capacitor voltage. For 0 V input only the NMOS RDCM (switch S_2) is on which discharges the capacitor, leading to a digital output of 00000000. On the other hand, for 1 V input only the PMOS RDCM (switch S_1) is enabled which charges the capacitor, giving all 1's at the output of ADC. Fig. 12 proves the working of pulse width to analog switch-capacitor DAC as V_{CAP} change for minimum input is exact mirror image of the V_{CAP} change for maximum input.

To calculate the power consumption in ADC, 1 V peak to peak, near nyquist frequency sinusoid is applied to ADC input. The average power consumption in core ADC, when clocked at 100 kHz sampling rate comes out to be $6.75 \,\mu$ W. Table 3 shows the power consumption in different circuit components of the ADC. Being active circuits in the design, N-RDCM and P-RDCM constitute

almost half of the total power. The comparator designed to obtain minimal offset voltage consumes only 17% of total power while the input sampling block dissipates the least power amongst all. The quantization energy (E_0) for this ADC is calculated to be 305 fJ/ conv-step while the figure-of-merit (FOM) which takes area occupied by the ADC into consideration [13] and has been used to compare the performance of ADC, defined as,

$$FOM = \frac{2^{N} \times f_{sample}}{Power \times Chip - area}$$

is computed to be 3.87×10^{20} .

Table 4 compares the performance of this ADC with its state-ofthe-art counterparts. The proposed ADC has the highest FOM and smallest chip area compared to other ADCs in RFID application.

5. Conclusion

An 8 bit, 100 kS/s, 1V switch-capacitor DAC SAR ADC for RFID applications is presented in this paper. Only one capacitor in the circuit and low-complexity SAR logic tremendously minifies the area acquired by the ADC on silicon wafer. As only one capacitor is used in this design, capacitor matching is not a concern here. To achieve high accuracy, good power efficiency and moderate speed, this unprecedented ADC incorporates regulated dynamic current mirrors (RDCM) in the design. Comparative DC and transient

Table 4

Reference	Verma [12]	Ruoyu Xu [13]	Hua Gao [14]	Kim, H [18]	Marjonen, J. [16]	De Venuto [17]	G. Zhang [20]	Proposed Work
Technology (CMOS) Application	180 nm Wireless sensor nodes	180 nm Imager	130 nm Neural recording	180 nm Biomedical	180 nm RFID	140 nm RFID	350 nm -	90 nm RFID
Supply voltage (V) Sampling rate (kS/s) Resolution (Bits) DNL (LSB) INL (LSB) SNDR (dB) ENOB(Bits) Power (µW) quantization energy (fJ/ conv)	1 200 8 0.66 0.68 49.7 7.9 19 397	3.3/1.8 768 10 0.55 0.77 60.94 9.83 58 74	1.2 31.2 10 0.29/-0.37 0.28/-0.33 60.26 9.7 1.1 42	1.5 137 10 0.56 0.38 53.8 8.65 13.4 243	1.8 1 8 2 2.4 - 5.1 -	$ \begin{array}{r} 1.2 \\ 6.25 \\ 12 \\ + 1.4 \\ - 1.0 \\ 3 \\ 60 \\ - \\ 0.850 \\ 66.5 \\ \end{array} $	3.3 500 6 0.42 0.32 - - 22.6	$ \begin{array}{c} 1 \\ 100 \\ 8 \\ +0.7/-0.89 \\ +1.4/-0.1 \\ 48.68 \\ 7.79 \\ 6.75 \\ 304 \end{array} $
Chip area (mm²) FOM	$\begin{array}{c} 0.63 \\ 2.14 \times 10^{18} \end{array}$	$\begin{array}{c} 0.01 \\ 1.27 \times 10^{21} \end{array}$	$\begin{array}{l} 0.11 \\ 2.64 \ \times \ 10^{20} \end{array}$	$\begin{array}{c} 0.456 \\ 2.30 \times 10^{19} \end{array}$	${}^{36}_{1.39\times10^{15}}$	$\begin{array}{c} 0.35 \\ 8.60 \times 10^{19} \end{array}$	-	$\begin{array}{l} 0.0098 \\ 3.87 \times 10^{20} \end{array}$

analysis of standard cascode mirror and RDCM shows that the RDCM performs exceptionally well while providing approximately 10 times more stable current to precisely change the voltage across DAC-capacitor. This ADC design has SNDR of 48.68 dB and ENOB of 7.79 bits. At 100 kS/s, power consumption in ADC is only 6.75 μ W. This architecture occupies only 0.0098 mm² on the chip, proving its candidature for sensor RFID interface circuits where the layout area of ADC is to be kept minimum compared to other circuitry while preserving the conversion accuracy and minimal power consumption in core ADC.

References

- H.H. Bi, D.K. Lin, RFID-enabled discovery of supply networks, IEEE Trans. Eng. Manag. 56 (1) (2009) 129–141.
- [2] M. POlívka, M. Švanda, P. Hudec, S. Zvánovec, UHF RF identification of people in indoor and open areas, IEEE Trans. Microw. Theory Tech. 57 (2009) 1341–1347.
- [3] J. Barman, G. Uswatte, T. Ghaffan, B. Sokal, E. Trinh, et al., Sensor-enabled RFID system for monitoring arm activity: reliability and validity, IEEE Trans. Neural Syst. Rehab. Eng. 20 (6) (2012) 771–777.
- [4] W. Yao, C.H. Chu, and Z. Li, The use of RFID in healthcare: benefits and barriers, in: Proceedings of the IEEE Conference on RFID-Technologies and Applications, 17–19 June 2010, pp. 128–134.
- [5] K. Finkelzeller, The RFID Handbook, 2nd ed., John Wiley & Sons, 2003.
- [6] M. Kaur, M. Sandhu, N. Mohan, P. Sandhu, RFID technology principles, advantages, limitations & its applications, Int. J. Comput. Electr. Eng. 1/3 (2011) 1793-8163.
- [7] Deng, H., Varanasi, M., Swigger, K., et al., Design of sensor-embedded radio frequency identification (SE-RFID) systems. in: Proceedings of the IEEE International Conference on Mechatronics and Automation, June 2006, pp. 792– 796.
- [8] A.P. Sample, D.J. Yeager, P.S. Powledge, et al., Design of an RFID based batteryfree programmable sensing platform, IEEE Trans. Instrum. Meas. 57 (11) (2008) 2608–2615.
- [9] Xiao, Q.; Boulet, C. & Gibbons, T. (). RFID security issues in military supply chains, in: Proceedings of the Second International Conference on Availability, Reliability and Security, ISBN: 0-7695-2775-2, Vienna, Austria, 10–13 April 2007, pp. 599–605.
- [10] A. Juels, RFID security and privacy: a research survey, IEEE J. Secur. Areas Commun. 24 (2) (2006) 381–394.
- [11] Egli Peter, A.G. Netmodule, Susceptibility of wireless devices to denial of service attacks, White paper, Netmodule AG, Niederwangen, Switzerland, 2006.
- [12] N. Verma, A.P. Chandrakasan, An ultra-low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes, IEEE J. Solid-State Circuits 42 (6) (2007) 1196–1205.

- [13] Ruoyu Xu, Bing Liu, J.i.e. Yuan, Digitally calibrated 768-kS/s 10-b minimum-size SAR ADC array with dithering, IEEE J. Solid-State Circuits 47 (9) (2012) 2129–2140.
- [14] H.u.a. Gao, R.M. Walker, P. Nuyujukian, K.A.A. Makinwa, K.V. Shenoy, B. Murmann, T.H. Meng, HermesE: a 96-channel full data rate direct neural interface in 0.13 μ m CMOS, IEEE J. Solid-State Circuits 47 (4) (April 2012) 1043–1055.
- [15] J. Marjonen, N. Pesonen, O. Vermesan, M. Aberg, A. Oja, H. Rustad, C. Rusu, P. Enoksson, An 8-bit 10 kS/s 0.18 um CMOS SAR ADC for RFID applications with sensing capabilities, Proc. Nor Chip (2007) 1–4.
- [16] J. Marjonen, O. Vermesan, H. Rustad, An 8-bit, 10 kHz, 5.1 μW, 0.18 μm CMOS SAR ADC for RFID applications with sensing capabilities, Analog Integr. Circuits Signal Process. 66 (3) (2011) 389–405.
- [17] D. De Venuto, D.T. Castro, Y. Ponomarev, E. Stikvoort, 0.8 μW 12-bit SAR ADC sensors interface for RFID applications, Microelectron. J. (Elsevier) 41 (11) (2010) 746–751.
- [18] Kim, H., Min, Y.J., Kim, Y., & Kim, S., A low power consumption 10-bit rail-to-rail SAR ADC using a C-2C capacitor array, in: Proceedings of the EDSSC 2008 IEEE International Conference on Electron Devices and Solid-State Circuits, 8-10 December 2008, pp. 1-4.
- [19] Tajalli, A., Leblebići, Y., Ultra-low power mixed-signal design platform using sub-threshold source-coupled circuits, in: Proceedings of the IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE), March 2010, pp. 711–716.
- [20] G. Zhang, and K.S. Lee, SAR ADC using single-capacitor pulse width to analog converter based DAC, in: Proceedings of the International Symposium on Circuits and Systems (ISCAS), 2012, pp. 2365–2368.
- [21] EPC global, Radio-frequency identity protocols class-1 generation-2 RFID v1.1.0. EPC global Standard, December 2005. (http://www.epcglobalinc.org).
- [22] C. Aoumazou, J.B. Hughes, D.M. Pattulo, Regulated cascode switched-current memory cell, Electron. Lett. 26 (5) (1993) 303–305.
- [23] Dai. Zhang, A. Bhide, A. Alvandpour, A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13 CMOS for medical implant devices, IEEE J. Solid-State Circuits 47 (7) (2012) 1585–1593.
- [24] T. Kim, H. Eom, J. Keane, and C. Kim, Utilizing reverse short channel effect for optimal sub- threshold circuit design, in: Proceedings International Symposium on Low Power Electronics and Design, 2006, pp. 127–130.
- [25] T. Kobayashi, K. Nogami, T. Shiroto, Y. Fujimoto, A current controlled latch sense amplifier and a static power-saving input buffer for low-power architecture, IEEE J. Solid-State Circuits 28 (4) (1993) 523–527.
- [26] B. Wicht, T. Nirschl, D. Schmitt-Landsiedel, Yield and speed optimization of a latch-type voltage sense amplifier, IEEE J. Solid-State Circuits 39 (No. 7) (2004) 1148–1158.
- [27] Li-Jen Liu; Yeong-Chau Kuo; Wen-Chieh Cheng, Analog PWM and Digital PWM Controller IC for DC/DC Converters, in: Proceedings of the Fourth International Conference on Innovative Computing, Information and Control (ICICIC), 7–9 December 2009, pp. 904–907.