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Multilevel metal/$Pb(Zr_{0.52}Ti_{0.48})O_3$/$TiO_xN_y$/Si for next generation FeRAM technology node

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ABSTRACT

Metal–Ferroelectric–Insulator–Semiconductor (MFIS) thin film capacitors with lead zirconate titanate ($Pb(Zr_{0.52}Ti_{0.48})O_3$) as ferroelectric layer and ultrathin high-κ titanium oxynitride (TiO_xN_y) as insulating buffer layer on p-Si are fabricated by RF magnetron sputtering for non-volatile multilevel ferroelectric random access memory (FeRAM). Micro Raman analysis of the proposed systems confirmed the existence of most stable tetragonal rutile phase in ultrathin TiO_xN_y and perovskite phase of PZT thin films. AFM analysis showed that surface roughness of ultrathin TiO_xN_y and thin PZT films are ~2.54 nm and ~1.85 nm, respectively and result the uniform interface between substrate and metal. The maximum *C–V* memory window of ~1.25 V was obtained at cyclic sweep voltage of ±6 V and starts to decrease when the sweep voltage exceeds 6 V due to charge injection. The fabricated structure possesses good data retention measured till 1.5 h and high, low capacitance states remain distinguishable even if extrapolated to 15 years. The proposed system exhibited excellent TiO_xN_y–Si interface, incomparable high breakdown field strength ~11.15 MV/cm and low leakage current density (*J*) ~5 μA/cm^2 at +4 V. Thus, Au/PZT/TiO_xN_y/Si MFIS based FeRAM devices with multilevel operation, high breakdown field and excellent retention are prospective contender for next generation multilevel FeRAM technology node.

1. Introduction

The advent of online data storage, smart cards, cellular phone or digital cameras, personal electronics necessitate memories which can provide fast data access, high retention and low power consumption while allowing cost reductions through scaling of FeRAM for next generation technology node [1–3]. The front line memories which used to meet above stated demands are Flash memories and FeRAM. FeRAM can be integrated in CMOS technology using two extra masks [4] while Flash memories require additional fabrication steps due to extra floating gate and charge pumping circuits which typically increase manufacturing cost, and power dissipation [5]. FeRAM provides much better access time, high endurance, and low power consumption as compared to Flash memories [6]. Likewise, it permits a non-destructive read-out, high speed, low voltage operation with higher endurance and abides by the IC's scaling rule [7]. Nevertheless, to fabricate MFIS structure for FeRAM with the aforesaid properties is a challenge for process engineers due to inter-diffusion of dielectric materials to the substrate during high temperature annealing process along with low remanent polarization and dielectric constant. Indeed, in FeRAM with MFIS structure utilizing a typical ferroelectric material has high dielectric constant which generates a moderately large voltage drop in the insulating layer. Furthermore, the charge induced by switching the polarization of ferroelectric material sometimes goes beyond the induced charge in the buffer insulator layer. Consequently, the insulating layer may breakdown before the polarization of the ferroelectric film is saturated. Therefore, ferroelectric gate material needs to have sufficient remnant polarization (P_r) of order (~1 μC/cm^2) to tune the charge required to control the channel conductivity of silicon. Recently, ferroelectricity in Si doped HfO_2 was demonstrated [8] for FeRAM but showed a much lower fatigue of ~10^4 cycles [24,25] as compared to PZT. In the past decade, a lot of investigation is done on MFIS structure using Al_2O_3 [9], ZrO_2 [10], Y_2O_3 [11], Dy_2O_3 [12], La_2O_3 [13], HfO_2 [14], etc. as gate dielectrics and PZT [9–13], SBT [14] as ferroelectric films. However, each of them investigated the MFIS structure with thick ferroelectric films of order greater than 60 nm. The scaling concerns of FeRAM reported in [15] make it necessary to study the characteristics of MFIS structures with thin ferroelectric layers and ultrathin buffer layers for next generation technology node. In literature, FeRAM using TiO_2 as buffer layer has been reported with thickness of 90 nm and memory window of 0.5 V [16]. On the other hand, the breakdown

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voltage reported for Al/PZT (250 nm)/Al_2O_3 (3.8 nm)/Si structure is 1.2 MV/cm [9]. Likewise, the retention characteristics are considered to be the most important issue of MFIS structure for non-volatile memory applications. The data retention periods from a few days to 10 years have been reported in the diverse MFIS FETs structures [8–13]. Recently, significant interests in titanium oxynitride films have attracted the scientific community because of its high-κ which allows sufficient voltage across ferroelectric layer, improved physical and chemical properties such as compared to TiO_2 such as higher resistance to interfacial oxide formation, an excellent diffusion barrier, especially for memory devices [17,18]. Still, there is only limited literature found regarding the investigation of ultrathin (~6 nm) TiO_xN_y as an alternate buffer material and thin (~20 nm) PZT layers for next generation FeRAM device applications. There are various well established physical and chemical techniques such as physical vapour deposition (PVD), chemical vapour deposition (CVD), and plasma enhanced chemical deposition (PECVD) listed in the literature to deposit the titanium oxynitrides (TiO_xN_y) films [19,20]. R.F based reactive ion magnetron sputtering is specially an attractive process to deposit TiO_xN_y films and PZT films due to its numerous intrinsic advantages such as low-temperature deposition, large area deposition, and use of non-toxic gas, over the counterpart [11]. The effect of electrical stress on Au/PZT/TiO_xN_y/Si MFIS FeRAM devices was reported elsewhere [21], however the structural, multilevel characteristics and breakdown analysis are needed to be performed which forms the basis of this work.

In this work, authors have investigated multilevel Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structure for next generation FeRAM device applications. The chemical confirmation and surface roughness was investigated by Raman spectroscopy and AFM respectively. The size of memory window with sweeping voltage, breakdown voltage and retention analysis was investigated by Capacitance Voltage (*C–V*), Leakage current density–Voltage (*J–V*) and Capacitance–Time (*C-T*) method.

2. Experiment

P-type ⟨100⟩ orientation, 2-in. diameter, standard RCA cleaned silicon wafers (1–10 Ω cm) were used in this study. After drying these RCA cleaned silicon wafers in nitrogen gas, wafers were used for the ultrathin TiO_xN_y (buffer layer) and thin PZT ($PbZr_{0.52}Ti_{0.48}O_3$) films deposition by RF-magnetron sputtering system and thicknesses of deposited films were measured by Accurion EP3 imaging Ellipsometry. At the outset, the ultimate pressure of sputtering system was 1.9×10^{-5} torr accomplished and then deposition of ultrathin (6 nm) TiO_xN_y films were carried out at R.F power 90 W, 3.9×10^{-2} torr, pressure of Ar/N_2 (60:19 sccm) and temperature of 27 °C on the four RCA cleaned silicon wafers. Ensuing to this the above ultrathin TiO_xN_y deposited, three Si wafers were subjected to the high vacuum annealing at 600 °C for 30 min in N_2 ambient and fourth wafer was held in reserve as a reference for further metrology characterization. Hereafter the annealed three TiO_xN_y deposited Si wafers were used for the PZT thin film deposition. The three ultrathin TiO_xN_y film deposited wafers were loaded into the RF-magnetron sputtering and the ultimate pressure 1.9×10^{-5} torr was achieved. Deposition of 20 nm PZT ($PbZr_{0.52}Ti_{0.48}O_3$) thin films were followed at R.F power 120 W, 1.8×10^{-2} torr pressure of Ar and temperature of 27 °C. Subsequent to this the PZT (20 nm) deposited samples were subjected to annealing at 700 °C for 60 min in inert ambient. For FeRAM, MFIS gate electrodes, samples were loaded into RF Magnetron Sputtering chamber and then followed the deposition of 100 nm, Au thin film onto PZT/TiO_xN_y/Si samples at 3.9×10^{-2} torr. Next, in the photolithography process, a 1500 nm layer of positive photo-resist (PR) is first applied onto the Au surface using the spin coating technique and pre-heat at 90 °C for 1 min. This process (soft bake) was done in order to remove the moisture on the surface of Au/PZT/TiO_xN_y/Si substrate and to semi-harden the photo-resist (PR) layer. To define the gate electrodes commercial available chrome photo masks that have been designed using the aid of AutoCAD software and subsequently fabricated and transferred onto the mask was employed using conventional photolithography process. To transfer the circles, dot matrix pattern on the surface of Au/PZT/TiO_xN_y/Si sample, the ultraviolet (UV) light were exposed for 10 s using the mask aligner, through the chrome mask. After development, the portion of the photo-resist that is exposed to light becomes soluble to the photo-resist developer. This process was carried out for 30 s and continue by pre-heated to between 100 and 109 °C (hard bake) with a view to remove unwanted moisture and enhance the adhesion between gold and photo-resist prior a high power microscope (HPM), inspection of the wafer, to see if the circles, dot matrix patterns were clear and well defined. Then the process was continued by immersing the sample in gold etchant for 30 s before removing the resist. Finally the fabricated gate electrode of $\sim 3.85 \times 10^{-3}$ cm^2 area was experimentally measured through high precision travelling optical microscope. The structural information and phase purity of deposited TiO_xN_y thin film was characterized by Raman Spectroscopy using WiTec Germany at 532 nm wavelength of laser light. The topography and morphology of thin films were studied by Atomic Force Microscopy of Imaging Company, USA (Pico-Scan). Further, the MFIS structures of FeRAM were electrically characterized at room temperature by capacitance–voltage (*C–V*), current–voltage (*I–V*) and capacitance–time (*C–T*) using the KEITHLY 4200 SCS system.

3. Results and discussions

3.1. Structural characteristics

The chemical confirmation of TiO_xN_y (6 nm) and PZT (20 nm) films were carried out by Raman spectroscopy. Fig. 1(a) indicates the significant signature of Raman spectral peaks at 235 cm^{-1}, 612 cm^{-1}, 821 cm^{-1} corresponding to most stable tetragonal rutile phase [22] which is one of desirable phase required for utilization of TiO_xN_y as a buffer for FeRAM device applications, while peaks 144 cm^{-1} and 359 cm^{-1} represents the existence of anatase phase. Likewise, the reduction in the Raman intensity and broadening of spectral peaks full width half maxima attribute the presence of nitrogen in the TiO_xN_y [22]. Similarly, Fig. 1(b) represent the $Pb(Zr_{0.52}Ti_{0.48})O_3$ Raman signature peaks at ~198 cm^{-1}, ~315 cm^{-1} and ~495 cm^{-1} corresponds to vibrational modes at E [transverse optical(2TO)], A_1 [transverse optical (2TO)] and E[transverse optical (3LO)]+A_1[Transverse Optical (2LO)]. This confirms the presence of perovskite phase of PZT film, which one of prime importance for the excellent remnant polarization [23].

The interface between the thin films and silicon substrate intensely depends on the surface roughness of the buffer layer and PZT thin film in the MFIS structure. Moreover, the surface roughness of the insulator layer do affect the electrical properties of MFIS structure because of non-uniform thickness and poor interfacial properties; therefore, the smooth surface of TiO_xN_y and PZT thin films is very important [27]. Surface morphology of PZT and TiO_xN_y thin films were characterized by Atomic Force Microscopy in tapping mode. Fig. 2(a) and (b) shows the 2D and 3D the surface morphology images of 6 nm (TiO_xN_y) and 20 nm $Pb(Zr_{0.52}Ti_{0.48})O_3$ films. The R.M.S surface roughness of ultrathin TiO_xN_y and thin PZT films are computed ~2.54 ± 0.39 nm and ~1.85 ± 0.23 nm respectively, where the error is calculated from 5 μm × 5 μm AFM images (not shown). The appearance of particles on the surface of TiO_xN_y thin

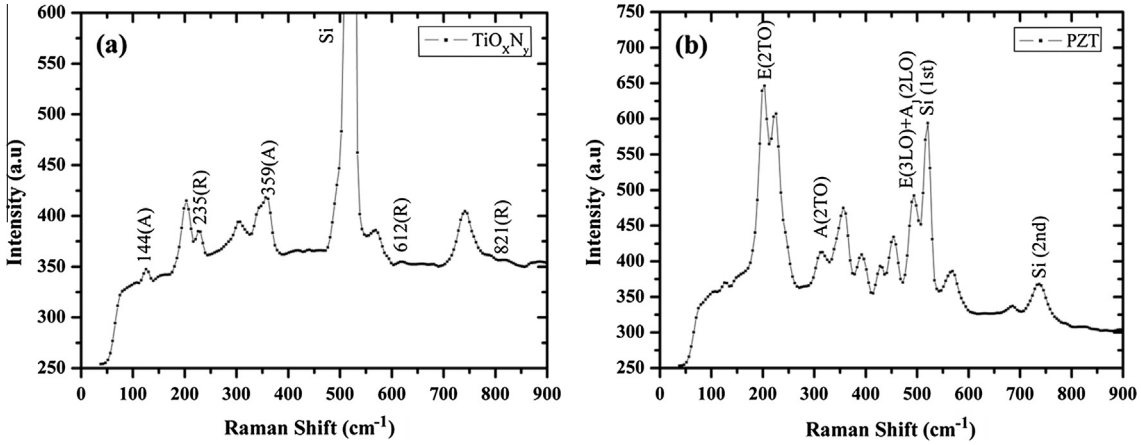

Fig. 1. Raman spectra of (a) ultrathin (~6 nm) TiO_xN_y buffer layer, and (b) PZT thin (~20 nm) films for Au/PZT/TiO_xN_y/Si, MFIS FeRAM devices respectively, in the range 0–900 cm^{-1}.

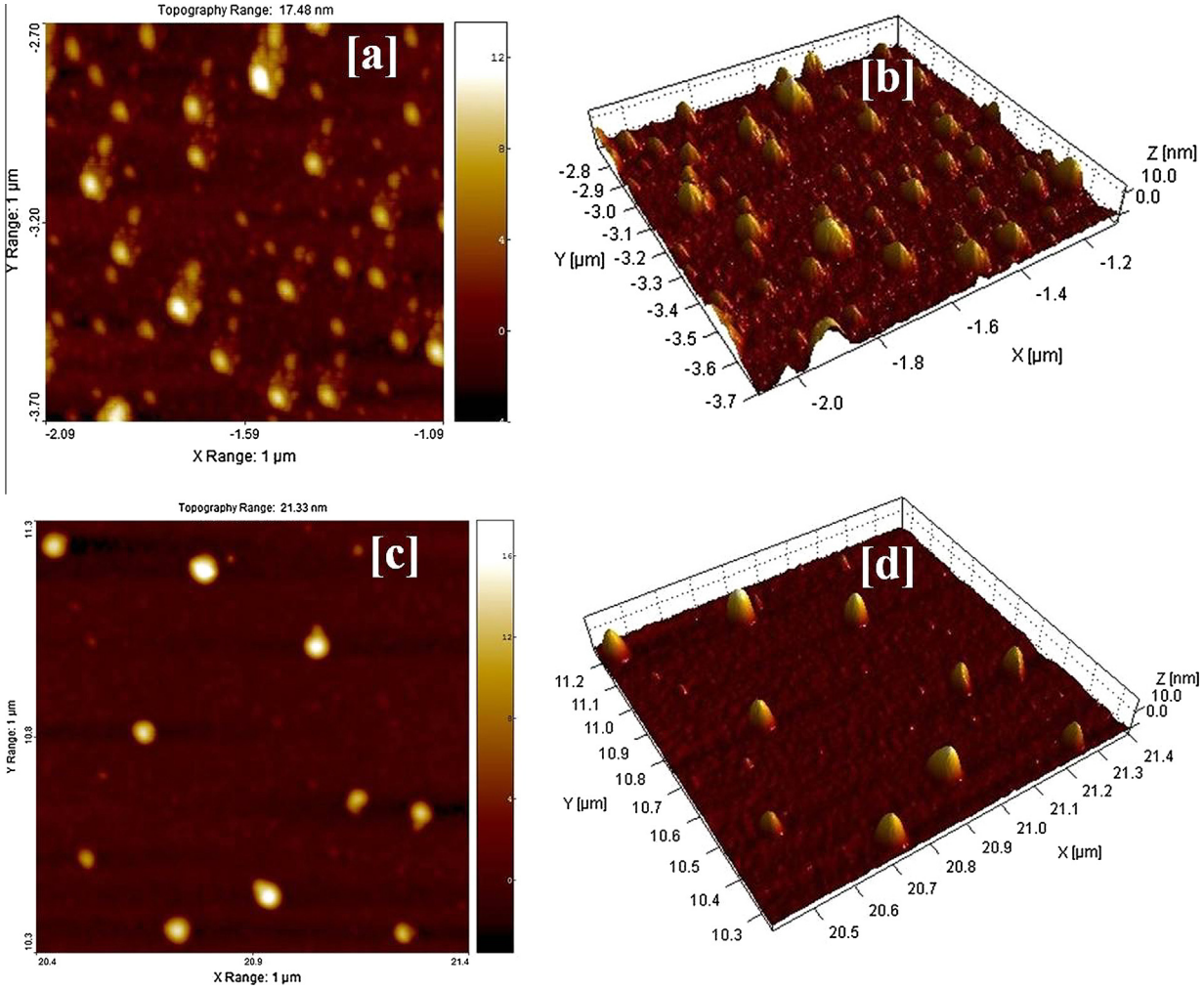

Fig. 2. A.F.M 2D and 3D images: (a and b) ultrathin (~6 nm) TiO_xN_y buffer layer, and (c & d) PZT thin (~20 nm) films for Au/PZT/TiO_xN_y/Si MFIS FeRAM devices respectively.

film can be explained as, the sputtered thin film atoms/ions of TiO_xN_y may have adequate time to interact with the reactive plasma precursor gas atoms/ions, and results mixtures of asperities, which may be hemi-spherical, spherical and rounded-top pyramidal structures etc., and approached to the surface of substrate to form the respective TiO_xN_y phase. However, the similar trend also reported in the literature for titanium oxynitride films [26]. The average particle size of TiO_xN_y and PZT were found in the present study are 42.21 nm and 52.61 nm.

3.2. Electrical characteristics

Fig. 3 shows the typical cyclic *C–V* characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structure of FeRAM, measured at

1 MHz frequency and 0.01 V/s sweep rate for different sweep voltages [21]. During forward sweep from accumulation to inversion once the ferroelectric layer gets polarized it alters the surface conductivity of silicon and results the clockwise hysteresis which is attributed to the polarization of PZT. The hysteresis or memory window is defined by the flatband voltage shift obtained from dual sweep method of *C–V* Characteristics. Here dual sweep method implies sweeping the voltage from accumulation (−*V*) to inversion (+*V*) during forward sweep followed by sweeping the voltage from inversion (+*V*) to accumulation (−*V*) during backward sweep. The memory window was calculated to be 0.42 V at sweep voltage of ±2 V which increases to 1.25 V at sweep voltage of ±6 V. This noteworthy increase in FeRAM memory window is consequence of gate voltage variation attribute to the considerable improvement in $PbZr_{0.52}Ti_{0.48}O_3$ polarization. However at higher gate voltages memory window found to decreases from 1.2 V @ ±6 V to 1.10 V @ ±10 V.

To further confirm that the observed memory window is due to polarization and not due to mobile ionic charges, interfacial polarization, and rearrangement of space charge in lattice, *C–V* characteristics were measured at different frequencies as show in inset of Fig. 3. However the trivial change in memory window at different frequencies which may be due to random variations, confirms that the observed memory window is due to ferroelectric polarization of PZT and not due to mobile charges.

Fig. 4 shows the variation of memory window at different sweep voltages. The memory window was nearly close to theoretically calculated memory window from [2]

$$\Delta W \approx 2 d_f E_C \tag{1}$$

where d_f is the thickness of PZT, E_C is the coercive electric field. However at greater than 8 V sweep voltage, memory window gets sidetracked from theoretical calculation. This decrease in memory window is attributed to increase in charge injection ($\Delta V_{FB,ci}$) due to increase in effective electric field across the insulating oxide [14] and can be given by the following equation:

$$\Delta W \approx 2 d_f E_C - \Delta V_{FB,ci} \tag{2}$$

Fig. 5 shows the gate leakage current density (*J*) as a function of gate voltage sweep (*V*). The measured gate leakage current density for Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structures was ~5 μA/cm^2 at +4 V which increases to ~11 μA/cm^2 at +27 V. It is perceived that with the variation in electric field from 1.92 to 10.38 MV/cm consequences the endurable alteration in gate leakage current by a factor 6 μA/cm^2. It clearly signifies the good

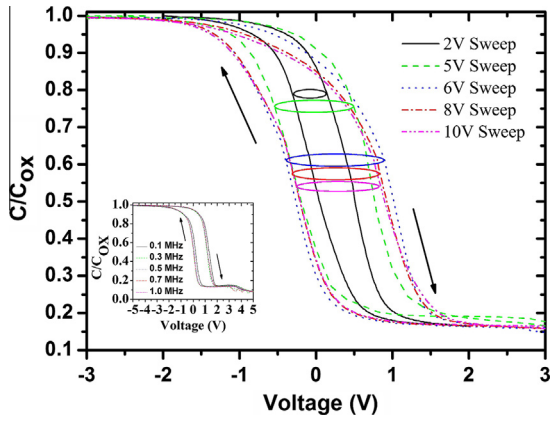

Fig. 3. Cyclic *C–V* characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS FeRAM devices measured at 1 MHz for different sweeping voltage. The inset shows cyclic *C–V* characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS FeRAM devices measured at different frequencies for confirmation of memory window due to polarization.

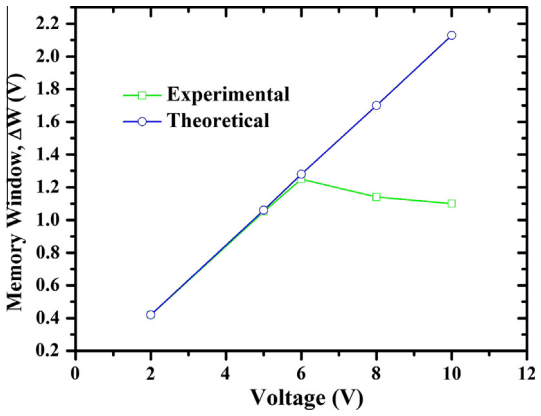

Fig. 4. Memory window for Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS FeRAM devices measured at 1 MHz frequency for different sweeping voltage.

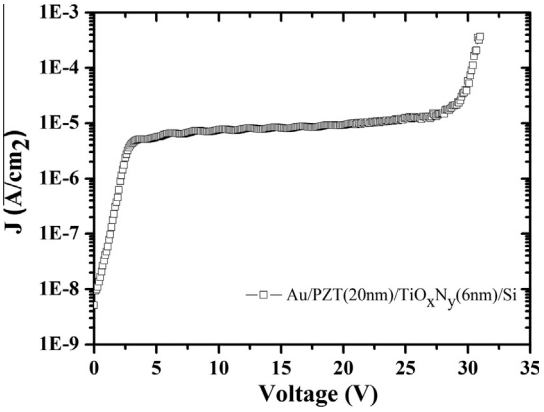

Fig. 5. Leakage current density (*J*)–voltage (*V*): characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si MFIS FeRAM devices.

quality TiO_xN_y/Si interface of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structure and prompt as a prospective contender for next generation FeRAM device applications. However, there is an abrupt increase in leakage current at 29 V gate voltage which corresponds to the very high breakdown field of ~11.15 MV/cm. This considerable higher breakdown strength is an indication of the elevated reliability and feasibility to use Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structure for multiple-level FeRAM device applications. Here, an interesting question arises that which layer will breakdown first in MFIS gate stack of FeRAM.

The breakdown voltage is usually inversely proportional to dielectric constant. So, for MFIS gate stacks ferroelectric layer with high dielectric constant is expected to breakdown first and then the buffer layer. However, this not the sole criteria for confirming which layer will breakdown first in MFIS gate stack. Since, there may be different voltages across both ferroelectric and buffer layers which are generally calculated by the following relation:

$$\frac{V_f}{V_i} = \frac{D_f}{D_i} * \frac{\varepsilon_i}{\varepsilon_f} \tag{3}$$

where V_f, V_i are the voltage across ferroelectric and insulator respectively. D_f, ε_f andD_i, ε_i are the thickness, dielectric constant of ferroelectric and insulator thin films respectively. So, depending upon the voltage across each layer, which layer will breakdown first can be easily estimated. For real non volatile memory applications, it is essential to check retention time behaviours of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si based MFIS structures. Fig. 6 shows the retention behaviours of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS

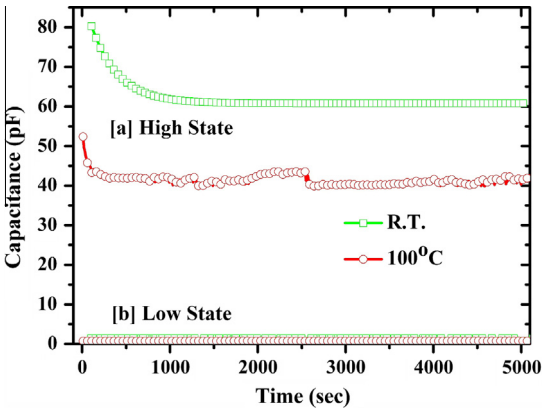

Fig. 6. Capacitance–time characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si MFIS FeRAM devices at room temperature (R.T.) and 100 °C.

structures characterized through the *C–T* analysis at room temperature. In this methodological investigation, a "write" voltage pulse of +5 V in height for low capacitance state, −5 V in height for high capacitance state applied for 100 ms to the MFIS devices. The high and low capacitance values are measured separately as a function of aging, keeping the bias voltage fixed near flat band voltage of 1.5 V. Initially the high state capacitance decays exponentially and loses ~25% of charge within few seconds and then eventually decays linearly with respect to time. The high and low capacitance difference is distinguishable for 1.5 h, even if extrapolated to 15 years [21], which is desired for next generation non-volatile memory applications. Since the real chips operate at elevated temperatures therefore high temperature aging at 100 °C is usually performed for device applications [28]. On high temperature aging, decrease in high state capacitance was observed but still the high and low capacitance values are distinguishable for 1.5 h, even if extrapolated to 15 years. Therefore, it is concluded that the Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS devices are one of the most promising contestants for realizing multi-level FeRAM with a long data retention time.

4. Conclusion

We have investigated the electrical characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structures for FeRAM device applications. The *C–V* characteristics results showed that device operates at multiple lower operating voltages suitable for multi-level FeRAM applications. A higher breakdown field of ~11.15 MV/cm and lower leakage current density of MFIS structures support its excellent candidature for multi-level FeRAM device applications. Furthermore, the devices exhibited excellent retention characteristics measured till 1.5 h at room temperature and 100 °C, capacitance difference remain distinguishable even if extrapolated to 15 years. Micro Raman and AFM analysis of the proposed systems confirmed the existence of most stable tetragonal rutile, perovskite phases and lesser surface roughness of buffer, polarization films respectively. Thus, the proposed Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS FeRAM devices props-up an exceptional aspirant as multilevel FeRAM for next generation technology node.

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References

[1] International Technology Roadmap for Semiconductor (ITRS). <http://public.itrs.net/Links/2013ITRS/Summary2013.html>, 2013.
[2] Zhang J, Sun J, Zheng XJ. A model for the *C–V* characteristics of the metal–ferroelectric–insulator–semiconductor structure. Solid-State Electron 2009;53:170–5.
[3] Tang MH, Zhou YC, Zheng XJ, Yan Z. Structural and electrical properties of metal–ferroelectric–insulator–semiconductor transistors using a Pt/$Bi_{3.25}Nd_{0.75}Ti_3O_{12}$/$Y_2O_3$/Si structure. Solid-State Electron 2007;51:371–5.
[4] Summerfelt S, Dev ST. Texas instruments, dallas "embedded ferroelectric memory using a 130-nm 5 metal layer Cu/FSG logic process. In: Fifth annual non-volatile memory technology symposium. Orlando (FL, USA), paper E-4, 2004.
[5] Wong OY, Wong H, Tam WS, Kok CW. An overview of charge pumping circuits for flash memory applications. In: IEEE 9th international conference on ASIC (ASICON), 2011. p. 116–9.
[6] Kryder MH, Kim CS. After hard drives—what comes next? IEEE Trans Magn 2009;45:3406–13.
[7] Kato Y, Yamada T, Shimada Y. 0.18-μm nondestructive readout FeRAM using charge compensation technique. IEEE Trans Electron Dev 2005;52:2616–21.
[8] Mueller S, Summerfelt SR, Muller J. Ten-nanometer ferroelectric Si:HfO_2 films for next-generation FRAM capacitors. IEEE Electron Dev Lett 2012;33:1300–2.
[9] Chin A, Yang MY, Sun CL, Chen SY. Stack gate PZT/Al_2O_3 one transistor ferroelectric memory. IEEE Electron Dev Lett 2001;22:336–8.
[10] Chiang YW, Wu JM. Characterization of metal–ferroelectric ($BiFeO_3$)–insulator (ZrO_2)–silicon capacitors for nonvolatile memory applications. Appl Phys Lett 2007;91:142103.
[11] Lin CM, Shih WC, Chang IYK. Metal–ferroelectric ($BiFeO_3$)–insulator (Y_2O_3)–semiconductor capacitors and field effect transistors for nonvolatile memory applications. Appl Phys Lett 2009;94:142905.
[12] Chang CY, Juan TPC, Lee JYM. Fabrication and characterization of metal–ferroelectric ($PbZr_{0.53}Ti_{0.47}O_3$)–insulator (Dy_2O_3)–semiconductor capacitors for non volatile memory applications. Appl Phys Lett 2006;88:072917.
[13] Juan TPC, Lin CL, Shih WC. Fabrication and characterization of metal–ferroelectric ($PbZr_{0.6}Ti_{0.4}O_3$)–insulator (La_2O_3)–semiconductor capacitors for nonvolatile memory applications. J Appl Phys 2009;105:061625.
[14] Tang MH, Sun ZH, Zhou YC, Sugiyama Y, Ishiwara H. Capacitance–voltage and retention characteristics of Pt/$SrBi_2Ta_2O_9$/HfO_2/Si structures with various buffer layer thickness. Appl Phys Lett 2009;94:212907.
[15] Setter N, Damjanovic D, Eng L. Ferroelectric thin films: review of materials, properties, and applications. J Appl Phys 2006;100:051606.
[16] Zhou C, Peng P, Yang Y, Ren T. Characteristics of Metal–Pb($Zr_{0.53}Ti_{0.47}$)O_3–TiO_2–Si capacitor for nonvolatile memory applications. IEEE Int Conf Nano/Micro Eng Mol Syst (NEMS) 2011:134–7.
[17] Suzuki M, Saito Y. Structural stability of ultrathin silicon oxynitride film improved by incorporated nitrogen. Appl Surf Sci 2001;173:171–6.
[18] Kumar N, Fissel MG. Growth and properties of TiN and TiO_xN_y diffusion barriers in silicon on sapphire integrated circuits. Thin Solid Films 1987;153:287–301.
[19] Pradhan SK, Reucroft PJ. A study of growth and morphological features of TiO_xN_y thin films prepared by MOCVD. J Cryst Growth 2003;250:588–94.
[20] Kazemeini MH, Berezin AA, Fukuhara N. Formation of thin TiN_xO_y films by using a hollow cathode reactive DC sputtering system. Thin Solid Films 2000;372:70–7.
[21] Khosla R, Sharma DK, Sharma SK. Effect of electrical stress on Au/Pb($Zr_{0.52}Ti_{0.48}$)O_3/TiO_xN_y/Si gate stack for reliability analysis of ferroelectric field effect transistors. Appl Phys Lett 2014;105:152907.
[22] Bersani D, Antonioli G, Lottici PP, Lopez T. Raman study of nanosized titania prepared by sol–gel route. J Non-Cryst Solids 1998;232–234:175–81.
[23] Song HW, No K. Characterization of the property degradation of PZT thin films with thickness. J Korean Phys Soc 2011;58:809–16.
[24] Mueller S, Muller J, Hoffmann R, Yurchuk E. From MFM capacitors toward ferroelectric transistors: endurance and disturb characteristics of HfO_2-based FeFET devices. IEEE Trans Electron Dev 2013;60:4199–205.
[25] Lomenzo D, Takmeel Q, Zhou C. The effects of layering in ferroelectric Si-doped HfO_2 thin films. Appl Phys Lett 2014;105:072906.
[26] Rawal KS et al. Structural, wettability and optical investigation of titanium oxynitride coatings: effect of various sputtering parameters. J Mater Sci Technol 2012;28(6):512–23.
[27] Choi HS, Lim GS, Lee JH, Kim YT, Kim S, Yoo DC, et al. Improvement of electrical properties of ferroelectric gate oxide structure by using Al_2O_3 thin films as buffer insulator. Thin Solid Films 2003;444:276.
[28] Ozaki S, Kato T, Kawae T, Morimoto A. Influence of low-temperature post deposition annealing on memory properties of Al/Al_2O_3/Al-rich Al–O/SiO_2/p-Si charge trapping flash memory structures. J Vac Sci Technol B 2014;32:031213.