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Dual Gate Tunable and High Responsivity Graphene-Based Field Effect Transistors

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Summary: The output characteristics of a dual gated depletion mode, *n*-channel graphene field effect transistor (*n*-Gr-FET) are simulated to understand the unipolar I_{ds}–V_{ds} behavior for different values of gate voltages, (V_{back} and V_{top}). In our results, the saturated drain-source current (I_{ds}) varies from 0.001 to 100 μA/μm, 9 to 125 μA/μm and 16 to 135 μA/μm as V_{back} is varied from 5 to 40 V with correspondingly V_{top} of 0, 2 and 10 volts. Consequently, there is four to eight times enhancement in estimated mobility for varying V_{back} from 5 to 40V. The unipolar saturation in I_{ds} at higher values of V_{ds} can be understood from the compensation of parallel V_{ds} and transverse ($V_{back}-V_{top}$) electric fields. Furthermore, the channel length modulation (increase in I_{ds} for $V_{top} > 0$) supported by the increase in mobility, is observed because of reverse junction formation at the vicinity of the drain and gate terminal. The results signify that the dual gated *n*-Gr-FET, at optimum V_{back}, modulates the unipolar characteristics in channel region. Thus, making *n*-Gr-FET a potential candidate to stipulate the demand of low power, high performance functionalities in nano-electronic applications.

Keywords: channel length modulation; electrostatic coupling; graphene field effect transistor; transconductance; unipolar saturation

Introduction

In microelectronics, the Moore's Law[1] for miniaturization of devices is approaching to its own saturations for density of transistor on a chip and materials for fabrication of devices. In the nanometric regime scaling of device feature size cannot be continued in the same pace due to the critical scaling parameters, for instance constant electric field scaling, generalized scaling, and selective scaling in SiO_2-based CMOS technology.[2–5]

Recently, graphene-based field-effect transistors (Gr-FETs) have attracted much attention of the scientific community as a break through aspirant over carbon nanotube and nanowire FETs. The significant attraction is owing to the novel aspects of low power consumption,[6] minimum bias voltage, high resistance to electro migration, high frequency operation, outstanding carrier transport properties,[7–9] extra ordinary mechanical strength. Furthermore, the International Technology Roadmap for Semiconductors (ITRS) 2009 also proposes graphene to be a potential aspirant for emerging nanoelectronics beyond 11 nm, as an alternative to Si technology.[10] In comparison with the array of carbon nanotubes, the graphene offers advantages such as high carrier mobility ($\sim 10^5$ cm^2/Vs), higher Fermi velocities ($\sim 10^8$ cm/s almost 10 times higher than Si),[8] ballistic transport of charge carriers, ambipolar characteristics.[7,8] There are several reports on the unipolar current saturation in Gr-FETs resulting to applications in terahertz

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devices,[11] diode switch,[12,13] liquid crystal display,[14] biosensors.[15] The experimental results have been supported by an analytical model solving 2D Poisson's equation for bilayer graphene as well as the array of graphene nanoribbons for FET application.[16,17]

For high frequency applications, the dual gate FET shows superior performances over single gate FET due to lower access resistance.[18,19] The dual gated electrical doping in graphene layer results in reduction of access (contact) resistance by a factor of half and hence the transconductance (g_m) increases by four times.[20,21] The negative top gate voltage (V_{top}) on Gr-FET positions the Fermi level in the valence band and thus resulting to *p*-type characteristics *of* Gr-FET and *vice versa* for *n*-type Gr-FET with positive V_{top}. The process is termed as switching of charge carriers in FETs. During switching of carriers from *p* to *n* type in Gr-FET, at a certain V_{top} the Fermi level coinciding the bottom of the conduction and top of the valence band with minimum conductivity point due to very low density of states, called as Dirac point (V_{Dirac}).[7,8] The suspended graphene has a semi metal characteristics, thus put a limitation on its applications in digital domain because of zero band gap and poor ON-OFF (I_{ON}/I_{OFF}) ratio. The band gap of ~0.3 eV opens when graphene is supported on a substrate,[7,8] thus can be used for FET applications. However, the complete understanding over the control of charge carrier in graphene channel using electrostatic doping is still premature, thus providing a platform for further exploration on this aspect. In the present report, we propose a model for unipolar current conduction in depletion mode transistor using multi-layer graphene channel device.

The presented model accounts for the effect of transverse and parallel electrical fields in the channel and mobility dependence on the drive current saturation. For the non-planar devices, the carrier mobility in the inversion layer can be calculated using a semi-empirical Lombardi model,[22] which takes care of critical parameters like temperature, impurity concentration, transverse and parallel components of electric field for numerical simulations. This is well known that the carrier mobility in the inversion region is mainly affected by surface scattering, carrier-carrier scattering. The model considers the local value functions of continuous parameters like electric field and carrier concentration at semiconductor-insulator interfaces. The estimation of carrier mobility using this model is based on the Matthiessen approximation[23] and Thornber's scaling law,[24] which provides the relation of drift velocity *vs.* electric field. The advantage of the proposed model is the separate modeling of ambipolar current saturation to obtain the desired unipolar current saturation, hence providing the mobility of the carriers in the channel region. The model also can suggest the specific scattering mechanism dominating at different conditions, for instance the surface roughness scattering dominates at high transverse electric field and low temperatures.

Device Structure

The proposed dual gated depletion mode n-Gr-FET device structure comprises of a 5 nm multi-layer graphene on 300 nm SiO2 over a degenerately doped *p*-type Si (100) substrate. The 15 nm HfO_2 ($\kappa = 16$) is used as high-κ dielectric for top gating on graphene while SiO_2 is used as a dielectric for back gate. The aluminum (Al) metal has been used for contact materials for back-gate, top-gate, source and drain electrodes. For simulation purpose, the growth parameters for SiO_2 on Si substrate have been assumed to be grown by dry thermal oxidation of Si at 1000 °C. The channel length between the source-drain electrodes has been kept ~700 nm. The cross-sectional view of dual gated depletion mode graphene-based FET is as shown in Figure 1.

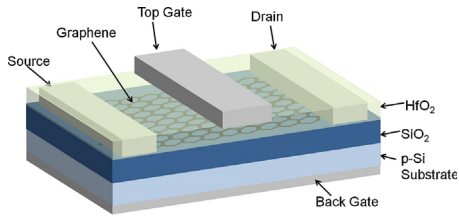

Figure 1.
Cross-sectional view of dual gate control *n*-Gr-FET.

Results and Discussion

The methodical simulation approach has been adopted to investigate the drain-source (I_{ds}–V_{ds}) characteristics for dual gated depletion mode *n*-Gr-FET. In this paper, top gate (V_{top}) bias is applied to modulate the charge density in the channel region; while constant back gate (V_{back}) bias is applied to generate sufficient vertical electric field to inject surfeit electrons in the channel. Figure 2 shows the top gated simulated I_{ds}–V_{ds} characteristics of *n*-Gr-FET, here the device operates through the electron conduction mechanism with positive V_{ds}(V_{ds}>V_{Dirac}). The observed zero or even negative transconductance ($g_m = \delta I_{ds}/\delta V_{top}$) in the I_{ds}–V_{ds} characteristics for increasing V_{top} indicates that undesirably the V_{top} has no control over I_{ds} in the channel. The zero and negative g_m signifying the existing small band gap in graphene comparing thermal energy of the electrons.[8,25]

With the increasing V_{ds}, the observed I_{ds} response can be divided in three different regions defined by *0 to A*, *A to B* and *B to C*. In the first region (*0 to A*), the parallel bias electric field is not completely compensated by the effective transverse field, the electron density in the channel region varies proportionally. In the second region (*A to B*), a non-linear disparity in I_{ds}–V_{ds} is noticed, which indicates that, the depletion region at the drain side extends and the holes start to accumulate in the channel region, leading to I_{ds} saturation. Thereafter, the further increase in bias voltage (*B* to *C*) the ambipolarity (both electrons and holes) contributes to the channel formation. This ambipolarity in the channel is understood with the zero input transconductance (g_m), thus undesirably the bias field is completely compensated by vertical field. Therefore, the ambipolar characteristics of graphene-based FETs, can be modulated by applying an external V_{back} bias voltage apart from V_{top}.

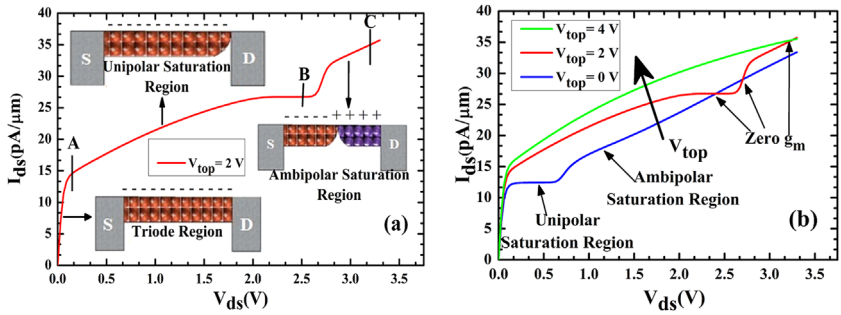

Figure 2.
Qualitative I_{ds}–V_{ds} of depletion mode *n*-Gr-FET showing (a) Triode, Unipolar saturation and Ambipolar saturation region for V_{top} of 2 V (b) zero input transconductance for variations in V_{top} of 0 V, 2 V and 4 V. (The same behaviour for V_{top} graphene-based FET is reported).[7,8]

Shown in Figure 3a, the I_{ds}–V_{ds} characteristics of *n*-Gr-FET as a function of V_{back} of 5, 20 and 40 V, respectively, while V_{top} is 0 volts. As depicted by curve 'p', the I_{ds} increases proportionally for V_{ds} varying from 0 to 0.1 V, and further saturates at ~1 nA/μm for V_{back} of 5 V. For curve 'q', I_{ds} increases linearly for $0 \leq V_{ds} \leq 0.2$ V, and at the I_{ds} ~14 μA/μm leading to a non-linearity for $0 < V_{ds} \leq 0.6$ V, before saturating to I_{ds} ~20 μA/μm, for V_{back} of 20V. Similarly, for curve 'r', I_{ds} follows the trend and increases linearly for $0 \leq V_{ds} \leq 0.4$ V, and at the I_{ds} ~76 μA/μm shows non-linearity for $0.4 < V_{ds} \leq 1.6$ V, before saturating to I_{ds} ~100 μA/μm, for V_{back} of 40V. We have observed the enhancement in (I_{ds}), of three orders of magnitude, for V_{back} from 5 to 40 V and five times increase for V_{back} varying from 20 to 40 V, while V_{top} is at 0 volts. The significant enhancement attributes that after certain value of V_{ds}, the bias field compensates with the transverse electric field and resulting to the I_{ds} saturation showing weak coupling of V_{top} with the channel. The carrier mobility across the channel region (μ_{ch}) is computed through the following formulation:

$$\mu_{ch} = \frac{Lg_m}{WC_{top}v_{ds}} \quad (1)$$

where, L (700 nm) is the length and W is the width of channel, C_{top} is the capacitance per unit area (~944 nF/cm^2) for 15 nm HfO_2. The calculated carrier mobility, in the linear region at V_{ds} = ~0.2 V, is found to be ~60, 75 and 235 cm^2(V.s)$^{-1}$ for V_{back} 5, 20 and 40 V (V_{back}), respectively. Thus, the carrier mobility enhances with V_{back} attributing the modulation of Fermi level in *n*-Gr-FET channel region.[20,21] Moreover, as evident from the proportional region (inset in Figure 3a), the slope of for I_{ds}–V_{ds} increases with V_{back} (5, 20, 40 V), showing increase in number of charge carriers while V_{top} 0V.

Further, the I_{ds}–V_{ds} characteristics as function of V_{back} of 5, 20 and 40 V have been shown for V_{top} of 2V (Figure 3b) and 10 V (Figure 3c). Unlike in Figure 3a, the I_{ds}–V_{ds} characteristics in Figure 3b and c do not follow the same trend for reaching the I_{ds} saturation values. The linear region exists for $0 \leq V_{ds} \leq 0.3$ V and, $0 \leq V_{ds} \leq 0.2$ V, until I_{ds} attains the value ~3.5 μA/μm (for curve 's') and ~4 μA/μm (for curve 'v'), respectively. Later I_{ds} saturating to ~9 μA/μm V_{ds}>2 v (for curve's') and 16 μA/μm V_{ds}>2.2 V (for curve 'v'). Correspondingly, increasing the V_{back} from 5 to 20 V, curves 't' and 'w', resulting to the linear behavior of I_{ds}–V_{ds} from $0 \leq V_{ds} \leq 0.3$ V and $0 \leq V_{ds} \leq 0.2$ V, and approaching the maxima at ~19 and 20 μA/μm, respectively. Finally, I_{ds} saturating to ~39 and 45 μA/μm when V_{ds}>2 V and V_{ds} > 2.4 V for V_{top} (2 and 10 V). For V_{back} from 20 to 40 V, curves 'u' and 'x', the I_{ds}–V_{ds} characteristics also exhibits resemblance to linear region from $0 \leq V_{ds} \leq 0.4$ V and $0 \leq V_{ds} \leq 0.3$ V, and attaining saturation values of ~125 and 135 μA/μm, above V_{ds}~2.6 V and V_{ds}~3V, while keeping V_{top} values of 2 and 10 V, respectively. Similarly, (inset of Figure 3b,c) the slope of linear

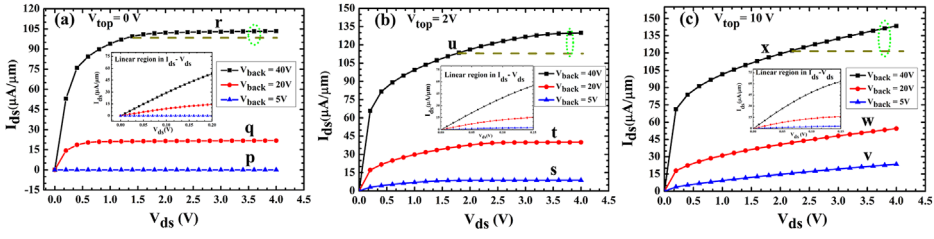

Figure 3.
I_{ds}–V_{ds} for dual gated *n*-Gr-FET as a function of V_{back} = 5, 20, 40 V at V_{top} (a) 0 V (b) 2 V (c) 10 V. Inset shows the magnified view of linear region in I_{ds}–V_{ds}.

region, the I_{ds} increases with the increase in V_{back} (5, 20, 40V), at fixed value of V_{top} (2 and 10 V). The estimated carriers mobility in the linear region is found to be ~296, 324, 2496 $cm^2(V.s)^{-1}$ for V_{back} values of 5, 20 and 40 V, respectively.

The output transconductance ($g_{ds} = \delta I_{ds}/\delta V_{ds}$) response, as a function of both V_{top} and V_{back}, is shown in Figure 4a. A noticeable increase in g_{ds} is observed at different V_{top} on increasing V_{back} from 5 to 40 V, which corresponds to the variation of unipolar charge carrier density (n) in the *n*-Gr-FET channel region.[26] The g_{ds} increases from ~(3.094 ± 0.834) nS/μm to (228 ± 4.04) μS/μm with V_{back} from 5 to 40 V while V_{top} is 0V. Furthermore for V_{top} 10 V, the g_{ds} increase from ~(20 ± 2.24) μS/μm to (440 ± 27.7) μS/μm with V_{back} varies from 5 to 40V. Thus, the obtained results support the earlier observation of carrier mobility enhancement in the *n*-Gr-FET channel region.

Figure 4b shows the variation in channel length modulation (CLM) as a function of V_{top} and V_{back}. It is clear from the Figure 3b and c that, that the I_{ds} saturation region is not following the trend of Figure 3a, for instance, with the increase in $V_{top}(>0)$, I_{ds} slightly increases due to reverse junction formation between the drain and the gate terminal leading to CLM in the vicinity of drain region and resulting in increase in I_{ds}. The behavior observed because of inverse relation of I_{ds} with *n*-Gr-FET channel length.[27,28] For V_{top} 0 V, the CLM is ~$(3.9 \pm 1.5)(\mu V)^{-1}$ for 40 V V_{back} and increasing V_{top} to 10 V results in significant increase in CLM to ~(24 ± 2.87) $(\mu V)^{-1}$. The above consequences signify that in dual gated *n*-Gr-FET, the optimum V_{back} (of same polarity as V_{top}) voltage efficiently moderates the accumulation of holes in the channel region, which suggests the unipolar characteristics in *n*-Gr-FETs. The dual gated graphene transistors have also been reported by Meric *et al*,[7] where the model rely on carrier concentration dependent velocity saturation leading to unipolar current saturating characteristic in 3 μm channel, without using the concept of channel length modulation. In the present work, the model accounts for the field dependent current saturation arising due to compensating transverse and parallel electric fields from the two gates in only 700 nm channel. To our understanding the transistor with lower gate length should have a higher cut-off frequency, thus justifying the consistencies with the literature.

Conclusion

We have studied the dual gated depletion mode model for *n*-Gr-FET based on standard models for simulating device characteristics taking into account the effect of transverse and parallel field

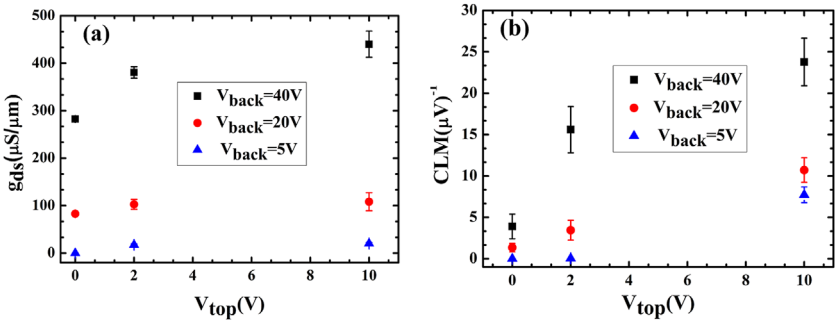

Figure 4.
(a) Output transconductance (b) variation in channel length modulation at different V_{top} and V_{back} gate voltages.

compensation for drive current saturation. The results provide a simple and intuitive perceptive of the under lying unipolar carrier transport in graphene channel leading to I_{ds} saturation. The desired unipolar conduction in the graphene channel is possible by utilizing the concept of channel length modulation at simultaneous optimization of V_{back} and V_{top}. The results on interesting transport properties suggesting for potential candidate for application in radio frequency nano electronic devices.

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