Charge Trapping and Decay Mechanism in Post Deposition Annealed Er_2O_3 MOS Capacitors by Nanoscopic and Macroscopic Characterization

Robin Khosla, Pawan Kumar, and Satinder K. Sharma

***Abstract*—In this paper, the charge trapping and decay mechanism is investigated in post deposition rapid thermal anneal (RTA) and furnace anneal (FA) erbium oxide (Er_2O_3) ultrathin films by Kelvin probe force microscopy (KPFM) technology. The trap density is calculated by the contact potential difference measurements obtained from KPFM. Furthermore, it is compared with the trap density calculated from the electrical measurements for Er_2O_3 MOS capacitors to give an insight on the reliability of KPFM for trap density estimation. Experimental results showed that post deposition RTA treatment results in higher trapping as compared to FA treatment on Er_2O_3 ultrathin films. It was observed that vertical charge leakage plays a dominant role in Er_2O_3 as compared to lateral charge spreading. The space-charge-limited conduction mechanism was observed in Er_2O_3 MOS capacitors, which was used to study the charge injection and decay mechanism. This investigation may help to fill the trap density computation gaps between nanoscopic KPFM and macroscopic capacitance–voltage-based electrical measurements for nanoscale MOS-based applications.**

***Index Terms*—Charge trapping, high-κ, rare earth oxides (Er_2O_3), rapid thermal annealing (RTA), Kelvin probe force microscopy (KPFM), MOS.**

I. Introduction

THE performance and functionality of integrated circuits (ICs) has been directed by the innovation and evolution of metal–oxide–semiconductor (MOS) driven by Moore's Law. However, conventional silicon dioxide based MOS devices have already attained their fundamental limits [1]. The gate leakage current at lower $SiO_2 < 5$ nm, due to direct tunneling exceeds 1 A/cm^2 at -1 V analogous to power dissipation to unacceptable values [2]. The solution to this tunneling problem is to replace SiO_2 with a relatively thicker higher dielectric constant (high-κ) material to keep leakage current well below 1.5×10^{-2} A/cm^2 for low standby power CMOS device applications [3]. Also, the next generation IC technology demands, high-κ based quality oxides not only for CMOS device applications but also for semiconductor memory applications such as charge storage memories i.e., NAND, NOR FLASH and non-charge storage memories i.e., Ferroelectric RAM (FeRAM), Magnetic RAM (MRAM), Phase Change RAM (PCRAM) and Resistive RAM (ReRAM) etc [1], [4]–[7]. In fact, the four key hitches of using high-κ on silicon identified by the industry and scientific community are the ability to continue scaling to lower equivalent oxide thickness (EOT), the loss of carrier mobility, threshold voltage shifts, and high concentration of defects [1]–[3], [8]. Although, the requirements of alternate oxide are six-fold: high enough κ, thermodynamically and kinetically stable, band offset (>1 eV), superior interface and small bulk electrically active defects [3].

In recent times, rare earth metal oxides with composition RE_2O_3 have attracted much attention as alternate gate dielectric for metal–oxide–semiconductor (MOS)/metal–insulator–semiconductor (MIS) structures in the past decade because of higher dielectric constant, band gap, conduction band offset and thermodynamic stability on silicon which restricts the formation of silicides and rugged surfaces [9]–[11]. Recently, from the class of rare earth oxides (REO), Sm_2O_3 have been reported as alternate dielectric for MOS based applications [5]. However, from REO's erbium oxide (Er_2O_3) especially with higher Gibbs free energy of $\sim$122 Kcal/mol, provides excellent thermodynamic stability which results in lowest possibility of silicate formation at elevated temperatures [12]. In addition, Er_2O_3 have been reported with high-κ ($\sim$8–20), higher conduction band offset ($\sim$3.5 eV) and lower leakage current density ($10^{-9} - 10^{-6}$ A/cm^2) [9], [10]. Also, there is limited literature found regarding the conduction mechanism of Er_2O_3 thin films. So, it becomes essential to investigate Er_2O_3 as alternate gate dielectric for MOS based device applications.

Generally, the electronic property of high-κ based structures is studied by macroscopic electrical characterization techniques such as capacitance–voltage (C–V), and leakage current density–voltage (J–V) measurements. But these measure the averaged property over gate area of fully processed MOS capacitor and are insensitive to variations at nanoscale [13]–[15]. Nevertheless, as the device dimensions continuously shrinks at nanoscale, the traps/defects in gate oxide have severe impact on reliability of nanoscale devices and there is a need of advanced characterization methods with high lateral resolutions which can investigate highly localized electrical properties at nanoscale [8], [15], [16]. In this respect, atomic force microscope based techniques especially, electrostatic force microscopy (EFM), also called KPFM is an elegant method employed for charge trapping analysis for ultrathin films on semiconductor, and gives direct investigation of charges from the surface

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of ultrathin films [17], [18]. In this method, initially charges are injected into the dielectric through a conductive tip which plays the role of metal gate over the bare dielectric surface forming nanometer sized MOS capacitor (few hundred nm^2) [19], followed by KPFM measurement which detects the potential difference between the tip and thin film surface. Characterization by these advanced techniques helps to find out how different manufacturing processes such as post deposition annealing treatments affect the electrical properties and quality (trap sites) of dielectrics at nanoscale. This necessitates the reliability of KPFM technique and to fill the electrical properties (e.g., trap sites) computation gaps between KPFM and traditional electrical characterization techniques.

In this paper, charge trapping and leakage mechanism of post deposition RTA and FA treated Er_2O_3 high-κ ultrathin films are investigated by KPFM. The total charge density is estimated from the measured CPD's by KPFM. Moreover, the Pt/Er_2O_3/Si/Pt, MISM structures are fabricated to compare the feasibility of the KPFM technology for trap charges estimation. The charge decay is explained based on vertical charge loss and lateral charge spreading mechanism. Here, Er_2O_3 films thickness (> 6 nm) was chosen to minimize the effect of direct tunneling for computation of trap density. Also, the measured capacitance and conductance of MOS devices was corrected to eliminate the effect of series resistance, so as to obtain real MOS characteristics. The flatband voltage ($V_{\rm fb}$), threshold voltage ($V_{\rm th}$), effective oxide charges ($N_{\rm eff}$) and leakage current density (J) of fabricated devices were investigated by C–V and J–V characteristics respectively. Further, the high frequency G–V curves were used to extract the interface trapping properties of Er_2O_3 ultrathin films. Finally, the conduction mechanism of Er_2O_3 is studied to investigate the charge distribution in Er_2O_3 thin films and the corresponding charge decay mechanism.

II. Experimental Procedures

The structure of Er_2O_3-Si and Pt-Er_2O_3-Si-Pt were fabricated on p-type Si (100) substrate with resistivity of 1–10 $\Omega - $ cm. After standard radio corporation of America (RCA) cleanings, wafers were used for the Er_2O_3 ultrathin film deposition by Techport RF-magnetron sputtering system from an erbium target with 99.99% purity. The chamber pressure was maintained at $\sim 5 \times 10^{-6}$ torr vacuum throughout the sputtering processes. Prior to sputtering on silicon samples, pre-sputtering was done at 60 W for 10 min to remove any impurities present on target surface. Firstly, deposition of ultrathin Er_2O_3 films was carried out at 300 K, R.F power 60 W, pressure of ultrapure (99.9999%) Ar/O_2 (45:5 sccm). Secondly, one set was subjected to rapid thermal annealing (RTA) at 700°C for 30 sec at ramp rate of 30°C/sec in N_2 and other set was subjected to furnace annealing (FA) at 700°C for 30 min in N_2 to compare both post deposition annealing (PDA) treatments. Finally, for metal–insulator–semiconductor–metal (MISM) gate electrodes, Pt thin films ($\sim$60 nm) were sputtered with a circular area of $\sim 1.256 \times 10^{-3}$ cm^2 on top through a shadow mask and on bottom after backside native oxide removal. The thickness of the deposited Er_2O_3 ultrathin films was measured to be $\sim$8.21 nm by Accurion EP3 imaging ellipsometer. The KPFM

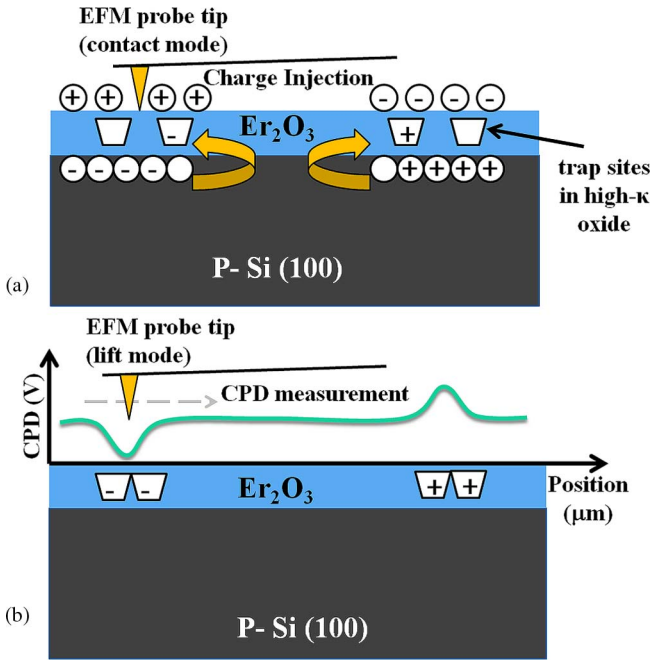

Fig. 1. Schematic of Er_2O_3/Si structure and EFM analysis method. (a) Charge injection in contact mode and (b) CPD measurement with lift height of 100 nm.

measurements were performed using AFM Dimension icon of Bruker. For CPD measurements by KPFM, initially the charge injection was done under contact mode (as shown in Fig 1(a)), $+3$ and -3 V was used for holes and electrons injection with substrate ground on Er_2O_3/Si structure for extended time of 10 min to confirm charge saturation. This was followed by CPD measurement, i.e., visualizing the injected charges in non-contact mode at lift height of 100 nm (as shown in Fig. 1(b)) [18]. The CPD measurements were done at fixed time intervals for time evaluation of surface potential profiles. The MOS capacitors were electrically characterized at room temperature by C–V at 100 KHz frequency and J–V using the KEITHLY 4200 SCS system.

III. Results and Discussion

Fig. 2 shows the line profiles of the measured CPD's for post deposition rapid thermal annealed (RTA) and furnace annealed (FA) Er_2O_3/Si structure. The line profiles are obtained by scanning a horizontal line across the injection center in the 2-D potential image. Since the positive sample bias or read voltage will form a positive electrostatic force during lift mode [13], therefore the bright (after electron injection) and dark regions (after hole injection) of inset images in Fig. 2, are attributed to hole and electron trapping respectively, from silicon and not from tip. Since during lift mode the positive electrostatic force on tip will repel the surface having hole trapping thus showing a height by white color spot in potential images and vice-versa. Higher CPD values for post deposition RTA Er_2O_3/Si, samples in comparison to FA Er_2O_3/Si, samples signifies high density of traps in post deposition RTA treated samples.

Fig. 3 shows the schematic band diagram of Er_2O_3/Si structure with (a) charge injection @ $+3$ V and (b) charge injection @ -3 V. In Fig. 3(a), initially the hole injection is performed

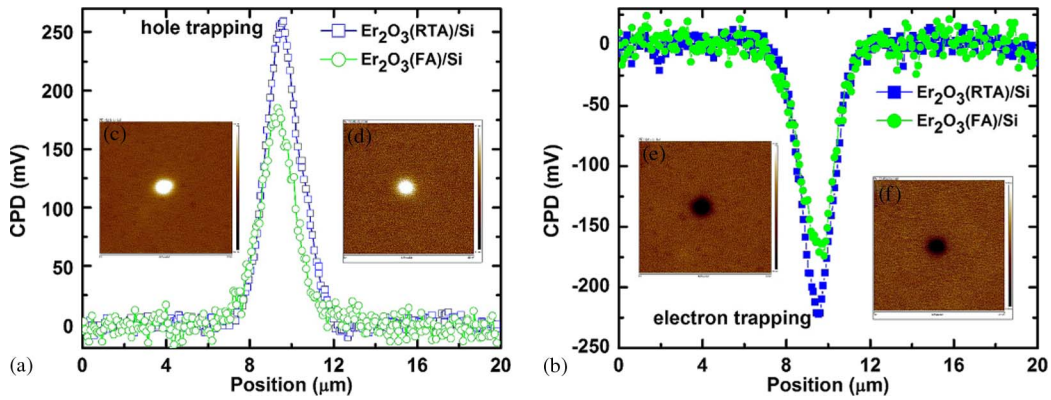

Fig. 2. Measured CPD line profiles of (a) hole trapping and (b) electron trapping for post deposition RTA and FA, Er_2O_3/Si samples. The bright and dark regions in inset images show the trapped holes and electrons, respectively for post deposition RTA (c), (e) and FA (d), (f) Er_2O_3/Si samples.

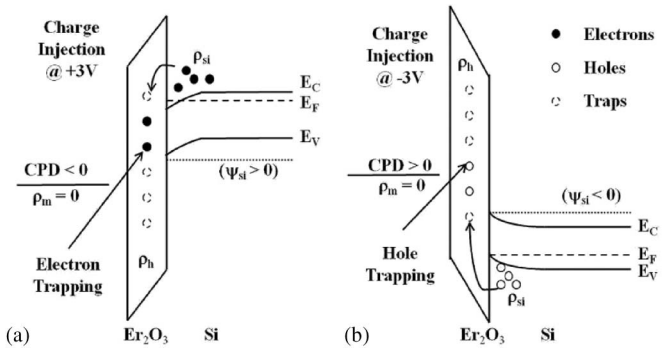

Fig. 3. Schematic band diagrams of high-κ/Si structure with (a) charge injection @ $+3$ V and (b) charge injection @ -3 V.

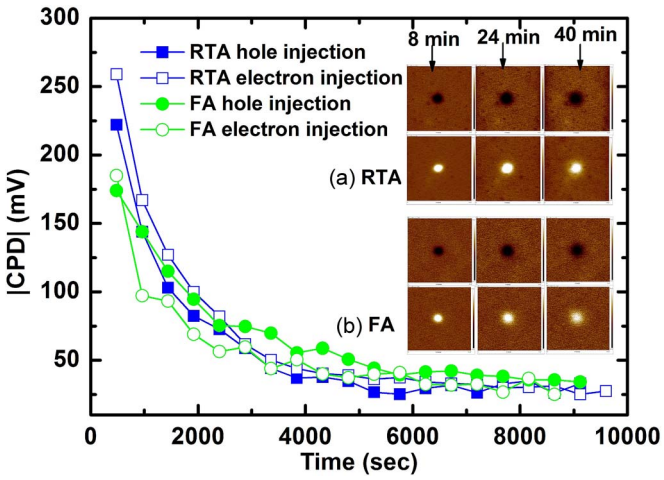

Fig. 4. The variation of CPD values with time for post deposition RTA and FA Er_2O_3/Si, samples measured at room temperature.

at $+3$ V, which results in electron trapping from silicon $(\rho_{\rm si})$ in high-κ Er_2O_3 traps (ρ_h) and hence CPD < 0 is obtained. In Fig. 3(b), electrons injection is performed at -3 V, which results in holes trapping from silicon $(\rho_{\rm si})$ in high-κ Er_2O_3 traps (ρ_h) and hence CPD > 0 is obtained. Further, to observe the retention of charges for post deposition annealing treatment by RTA and FA Er_2O_3/Si system, it is imperative to observe the charge decay using CPD values over time.

Fig. 4 shows the CPD values with time for post deposition RTA and FA Er_2O_3/Si, samples measured at room temperature. The measured CPD values decreases exponentially for both post deposition RTA and FA Er_2O_3/Si samples. From the measured CPD values over fixed time interval, it is observed that the CPD value decays rapidly in initial 4000 sec as compared to the increase in diameter of bright and dark spot over time as shown in inset of Fig. 4. Thus, it is attributed that vertical leakage is the dominant mechanism for charge leakage rather than lateral charge spreading [20]. From the CPD measurements, the approximate total charge density (units: traps/cm^2) can be estimated by using one-dimensional Poisson equation as follows [17], [18], [21], [22]:

$$\begin{aligned}\sigma_{\rm si}(\sigma_i,\rho_t) &= \int \rho_{\rm si}(z)dz \\ &= \mp\frac{\sqrt{2}\varepsilon_{\rm si}}{\beta L_D}\left\{[\exp(-\beta\psi_{\rm si})+\beta\psi_{\rm si}-1]\right. \\ &\quad \left.+\frac{n_{\rm po}}{p_{\rm po}}[\exp(\beta\psi_{\rm si})-\beta\psi_{\rm si}-1]\right\}^{\frac{1}{2}}\end{aligned} \tag{1}$$

where $\sigma_{\rm si}$ is the static surface charge density of silicon, $\epsilon_{\rm si}$ is the permittivity of silicon, $\beta = q/k_bT$ (q is the electronic charge, k_b is the Boltzmann's constant and T is the absolute temperature), $L_D = \sqrt{\epsilon_{\rm si}/qp_{\rm po}\beta}$ is the extrinsic Debye length for hole, $\psi_{\rm si}$ is the electrical potential at silicon surface, and $n_{\rm po}, p_{\rm po}$ are the equilibrium densities of electrons and holes respectively. The static electric field in the space between the tip and the sample surface is zero because electrostatic force is abolished by altering the offset voltage $(V_{\rm off})$ [17]. Therefore, the total charge density of high-κ/si structure is also zero:

$$\int \rho_h(z)dz + \sigma_i + \int \rho_{\rm si}(z)dz = 0 \tag{2}$$

where $\rho_h(z)$ is the trapped charge density in the high-κ Er_2O_3 film (units: traps/cm^3) and σ_i is the trapped charge density at the high-κ/Si interface (units: traps/cm^2). Assuming $\rho_h(z)$ is uniform i.e., $\rho_h(z) = \rho_h$ subsequently using Gauss' law, we get:

$$\begin{aligned}{\rm CPD} &= \psi_{\rm si} + \Delta V_h + \Delta V_i \\ &= \psi_{\rm si} + \rho_h t_h\left(\frac{t_h}{2\varepsilon_h}+\frac{t_i}{\varepsilon_i}\right) + \sigma_i\frac{t_i}{\varepsilon_i}\end{aligned} \tag{3}$$

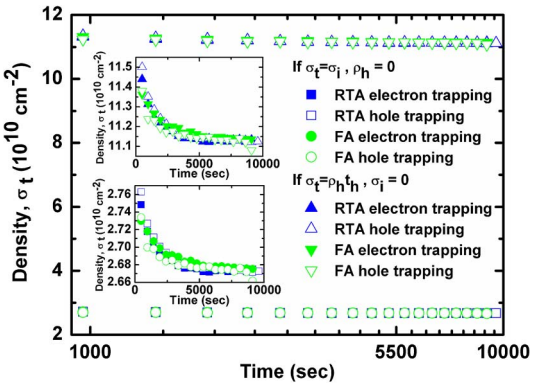

Fig. 5. The total charge density (σ_t)–time plot, converted from CPD values assuming extreme charge distribution conditions. The inset shows the magnified view of density ranges for both charge distribution conditions to signify the exponential decay in charge density with time.

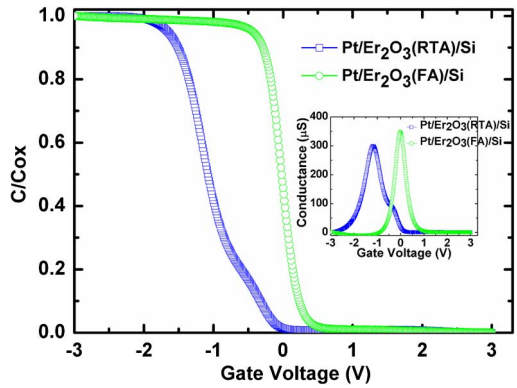

Fig. 6. Normalized capacitance v/s gate voltage characteristics for RTA and FA Pt/Er_2O_3/Si, MOS Capacitor. Inset shows the conductance (G)–gate voltage (V) characteristics for RTA and FA Pt/Er_2O_3/Si, MOS Capacitors.

where ϵ_h, ϵ_i and t_h, t_i are the dielectric constant and thickness of the high-κ, interface layer respectively. The total trapped charge density can be expressed as:

$$\sigma_{\rm si} = -\sigma_t = -\sigma_i - \rho_h t_h \tag{4}$$

where σ_t is the total trap charge density (units: traps/cm^2).

The relationship between CPD and σ_t can be obtained from Eqs. (1), (3) and (4) provided σ_i and ρ_h are known. However, the values of σ_i and ρ_h have not been determined up till now, therefore the assumption of two extreme charge distribution conditions i.e., (I) $\sigma_t = \sigma_i$ and $\rho_h = 0$, (II) $\sigma_t = \rho_h t_h$ and $\sigma_i = 0$ are taken. The real value of σ_t at any time t lies in between these two extreme charge distribution conditions. Here the values of trap charge density was calculated by assuming the value of $\psi_{\rm si}$ to be -6.83×10^3 corresponding to CPD of 0.2 V with impurity concentration of p-type silicon $N_A = 1.3 \times 10^{15}$ cm^{-3} [17].

Fig. 5 shows the calculated total charge density (σ_t) for the above two extreme charge distribution conditions for FA and RTA Er_2O_3/Si samples. The higher charge density in case of rapid thermal treated Er_2O_3/Si, evidences higher number of traps in RTA Er_2O_3/Si samples. The higher number of traps in post deposition treated RTA Er_2O_3/Si structure can be either due to higher number of Er_2O_3/Si interface traps or effective oxide traps. Usually, with rapid thermal treatment reduction in interface traps is observed due to structural reorientation in high-κ/semiconductor interface provided sufficient annealing time [23]. So, increase of trap density in RTA treated Er_2O_3/Si structure may be due to increase in effective oxide traps in Er_2O_3 after rapid thermal treatment. This higher number of trap charges in Er_2O_3 (RTA)/Si, system can be confirmed by the capacitance–voltage characteristics of the MOS Capacitors. Therefore, in order to further verify the reliability of KPFM for direct investigation of charge trapping in high-κ/Si structure, the Pt/Er_2O_3/Si, MOS Capacitor was fabricated to calculate the trap density via macroscopic electrical measurements.

Fig. 6 shows the capacitance–voltage (C–V) characteristics of Pt/Er_2O_3/Si, MOS Capacitor with different post deposition annealing treatments i.e., FA and RTA. The C–V measurements were performed by sweeping the gate voltage from +3 V [inversion] to −3 V [accumulation] at 100 KHz frequency. The flat band voltage $(V_{\rm fb})$, threshold voltage $(V_{\rm th})$, accumulation capacitance $(C_{\rm acc})$ as extracted from the C–V characteristics for post deposition RTA and FA Pt/Er_2O_3/Si, MOS Capacitors are ~ -1.48 V, ~ -0.07 V, $\sim$1.81 nF and ~ -0.26 V, $\sim$0.49 V, $\sim$2.06 nF respectively. The negative $V_{\rm fb}, V_{\rm th}$ in case of rapid thermal annealed (RTA) Pt/Er_2O_3/Si, MOS Capacitor again points to the presence of higher density of positive effective oxide charges that are created in oxides during rapid thermal treatment. However, to confirm the reason for negative flatband-voltage shift for post deposition RTA Pt/Er_2O_3/Si, MOS Capacitor it is desired to calculate the effective charge density $(N_{\rm eff})$ and interface trap density $(D_{\rm it})$ [24]. The total effective charges $(N_{\rm eff})$ is composed of fixed charges due to structural defects, trapped charge in oxide, and the possible presence of interface traps [25]. $N_{\rm eff}$ can be calculated by extracting the $V_{\rm fb}$ from the C–V curves and is given by:

$$N_{\rm eff} = \frac{C_{\rm acc}(\phi_{\rm ms} - V_{\rm fb})}{qA} \tag{5}$$

where $N_{\rm eff}$ is the effective oxide charge density (cm^{-2}), $C_{\rm acc}$ is accumulation capacitance (F), $\Phi_{\rm ms}$ is metal–semiconductor work function (V), $V_{\rm fb}$ is flatband potential (V), A is gate area (cm^2).

The inset of Fig. 6, shows the G–V characteristics for post deposition RTA and FA treated Pt/Er_2O_3/Si, MOS Capacitor. This well-established conductance based technique is one of superlative approach to extract the interface trap densities. In order to evaluate the interface trap density, the parallel conductance (G_p) was extracted from the G–V curves (corrected for series resistance effects [25]) by subtracting the reactance of the oxide capacitance [26] we get:

$$G_p = \frac{\omega C_{\rm ox}^2 G}{G^2 + \omega^2 (C_{\rm ox} - C_p)^2} \tag{6}$$

where $\omega = 2\pi$f. The interface trap density, $D_{\rm it}$ (eV^{-1} cm^{-2}) can be extracted from the peak of the conductance curve $(G_{p\_\max})$ as [25], [27]:

$$D_{\rm it} = \frac{2.5}{qA}\frac{G_{p\_\max}}{\omega}. \tag{7}$$

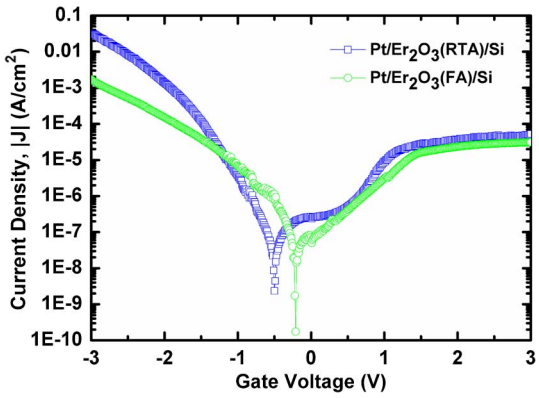

Fig. 7. Current density (J)–gate voltage (V) characteristics for RTA and FA Pt/Er_2O_3/Si, MOS Capacitors.

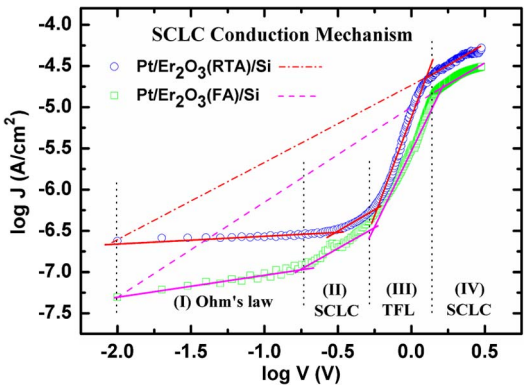

Fig. 8. Relation of log (J) vs. log (V) for positive applied voltage range from 0 to 3 V characteristics for RTA and FA Pt/Er_2O_3/Si, MOS Capacitor.

The $N_{\text{eff}}, D_{\text{it}}$ calculated using Eq. (5) and (7), for post deposition RTA and FA Pt/Er_2O_3/Si, MOS Capacitors are $\sim 1.3 \times 10^{13}$ cm^{-2}, $\sim 5.79 \times 10^{12}$ and $\sim 4.97 \times 10^{12}$ cm^{-2}, $\sim 5.96 \times 10^{12}$ cm^{-2} eV^{-1} respectively. Since a mild reduction in D_{it} is observed for post deposition RTA treated Pt/Er_2O_3/Si, MOS Capacitor, therefore, the contribution of acceptor-type interface traps is ruled out. This mild reduction in D_{it} may be due to structural re-orientation and relaxation at Er_2O_3/Si interface created during rapid thermal annealing treatment [23]. However, increase in N_{eff} for RTA treated Pt/Er_2O_3/Si, MOS Capacitors confirms that the negative flatband-voltage shift in Pt/Er_2O_3/Si, MOS Capacitor is due to density of positive effective oxide charges that are generated during rapid thermal annealing treatment in erbium oxide. Thus, furnace annealing (FA) treatment is desired for high quality erbium oxides as alternate gate dielectric for MOS based applications. Since interfaces provides dominant trap sites [20], thus, this significant variation in trap density (σ_t) calculated from KPFM measurement and N_{eff} computed from capacitance–voltage (C–V) measurement may be due to existence of additional traps sites at the metal–insulator interface (σ_{mi}) and can be described by the following relation:

$$N_{\text{eff}} \approx \sigma_t - \sigma_{\text{mi}} \tag{8}$$

Fig. 7 shows the leakage current density–gate voltage (J–V) characteristics of post deposition RTA and FA treated Pt/Er_2O_3/Si, MOS Capacitors. The leakage current density is observed to be $\sim 3.7 \times 10^{-6}$ and $\sim 6.74 \times 10^{-6}$ A/cm^2 @ -1 V in accumulation for post deposition rapid thermal annealed (RTA) and furnace anneal (FA), Pt/Er_2O_3/Si, MOS Capacitors. The lower leakage current density of ~ 6.74 μA/cm^2 @ -1 V in accumulation region for post deposition treated FA Pt/Er_2O_3/Si, MOS Capacitors reveals the feasibility of Er_2O_3 high-κ gate dielectric for MOS based device applications.

Further, to understand the charge decay mechanism in lift mode of KPFM, it is desired to first understand how the charges are distributed initially during charge injection at 3 V bias. For this conduction mechanism is studied for RTA and FA treated Pt/Er_2O_3/Si, MOS Capacitor. Fig. 8 shows the relation of log (J) vs. log (V) for RTA and FA Pt/Er_2O_3/Si, MOS Capacitors as extracted from Fig. 7. The J–V characteristics in log (J) vs. log (V) plane are confined within a "triangle" by three different regions Ohm's Law $(J \propto V)$, trap-filled-limit (TFL) curve and Child's Law $(J \propto V^2)$ and agrees with the space charge limited conduction theory [28]. The space charge forces have a significant role on electrical properties of insulators because they have small density of free charge carriers at room temperature and hence charge imbalance is created easily by electrical fields. The current density in these regions is given by the following equations [28]–[31]:

$$J_{\text{Ohm}} = q n_o \mu \frac{V}{d} \tag{9}$$

$$J_{\text{TFL}} = B\left(\frac{V^{l+1}}{d^{2l+1}}\right) \tag{10}$$

$$J_{\text{Child}} = \frac{9}{8}\mu\varepsilon\frac{V^2}{d^3} \tag{11}$$

where n_o is the concentration of free charge carriers in thermal equilibrium, B is an l-dependent parameter, $(l = T_c/T)$, T_c is characteristic temperature related to trap distribution, T is absolute temperature, V is the applied voltage, μ, d and ε are the mobility, thickness and dielectric constant in Er_2O_3 dielectric thin film.

Fig. 9 shows the distribution of carriers in Er_2O_3 dielectric to get a clearer picture of what is happening in regions of Fig. 8. In Region I (Ohm's law), at low gate voltage, carrier transit time (τ_c) is greater than dielectric relaxation time (τ_d), thus the injected charge density (σ_{inj}) is smaller than the thermally generated free carriers (n_o) in the dielectric, signifying injected charge (σ_{inj}) trapping in preexisting traps (σ_h) of Er_2O_3 dielectric i.e., all traps are not filled. Thus injected charge (σ_{inj}) will redistribute itself to sustain electric charge neutrality in a time analogous to τ_d. Here, the rearrangement of charge in dielectric is defined as dielectric relaxation. In Region II (SCLC), when carrier transit time (τ_c) becomes equal to dielectric relaxation time (τ_d) the traps are filled up and a space charge appears i.e., $\sigma_{\text{inj}} \sim n_o$. The voltage at which this transition from Region I

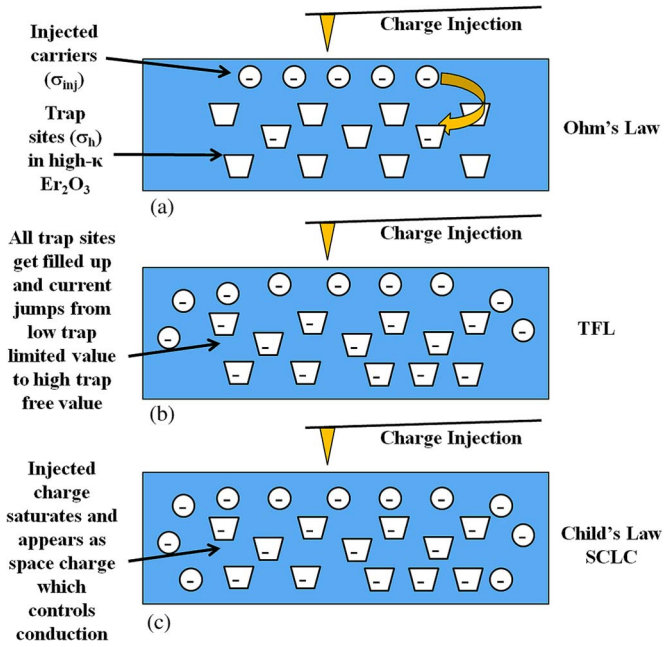

Fig. 9. Distribution of carriers in Er_2O_3 dielectric, (a) Ohm's law, (b) Trap-Filled-Limited (TFL) curve, and (c) SCLC conduction.

(Ohm's law) to Region II (SCLC) takes place is termed as transition voltage $(V_{\rm tr})$ [29], [30].

$$V_{\rm Tr} = \frac{8}{9} \times \frac{qn_o d^2}{\varepsilon\theta} \tag{12}$$

$$\theta = \frac{N_c}{g_n N_t} \exp\left(\frac{E_t - E_c}{k_b T}\right) \tag{13}$$

$$\tau_c = \frac{d^2}{\mu V_{\rm Tr}} \tag{14}$$

$$\tau_d = \frac{\varepsilon}{qn\mu} \tag{15}$$

where θ is the ratio of free carrier density to total carrier density, N_c is density of states in conduction band, N_t is trap density, g_n is degeneracy of the energy states in conduction band, E_t is trap energy level below E_c and n is the concentration of free carriers in insulator. In Region III (TFL curve), dielectric transition from trapped J–V curve to trap free J–V curve is observed. The current suddenly rises since all the traps are filled up and the available injected charge is free to move about in the dielectric. The voltage at which this transition from Region II (SCLC) to Region III (TFL) takes place is termed as trap-filled-limit voltage $(V_{\rm TFL})$. So, in this region current rapidly jumps from low trap limited value to high trap free space charge limit current [29], [30].

$$V_{\rm TFL} = \frac{qN_t d^2}{2\varepsilon}. \tag{16}$$

In Region IV (SCLC), at high gate voltage, the charge inside the dielectric gradually gets saturated. The current is entirely controlled by the space charge, which restricts extra injection of carriers in the dielectric. The $V_{\rm tr}, V_{\rm TFL}$ for post deposition RTA and FA treated $Pt/Er_2O_3/Si$, MOS Capacitors as extracted from log(J)-log(V) plot are ∼0.3 V, ∼0.57 V And ∼0.19 V, ∼0.57 V respectively. Since, $V_{\rm tr}$ is right shifted by ∼0.11 V for RTA treated $Pt/Er_2O_3/Si$, MOS Capacitors signifying higher oxide traps since it takes higher voltage for filling all traps. Note that, the offset of Region IV is corresponding to 3 V gate voltage, and we have a picture that looks something like, all trap sites are filled and dielectric is saturated with injected charge distributed throughout the dielectric. So, this picture is corresponding to the situation of Er_2O_3 dielectric, after charge injection and before KPFM measurement. Now, it becomes easy to analyze the decay mechanism of the injected charge. Thus, it can be attributed that, the rapid decay in CPD value for the initial 4000 sec (shown in Fig. 4.), is due to the space charge decay to the silicon substrate and after 4000 sec the slow decay can be related to decay of charges located in trap sites inside the dielectric.

IV. Conclusion

In Summary, charge trapping properties of post deposition rapid thermal and furnace annealed erbium oxide ultrathin films on silicon are systematically investigated by Kelvin probe force microscopy (KPFM) and $Pt/Er_2O_3/Si$, MOS Capacitor by capacitance–voltage technique. The trap density estimated for post deposition treated with RTA and FA Er_2O_3/Si structure varies from $\sim 3 \times 10^{10}$ to $\sim 11 \times 10^{10}$ $\rm cm^{-2}$ and for $Pt/Er_2O_3/Si$, MOS Capacitors are $\sim 1.3 \times 10^{13}$ $\rm cm^{-2}$, and $\sim 4.97 \times 10^{12}$ $\rm cm^{-2}$, respectively. It is envisaged that the trap density calculated from capacitance–voltage measurements is equal to sum of trap density calculated from KPFM and traps at the metal–insulator interface. Also, post deposition rapid thermal treatment resulted in higher density of effective oxide charges as compared to furnace annealing treatment in $Pt/Er_2O_3/Si$, MOS Capacitors. Moreover, lower leakage current density of $\sim 6.74 \times 10^{-6}$ A/cm^2 @ -1 V for post deposition FA $Pt/Er_2O_3/Si$, MOS Capacitors reveals the possibility of Er_2O_3 high-κ gate dielectric for MOS based device applications. Finally, the charge injection and decay mechanism is explained on the basis of space charge limited conduction mechanism. This study may help to fill the gaps between KPFM and capacitance–voltage based electrical measurements for trap density estimation and might provide direct investigation of charge trapping in high-κ based ultrathin films before they can be employed for next generation nanoscale MOS based device applications.

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