Charge Trapping Analysis of Metal/Al₂O₃/SiO₂/Si, Gate Stack for Emerging Embedded Memories

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Abstract—For Al_2O_3 charge trapping analysis, Metal/Al₂O₃/SiO₂/Si (MAOS) structures fabricated are from atomic layer deposition and plasma enhanced chemical vapor deposition-based Al2O3 and SiO2 thin films, respectively. The fabricated MAOS devices showed high memory window of ~7.81V@16V sweep voltage and leakage current density of $\sim 3.88 \times 10^{-6}$ A/cm²@-1V. The charge trapping and decay mechanism are investigated with the variation of alumina thickness by Kelvin probe force microscopy (KPFM). It reveals that vertical charge decay is a dominant phenomenon of charge loss for Al₂O₃ in contrast to lateral charge spreading. Constant current stress (CCS) measurements mark the location of charge trap centroid at ~10.30 nm from metal/Al₂O₃ interface attributes that bulk traps present close to the Al₂O₃/SiO₂ interface are dominant charge trap centres. In addition, a simple method is proposed to estimate the trap density using KPFM and CCS method at room temperature. Furthermore, there is $\sim 28\%$ exponential decay in high state capacitance observed after 10⁴ s in capacitance-time analysis at room temperature. This material engineering of charge traps will improve the performance and functionality of bilayer Al₂O₃/SiO₂ structure for embedded memory applications.

Index Terms—Charge trapping, high- κ , aluminium oxides (Al₂O₃), atomic layer deposition (ALD), Kelvin probe force microscopy (KPFM), memory.

I. INTRODUCTION

T HE miniaturization of metal-oxide-semiconductor-fieldeffect-transistors (MOSFET) is a major driving force behind the growth of semiconductor industry to obtain high performance and low cost electronic devices [1]. As the device feature size is continuously shrinking to the nano-metric regime, the universal gate oxide (SiO₂) approaches towards ~1nm which results in excessive leakage current and originates large static power dissipations [2]. Therefore, to meet the ITRS 2020 technology node [1], [3] stringent requirements, a compatible high dielectric constant (high- κ) material is required with optimal performance and reliability to suppress the leakage current. Numerous, high- κ materials have

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been investigated in the past decade, such as Al_2O_3 , Er_2O_3 , Sr₂O₃, HfO₂, ZrO₂, La₂O₃, and TiO₂ etc., to replace the traditional SiO₂ gate dielectric for next-generation cuttingedge complementary metal oxide semiconductor (CMOS) technology [4]. However, it has been observed that dielectric constant of alternate materials should not be too large, because higher- κ results in the fringing field induced barrier lowering based short channel effect [5]. Besides this, the deposition of high- κ material onto active silicon, results in the formation of a poor quality uncontrollable interfacial layer which decreases the effective dielectric constant, channel mobility and device reliability [6]. Therefore, a high quality SiO₂ ultrathin film is generally grown/deposited onto active silicon surface before depositing high- κ material to decrease the interfacial mismatch of high- κ /Si system [6]. Moreover, the device dimensions scale more rapidly as compared to the supply voltage with each successive IC's technology node. Thus, the increase in effective electric field with the scaling of device feature size is at a higher rate and originates various reliability issues [7], [8]. Hence, as the device dimensions scale down to the nano-metric regime the methodical investigations of charge trapping, breakdown characteristics, interface endurance etc. of high- κ material becomes extremely important from reliability view point of end users. Especially, for embedded charge trapping based flash memories, which offer a smaller cell size, lower program/erase voltage and high reliability, contrary over the conventional floating gate flash memories [1]. Albeit in charge trapping memories tunneling, trapping and blocking oxide based tri-layer stack is principally used as storage media [9]. Scaling derived the channel length reduction much faster than the gate stack thickness and attribute to the cross coupling between gate stacks of adjacent cells [10]. Recently, bi-layer (trapping and tunneling) based structures have attracted much attention instead of tri-layer due to exclusion of thicker blocking layer from gate stack for flash memories applications. The advantages of bi-layer gate stack is such that if the charges are made to trap in deep defect sites of trapping layer or close to the tunneling and trapping layer interface then there is no need of blocking layer [11]. In bi-layer gate stacks, Si_3N_4 [12], Al_2O_3 [13], HfO₂ [11], [14] and TiO₂ [15] deposited/grown with various techniques have been investigated for both CMOS and memory applications in past few years, while the charge trapping mechanism is still not well understood. Among, high- κ materials, aluminium oxide/alumina (Al2O3) has attracted much attention because of moderate dielectric constant (~ 10), high

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band gap (\sim 5.1-8.8 eV), higher thermal-kinetic stability and few bulk electrically active defects [16], [17].

There are various deposition techniques, physical (e-beam evaporation, sputtering etc.) and chemical (plasma enhanced chemical vapour deposition (PECVD), atomic layer deposition (ALD) etc.) listed in literature to deposit Al_2O_3 films [16], [18]–[20]. Recently, ALD has attracted much attention because of its superior uniformity, high quality oxide and precise thickness control [16]. Consequently, ALD based Al_2O_3 is reported as an alternate gate oxide for CMOS applications, passivation layer for solar cells, top blocking oxide in flash memories and embedded Electrically Erasable Read Only Memory (EEPROM) applications [13], [16].

In literature, there are few investigations on bi-layer gate stack for Metal-Aluminium-Oxide-Silicon (MAOS) structure. Even if, the concept of bi-layer gate stack [21]-[23] emanated before the first proposed concept of tri-layer gate stack like Silicon - Oxide - Nitride - Oxide - Silicon (SONOS) [9], Metal - Oxide - High- κ - Oxide - Silicon (MOHOS) [24] and TaN - Al₂O₃ - Si₃N₄ - Oxide - Si (TANOS) [25]. Recently, Zhang et al. [11] reported considerable memory window for bi-layer gate stack based on thick HfO_2 (~55 nm) trapping layer and motivated the scientific community to make an effort for alternate high- κ materials, as this may be a step forward to reduce the gate stack thickness with reduced fabrication steps, cost and hence overcome the coupling capacitance issues for next generation IC's technology node. Austin et al. [3] described that the Al₂O₃/SiO₂ bi-layer stacks meets ITRS 2020 node for Metal-Insulator-Metal (MIM) structure. Hence, it is worthwhile to investigate the charge trapping of alumina in Al₂O₃/SiO₂, bi-layer gate stacks for diverse applications ranging from CMOS, MIM structure, passivation layer for solar cells, blocking oxide in flash memories and embedded Electrically Erasable Read Only Memories (EEPROM) device applications.

Conventionally, the memory characteristics of semiconductor devices are investigated by macroscopic electrical characterization techniques such as Capacitance-Voltage (C-V), and Current density-Voltage (J-V) measurements etc. But these measure the averaged property over gate area of the device and are insensitive to variations at nanoscale, therefore termed "macroscopic" [26]-[28]. Nevertheless, as the device feature size incessantly shrinks to the nanometric regime, the traps/defects in gate oxide have inevitable effect on the performance of memory devices. Hence, advanced characterization methods with high lateral resolutions are required to investigate highly localized electrical properties at nano-metric regime [28], [29]. In this respect, Atomic Force Microscope (AFM) based Kelvin Probe Force Microscopy (KPFM) technique is adequate for charge trapping analysis of gate stacks and gives direct investigation of charges from the surface of ultrathin films at localized nano-metric regime, hence termed "nanoscopic" [30], [31]. In this method, initially charges are injected into the dielectric through a conductive tip which plays the role of metal gate over the bare dielectric surface forming nano-meter size device (few hundred nm²), followed by KPFM measurement which detects the potential difference between the tip and thin film surface [32], [33]. This non-destructive advanced KPFM technique will engineer the performance and functionality of memory devices by tuning the defects/trap sites of dielectrics at nanoscale.

In this work, we systematically investigated the Al/Al₂O₃/SiO₂/Si, MAOS structure to study the charge trapping characteristics and the location of trap centroid in MAOS devices. The multilevel memory characteristics are measured by capacitance-voltage (C-V) characteristics. Subsequently, the pre & post-breakdown and leakage characteristics are evaluated by the current density-voltage (J-V) characteristics. Consequently, the charge trapping in Al₂O₃/SiO₂/Si, system is investigated by KPFM technique with variation in thickness of alumina to predict the nature of trap sites. Moreover, a simple method is proposed to estimate the trap density using KPFM at room temperature. Further, the charge trapping centroid, trap density are estimated by the constant current stress (CCS) method using voltage-stress time measurements. Thereafter, the retention characteristics are evaluated by the capacitance-time (C-T) measurements at room temperature.

II. EXPERIMENTAL PROCEDURES

The structures of Al₂O₃-SiO₂-Si and Al-Al₂O₃-SiO₂-Si were fabricated on p-type Si (100) substrate with resistivity of 2-10 Ω -cm. After standard RCA cleanings, deposition of ultrathin SiO₂ films was carried out by PECVD. The substrate was maintained at 390 °C throughout the PECVD deposition process. The tetraethoxysilane (TEOS) was supplied to the process chamber with inert Ar gas where it reacted with O₂ to form SiO₂ ultrathin films. Subsequently, the growth of Al_2O_3 thin films was carried out by remote plasma enhanced ALD in a Plasma electronics ALD system using trimethylaluminium (TMA), O₂ as oxidant precursors and Ar as carrier purge gas at temperature of 250 °C using 100 cycles. For gate electrodes, Al thin film (\sim 600 nm) was deposited by Sputtering at 3.9×10^{-2} torr pressure of Ar and circular gate electrodes of area 80.45×10^{-5} cm² are patterned through the standard photolithography and chemically etching techniques. The thickness of deposited SiO₂ and Al₂O₃ thin films is ~ 6.15 nm and ~ 13.68 nm, respectively measured by ellipsometer. To study the effect on trap centroid with Al₂O₃ thickness using CCS measurement, another set of MAOS structure is fabricated for reference using similar fabrication steps but with different high Al₂O₃ thickness of ~48.80 nm. The C-V, J-V, CCS voltage-stress time and C-T measurements were carried out at room temperature using KEITHLY 4200 SCS system. The KPFM measurements were performed using AFM (Dimension Icon from Bruker) at room temperature. The conducting MESP Co/Cr coated AFM probes (from Bruker) with frequency, 60-100 kHz and spring constant, 1-5 N/m are used for the charge injection and KPFM study. Initially, the charge injection on ultrathin Al₂O₃/SiO₂/Si surfaces is performed under standard AFM contact mode. For charge injection, -3 and +3 V bias are applied to the tip for electrons and holes injection respectively, in 200 nm lateral direction along x-axis on Al₂O₃/SiO₂/Si system for optimum time (injected charge saturation) of 10 min and the substrate

kept at ground potential. Afterwards, for the CPDs analysis (KPFM measurement), the images of injected charges are visualized under non-contact (lift) mode with the optimized lift height (minimizes the interference between the tip and the sample) of ~ 100 nm. CPDs data acquisition is accomplished in interleaved line by line scan mode with sample topography analysis and an a.c. bias of 500 mV is applied to the tip. KPFM measurement of the sample surfaces are attained with the cantilever vibrating at a slightly lower frequency $(\sim 2 \text{ KHz})$ than its resonance frequency and at a probe scan rate of 0.99 Hz. Furthermore, the KPFM feedback parameters are augmented to an elevated magnitude for minimization of error profile. The protruding range of error profile with best contrast fit for KPFM imaging is found well below ± 2 mV. The KPFM images have been processed with Flatten tool of the Nanoscope 9 software, which fit each line individually to center the data (0th order). This remove any tilt in measurement so that the CPD value other than the injected area becomes zero and provides better comparison of different samples. In this analysis, contact potential difference magnitude variations with the time domain is computed by KPFM at a periodicity of 8 min. Albeit, all the KPFM micrographs based surface potential analysis accomplished in the form of contact potential difference (CPD) for Al₂O₃/SiO₂/Si systems are performed through the standard centre line profile scheme.

III. RESULTS AND DISCUSSION

То investigate the memory characteristics of Al/Al₂O₃/SiO₂/Si, MAOS structures, the high frequency (1 MHz) cyclic C-V measurements are carried out at room temperature. Fig. 1 shows the cyclic C-V characteristics of Al/Al₂O₃(13.68 nm)/SiO₂(6.15 nm)/Si, MAOS structures at different sweep voltages, measured by forward [inversion (V_g+) to accumulation (V_g-)] and reverse [accumulation (Vg-) to inversion (Vg+)] gate voltage sweeps. Here, memory window (ΔW) is defined by the difference in voltage corresponding to mid capacitance, measured from forward and reverse gate voltage sweeps, i.e., positive-negative-positive sweep. During forward sweep, initially high program voltage [positive gate voltage] result the inversion region and the corresponding electric field result the Fowler-Nordheim (F-N) tunneling of inversion charges (electrons) across SiO₂ (tunneling layer) and fill the available trap sites of Al₂O₃. It consequences the right shift in threshold voltage. Similarly, during reverse sweep, high erase voltage [negative gate voltage] in accumulation region result the F-N tunneling of accumulation charges (holes) across SiO₂ and recombine with already existing electrons stored in trap sites (forward sweep) consequences left shifted threshold voltage and C-V curves. Henceforth, the existence of anticlockwise memory window signifies the charge trapping in Al/Al₂O₃/SiO₂/Si, MAOS system. The noteworthy increase in memory window from ~ 0.54 V@4V to ~ 7.81 @16V attributes the increase in charge trapping with increase in electric field. The high memory window of $\sim 7.81 V@16V$ supports the potential candidature of Al/Al₂O₃/SiO₂/Si, MAOS structure for reliable multilevel data storage applications. However, on increasing the sweep



Fig. 1. C-V characteristics of Al / Al_2O_3 (13.68 nm) / SiO₂ (6.15 nm) / Si, MAOS structure at different sweeping voltages and 1MHz frequency. Inset shows the variation of memory window with sweep voltage for Al / Al_2O_3 (13.68 nm) / SiO₂ (6.15 nm) / Si, MAOS devices.



Fig. 2. J-V characteristics of Al / Al_2O_3 (13.68 nm) / SiO₂ (6.15 nm) / Si, MAOS structures pre-breakdown and post-breakdown. The inset shows the J-V characteristics post-breakdown for MAOS capacitors from -15 to +15V gate voltage.

voltage above 16 V the C-V characteristics of devices are observed to distort [not shown here]. Furthermore, there is sudden variation in ΔW (inset of Fig. 1) noticed as depicted from Fig. 1 for variation of gate voltage sweep from 14 V [Fig. 1 inset (Q)] to 16 V [Fig. 1 inset (P)]. To establish this anomalous behaviour at high electric fields, it is anticipated to study the current density-voltage (J-V) characteristics of devices.

Fig. 2 shows the J-V characteristics (|J|/V) of Al/Al₂O₃ (13.68 nm)/SiO₂(6.15 nm)/Si, MAOS structures. Initially, the gate voltage is varied from 0 to 16 V to measure the breakdown voltage of the MAOS devices. There is a sharp increase in current density noticed at ~14.2 V corresponding to an electric field (E = V_g/t_{stack}) of ~7.16 MV/cm, where t_{stack} is the thickness of gate stack. Besides this, it is observed that the breakdown voltage of devices varied from ~14.2 to ~15.5 V across the wafer. Moreover, this behaviour is probably due to soft breakdown of Al₂O₃ or SiO₂ thin films which occurs due to the presence of traps and leads to unstable conducting paths in the dielectric system [39]. When the device breaks down, it reaches a current density of 1 A/cm², where 1A/cm² is set as the compliance of the parameter analyser, which is generally set to prevent the excess heating of the device in case of breakdown. Therefore, it is proven that the distorted C-V curves of Fig. 1. at above ~ 16 V (not shown) is owing to the electric field breakdown at high field than the breakdown of MAOS devices. Ensuing this, the post-breakdown J-V characteristics are measured and followed the typical behaviour. Although, during the post-breakdown curve, current density is higher as compared to the pre-breakdown curve which attributes to the creation of more number of defect states during soft breakdown in Al₂O₃/SiO₂ thin films that results in higher current density in post-breakdown curves. Further, the JJI/V characteristic for post breakdown devices from -15 V to +15 V is shown in inset of Fig. 2. In general, lower leakage current density is desired for low static power dissipations in semiconductor devices. The measured current density of ~ 12 nA/cm² for pre breakdown devices and $\sim 3.88 \ \mu A/cm^2$ for post breakdown devices at -1 V gate voltage indicates the lower leakage current for Al/Al₂O₃/SiO₂/Si, MAOS system and its viability for CMOS technology and particularly ($\Delta W \sim 7.81 \text{V}@16 \text{V} \& |\text{J}|$ \sim 3.88 x 10⁻⁶ A/cm²@-1V) for EEPROM applications. Next, an interesting question arises that whether Al₂O₃ or SiO₂ layer will breakdown first in the MAOS system. Generally, the breakdown field (E_{bd}) is inversely proportional to the dielectric constant (ε), with relation, $E_{bd} \propto \varepsilon^{-0.65}$. For instance, SiO₂ has the lowest dielectric constant and highest breakdown field whereas Al_2O_3 has high dielectric constant and low breakdown voltage/strength due to high local electric field. This high local electric field in high dielectric constant material (Al₂O₃) distorts/weakens the polar molecular bonds and increases the probability of bonds breakage in accordance with standard Boltzmann process and/or by hole capture [38]. So, for MAOS gate stacks alumina layer with high dielectric constant is expected to breakdown first and then the SiO₂ layer. However, this is not the sole criteria for confirming which layer will breakdown first in MAOS gate stack. As, there may be different voltages across both alumina and buffer layer which are generally calculated for bilayer gate stack by the following relation [37], [39]:

$$\frac{V_{Al_2O_3}}{V_{SiO_2}} = \frac{t_{Al_2O_3}}{t_{SiO_2}} \frac{\varepsilon_{SiO_2}}{\varepsilon_{Al_2O_3}} \tag{1}$$

where V_{A12O3} , t_{A12O3} , ϵ_{A12O3} and V_{SiO2} , t_{SiO2} , ϵ_{SiO2} are the voltage, thickness, dielectric constant of Al_2O_3 and SiO_2 thin films respectively. So, depending upon the voltage across each layer, which layer will breakdown first can be easily estimated. e.g.: $Al/Al_2O_3(13.68 \text{ nm})/SiO_2(6.15 \text{ nm})/Si$, MAOS system with, $t_{A12O3} = 13.68 \text{ nm}$, $\epsilon_{A12O3} = 9$, $t_{SiO2} = 6.15 \text{ nm}$, $\epsilon_{SiO2} = 3.9$, the ratio V_{A12O3}/V_{SiO2} is $\sim 24:25$. Therefore, for an applied voltage of 16V, the voltage across Al_2O_3 is $\sim 7.85 \text{ V}$ and SiO_2 is $\sim 8.15 \text{ V}$ corresponding to an electric field of ($E_{bd_A12O3}=V_{A12O3}/t_{A12O3}$) $\sim 5.74 \text{ MV/cm}$ and ($E_{bd_SiO2}=V_{SiO2}/t_{SiO2}$) $\sim 13.2 \text{ MV/cm}$ across Al_2O_3 and SiO_2 ,



Fig. 3. Normalized C-V characteristics of Al / Al_2O_3 (13.68 nm) / SiO_2 (6.15 nm) / Si, MAOS structure with variation in frequency.

respectively. Hence, the applied electric field across SiO_2 layer is close to the breakdown field of SiO_2 [38], therefore SiO_2 layer is expected to breakdown first for the fabricated MAOS devices and Al_2O_3 layer maintains the reliability of the bilayer MAOS system by preventing hard breakdown.

Further, to confirm the observed memory window is due to charge trapping and not due to random variations, it is anticipated to measure the C-V characteristics with variation in frequency. Fig. 3 shows the normalized cyclic C-V characteristics of Al/Al₂O₃ (13.68 nm) / SiO₂ (6.15 nm) / Si, MAOS structure with variation in frequency, measured by forward [inversion (V_g+) to accumulation (V_g-)] and reverse [accumulation (V_g-) to inversion (V_g+)] gate voltage sweeps. The significant variation in flatband voltage (V_{fb}) of ~ 0.95 V and right shifted C-V curves with variation in frequency from 1MHz to 10 KHz is attributed to the frequency dependent trapping states in the Al/Al₂O₃/SiO₂/Si, MAOS system [42]. For instance, when gate voltage is positive, the MAOS device is in inversion region and occupied by minority charge carrier electrons. These electrons get trapped in the trap sites/slow states. At lower frequencies, when the voltage is swept from inversion to accumulation, these negative traps respond to the lower frequencies of the applied voltage and result in right shifted V_{fb} and C-V curves [42]. Nevertheless, the memory window is counter-clockwise and there is negligible variation in memory window with variation in frequency that confirms that the observed memory window is due to charge trapping and not due to dielectric polarization or ionic displacement [43].

To establish a better understanding about the MAOS device memory characteristics the systematic investigation of charge trapping is needed to be explored. In principal, there are two charge trapping possibilities: (i) either the charge may be stored in the bulk traps of high- κ Al₂O₃ thin films as previously reported by You and Cho [14] for HfO₂, or (ii) at the SiO₂-Al₂O₃ interface. For this KPFM analysis are performed on Al₂O₃(13.68 nm)/SiO₂/Si and Al₂O₃(48.80 nm)/SiO₂/Si system to compute the contact potential difference (CPD) values. If the charge trap sites are uniformly distributed in Al₂O₃, then the initial CPD value



Fig. 4. Measured CPD line profiles of (a) hole trapping and (b) electron trapping in $Al_2O_3/SiO_2/Si$, system. The bright and dark regions in inset images show the trapped holes and electrons, for MAOS system with variation in alumina thickness of 13.68 nm (c), (e) and 48.80 nm (d), (f), respectively.

will be proportional to thickness of Al₂O₃, i.e., higher initial CPD value for higher Al₂O₃ thickness. On the other hand, if the charge trap sites are distributed at the interface, then the initial CPD value will be nearly similar for both systems [31]. Fig. 4. shows the initial measured CPD line profiles after the holes [Fig. 4(a)] and electron injection [Fig. 4(b)] on the Al₂O₃(13.68 nm)/SiO₂/Si and Al₂O₃(48.80 nm)/SiO₂/Si system, respectively. The line profiles are obtained by scanning a horizontal line across the injection center in the 2-D potential image. The inset of Fig. 4 shows the KPFM images of Al₂O₃(13.68 nm)/SiO₂/Si [Fig. 4 (c), (e)] and Al₂O₃(48.80 nm)/SiO₂/Si [Fig. 4 (d), (f)] systems, where the bright and dark regions denote the trapped holes and electrons, respectively. The observed CPD value of holes, electrons are \sim 393.74, \sim -345.3 and \sim 228, \sim 200.1 mV for Al₂O₃ (13.68 nm)/SiO₂/Si and Al₂O₃(48.80 nm)/SiO₂/Si system, respectively. The higher initial CPD value for Al₂O₃(48.80 nm)/SiO₂/Si system, signifies that charge trap sites are uniformly distributed in bulk of Al₂O₃. Further, to observe the retention of charges in both systems, it is imperative to observe the charge decay using CPD values over time.

Fig. 5 shows the variation of computed CPD values from KPFM analysis with time for Al₂O₃(13.68 nm)/SiO₂/Si and Al₂O₃(48.80 nm)/SiO₂/Si systems, measured after consecutive 8 min interval at room temperature. From the measured CPD values over fixed time interval, it is observed that the CPD value decays rapidly in initial 4000 sec as compared to the increase in diameter of bright and dark spot over time as shown in inset of Fig. 5. Thus, it is attributed that vertical leakage is the dominant mechanism for charge leakage rather than lateral charge spreading [34], [44]. Also, it is visibly observed that the measured CPD values decays exponentially for both systems independent of alumina thickness. But, for Al₂O₃(48.80 nm)/SiO₂/Si system the CPD value is higher even after extended time of 10^4 sec signifying that the trap charges are held in the bulk of Al₂O₃ and proportional to the thickness of alumina. Furthermore, the approximate total traps charge density (units: traps/cm²) is calculated from the CPD measurements, with the help of one-dimensional (1-d) Poisson equation as follows [30], [31], [40], [41]:

$$\sigma_{si}(\sigma_i, \rho_t) = \int \rho_{si}(z) dz$$

= $\mp \frac{\sqrt{2}\varepsilon_{si}}{\beta L_D} \left\{ \begin{bmatrix} \exp(-\beta\psi_{si}) + \beta\psi_{si} - 1 \end{bmatrix} + \frac{n_{po}}{p_{po}} \begin{bmatrix} \exp(\beta\psi_{si}) - \beta\psi_{si} - 1 \end{bmatrix} \right\}^{1/2}$
(2)



Fig. 5. The variation of CPD values with aging after charge (holes or electrons) injection, for MAOS system with variation in alumina thickness of 13.68 nm and 48.80 nm, respectively. The inset shows the KPFM images of injected charges (holes or electrons) scanned after 8 min and 152 min for MAOS system with variation in alumina thickness of 13.68 nm and 48.80 nm signifying vertical leakage is the dominant mechanism for charge leakage rather than lateral charge spreading.

where σ_{si} is the static surface charge density of silicon, \in_{si} is the relative permittivity of silicon, ψ_{si} is the electrical potential at surface of silicon, $\beta = q/k_bT$ (q is the electronic charge, k_b is the Boltzmann's constant and T is the absolute temperature), $L_D = \sqrt{\in_{si}/qp_{po}\beta}$ is the extrinsic Debye length for hole, and n_{po} , p_{po} are the equilibrium densities of electrons and holes respectively. In the KPFM measurement, the static electric field between the sample and the tip is nullified by varying the offset voltage (V_{off}). The static electric field in the space between the tip and the sample surface is zero because electrostatic force is abolished by altering the offset voltage (V_{off}) [30]. Hence, the total charge density of high- κ /si system is also zero:

$$\int \rho_h(z)dz + \sigma_i + \int \rho_{si}(z)dz = 0$$
(3)

where $\rho_h(z)$ is the density of trap charges in the high- κ Al₂O₃ film (units: traps/cm³) and σ_i is the density of trap charges in the SiO₂ film (units: traps/cm²). Consequently, using Gauss' law with the assumption that $\rho_h(z)$ is uniform, i.e., $\rho_h(z) = \rho_h$, we get:

$$CPD = \psi_{si} + \Delta V_h + \Delta V_i$$

= $\psi_{si} + \rho_h t_h \left(\frac{t_h}{2\varepsilon_h} + \frac{t_i}{\varepsilon_i}\right) + \sigma_i \frac{t_i}{\varepsilon_i}$ (4)

where \in_h , \in_i and t_h , t_i are the dielectric constant and thickness of the high- κ , interface layer respectively. The total trapped charge density can be expressed as:

$$\sigma_{si} = -\sigma_t = -\sigma_i - \rho_h t_h \tag{5}$$

where σ_t is the total trap charge density (units: traps/cm²).

Using equations (2), (4) and (5), the relationship between CPD and σ_t can be obtained provided σ_i and ρ_h are identified. However, the value of σ_i and ρ_h have not been determined till now, therefore two extreme charge distribution conditions are assumed, i.e., (I) $\sigma_t = \sigma_i$ and $\rho_h = 0$, (II) $\sigma_t = \rho_h t_h$ and $\sigma_i = 0$.



Fig. 6. The total trap charge density (σ_t) – time plot, extracted from the CPD values with the assumption of extreme charge distribution boundary conditions. Here, the inset shows the magnified view of trap density to signify the exponential decay in charge density with time for both boundary conditions.

The exact value of σ_t at a time t lies amongst these two extreme charge distribution boundary conditions. Here the values of charge density is calculated by assuming the value of $\Psi_{si} \sim$ -6.83×10³/cm = -5.51×10⁷ V analogous to CPD of 200 mV and impurity concentration of p-Si N_A=1.3×10¹⁵ cm⁻³ [30].

Fig. 6 shows the calculated total trap charge density (σ_t) for the aforesaid two extreme charge distribution boundary conditions for Al₂O₃/SiO₂/Si structure. The inset shows the magnified view of trap density to signify the exponential decay in charge density with time for both boundary conditions. The charge density for Al₂O₃/SiO₂/Si structure varies from $10^{12}-10^{15}$ traps/cm². Here, it is interesting to note that the trap density decay with aging is negligible in this above method and is not much sensitive to CPD value especially for analysis at room temperature.

Here, an exciting question arises that what is the effect of lift height, i.e., the tip and sample separation distance on the measured CPD values. Fig. 7 shows the effect of lift height on CPD value for Al₂O₃/SiO₂/Si structure after Hole injection at 3V. It is observed that the CPD value increases from ~ 0.23 to ~ 0.79 V and the diameter of the injected charge area increases from ~ 0.92 to $\sim 1.68 \ \mu m$, with variation in lift height from 100 to 20 nm for Al₂O₃ (13.68 nm) / SiO₂ (6.15 nm) / Si, system. Here, the diameter of injected charge is defined as the full width at half maximum (FWHM) extracted from the Gaussian fit of the measured CPD line profiles (i.e., CPD-Position curves) of Al₂O₃ (13.68 nm) / SiO₂ (6.15 nm) / Si, system. Although, the increase of CPD value with decrease in lift height might be due to the averaging effect in KPFM where the tip surrounding area also contributes to the KPFM signal and hence to the CPD value [46]. Therefore, it is visualized that a more simple and efficient method is required for trap density computation that also takes into account the lift height of the KPFM tip.

Apart from the above mentioned conventional technique for trap density estimation, there is an alternate and simple method proposed for trap density estimation which includes



Fig. 7. Effect of lift height on CPD value for Al₂O₃/SiO₂/Si system after Hole injection at 3 V.



Fig. 8. The proposed simple trap density estimation method for oxide/ semiconductor systems.

the effect of lift height during CPD measurements, applicable to oxide/semiconductor systems as shown in Fig. 8. The total stored charges (Q_t , units: C/cm²) in trap sites is estimated by:

$$Q_t = C_t * V_{cpd} \tag{6}$$

where V_{cpd} is the contact potential difference between the tip and the sample measured from the KPFM technique and C_t is the total capacitance between the KPFM tip and the semiconductor substrate, i.e., series combination of capacitance of air (C_{air}) and oxide gate stack (C_{ox}) [45]. Here, the total capacitance is given by:

$$C_t = \frac{\varepsilon_o}{\left[\frac{l_{air}}{\varepsilon_{air}} + \frac{l_{ox}}{\varepsilon_{ox}}\right]} \tag{7}$$

Therefore, using equations (6) and (7), the total number of charges per unit area, i.e., charge density ($N_t = Q_t/q$, units: traps/cm²) stored in trap sites of MAOS devices is expressed as:

$$N_t = \frac{\varepsilon_o V_{cpd}}{q \left[\frac{l_{air}}{\varepsilon_{air}} + \frac{l_{ox}}{\varepsilon_{ox}} \right]}$$
(8)

where q is the electronic charge, \in_o is the permittivity of free space, \in_{ox} is the relative permittivity of oxide stack estimated



Fig. 9. The total trap charge density (σ_t) – time plot, estimated using the proposed method of equation (8), for MAOS system with variation in alumina thickness of 13.68 nm and 48.80 nm.

from C-V characteristics in accumulation region, t_{ox} is the thickness of gate stack, \in_{air} is the permittivity of air (~1) and tair is the lift height during CPD measurements. Using equation (8), the total trap charge density (N_t) is calculated for Al₂O₃ (48.80 nm)/SiO₂/Si and Al₂O₃ (13.68 nm)/SiO₂/Si structures. Fig. 8. shows the variation of trap density (N_t) for Al2O3/SiO2/Si system with variation in alumina thickness of 13.68 nm and 48.80 nm, respectively. The initial trap density N_t is estimated to be ~1.07 x 10¹⁰ (electrons trap) and ~1.21 x 10¹⁰ (holes trap) traps/cm² for Al₂O₃ (13.68 nm)/SiO₂/Si structure, whereas $\sim 1.76 \times 10^{13}$ (electrons trap) and $\sim 2.01 \times 10^{13}$ 10¹³ (holes trap) traps/cm² for Al₂O₃ (48.80 nm)/SiO₂/Si structure. In addition, it is visibly observed from Fig. 9 that the trap density variation with time is much more sensitive to CPD value as compared to conventional method results shown in Fig. 6, where negligible variation in trap density is observed with decay in CPD value. Therefore, the proposed trap density estimation method is appropriate for KPFM measurements including the effect of lift height and much more sensitive to CPD value.

Next, an interesting question arises that how much is the role of interface traps and where in bulk of Al₂O₃ is the charge centroid located. To understand the aforesaid concern, to prove the existence of bulk traps and to study the variation in location of trap centroid with the Al₂O₃ thickness, the constant current stress (CCS) is an elegant method and extensively adopted to estimate charge trap centroid in bi-layer gate stacks [15]. If the charge trap sites are uniformly distributed in Al₂O₃, then the initial CPD value will be proportional to thickness of Al₂O₃, i.e., higher initial CPD value for higher Al₂O₃ thickness. On the other hand, if the charge trap sites are distributed at the interface, then the initial CPD value will be nearly similar for both systems [31].

Fig. 10. shows the charge trapping characteristic of MAOS structures with different Al₂O₃ thickness (\sim 13.68 nm & \sim 48.8 nm), to confirm the exact location of trap centroid and its variation with thickness of Al₂O₃. For CCS measurements, initially a constant current stress of 1 μ A/cm² is



Fig. 10. Charge trapping characteristics of Al/Al₂O₃/SiO₂/Si, MAOS Capacitors under constant current stress of 1 μ A/cm² with variation in Al₂O₃ thickness.

applied to gate electrode equivalent to total injected charge (Q_{total}) of ~100 μ C/cm². Thereafter, the voltage-stress time measurement is performed, which indicates the voltage drop across the Al₂O₃/SiO₂ stacked layer. This significant shift in voltage with stress time is attributed to the trapping of charges in the Al₂O₃/SiO₂ stack. It is proven and reported that single SiO₂ layer don't exhibit charge trapping characteristics in voltage-stress time measurement and shows negligible voltage shift [12], [14]. It confirms the proposed hypothesis that majority traps may reside at Al₂O₃ bulk or Al₂O₃/SiO₂ interface. Also, it is visibly observed from Fig. 10. that the voltage values for Al/Al₂O₃(48.80 nm)/SiO₂/Si system are higher as compared to Al/Al₂O₃(13.68 nm)/SiO₂/Si system, signifies higher trapping in system with higher alumina thickness, which supports the former KPFM analysis. Moreover, the location of majority trap sites in the Al₂O₃/SiO₂ stack is estimated by the computation of charge trap centroid. The charge trap centroid (X_{cent}) extracted by CCS measurements is computed by the following relation [12], [14]:

$$X_{cent} = \frac{t_{stack}}{\left[1 - \left(\Delta V_g^- / \Delta V_g^+\right)\right]} \tag{9}$$

where t_{stack} is the thickness of Al₂O₃/SiO₂ stack, ΔV_g^+ and ΔV_g^- are the positive and negative gate voltage shifts after constant current stress, respectively.

Using equation (9), the calculated value of X_{cent} is ~10.30 and ~30.73 nm for Al/Al₂O₃/SiO₂/Si, MAOS structure for corresponding alumina thickness of ~13.68 and ~48.8 nm, respectively. This signifies X_{cent} is located ~10.30 nm below the metal/Al₂O₃(~13.68nm) interface and hence close to the Al₂O₃/SiO₂ interface as shown graphically in Fig. 11. Thus, it attributes that the trap centroid moves closer to the Al₂O₃/SiO₂ interface with decrease in thickness of alumina. Analogous, observation was inspected and reported for Si₃N₄ and HfO₂ materials by Zhang *et al.* [11] and You and Cho [14]. Herein, it can be stated that bulk trap



Fig. 11. Schematic showing the estimated charge trap centroid in Al/Al_2O_3 (13.68 nm)/SiO₂ (6.15 nm)/Si, MAOS structure.

charges located close to Al₂O₃/SiO₂ interface are dominant trap centres for Al/Al₂O₃/SiO₂/Si, MAOS systems as shown in the schematic of Fig. 11. Thus, this charge centroid analysis reveals the engineering of localized or depth of charge traps or storage cells, and can be employed for the performance improvement of bi-layer gate stacks for memory applications. Further, the stored charges (ΔQ , units: C/cm²) in trap sites is estimated by $\Delta Q = C\Delta V_{th} = C (\Delta V_g^+ - \Delta V_g^-)$, where $C = \epsilon_0 \epsilon_{stack}/t_{stack}$, i.e.,

$$\Delta Q = \frac{\varepsilon_o \varepsilon_{stack}}{t_{stack}} \left(\Delta V_g^+ - \Delta V_g^- \right) \tag{10}$$

The total number of charges per unit area, i.e., charge density $(N_{trap} = \Delta Q/q, units: traps/cm^2)$ stored in trap sites of MAOS devices is computed as follows [35]:

$$N_{trap} = \frac{\varepsilon_o \varepsilon_{stack}}{q t_{stack}} \left(\Delta V_g^+ - \Delta V_g^- \right) \tag{11}$$

where \in_{stack} and t_{stack} is the relative permittivity of stack extracted from C-V characteristics in accumulation region and thickness of gate stack, respectively. The calculated value of ΔQ and N_{trap} is ~5.63 μ C/cm² and ~3.52 x 10^{13} traps/cm² for Al/Al₂O₃(13.68 nm)/SiO₂(6.15 nm)/Si, MAOS structure. This significantly high trap density points to the fact that the fabricated MAOS structure is feasible for high voltage multilevel data storage embedded memory applications. Further, the trapping efficiency (η) , defined as the ratio of trapped charges to total injected charges $(\Delta Q/Q_{total}*100 \%)$ for MAOS devices are calculated ~5.63 and ~ 5.02 % for MAOS structures with Al₂O₃ thickness \sim 13.68 nm and \sim 48.8 nm, respectively. It reveals that even though charges are trapped at bulk of Al₂O₃ but still the traps closer to the Al₂O₃/SiO₂ interface are dominant contributors. Moreover, the trap density $\sim 3.52 \text{ x } 10^{13} \text{ traps/cm}^2$ for Al/Al₂O₃(13.68 nm)/SiO₂(6.15 nm)/Si, system is higher than the trap density estimated from proposed method for Al₂O₃/SiO₂/Si structure of \sim 1.07 x 10¹⁰ traps/cm² and lies in the range of trap density $\sim 10^{12}$ - 10^{15} traps/cm² estimated from conventional method. Although, this significant variation in total charge density (N_t) estimated from KPFM



Fig. 12. Retention Characteristics of Al / $Al_2O_3(13.68 \text{ nm})$ / SiO₂(6.15 nm) / Si, MAOS Capacitors.

measurement and trap density (N_{trap}) estimated from constant current stress (CCS) method is possibly due to the presence of supplementary traps sites at the metal-insulator (Al₂O₃) interface (σ_{mi}) and can be expressed by the following relation [33]:

$$N_{trap} \approx \sigma_t - \sigma_{mi} \tag{12}$$

Finally, it is considered necessary to know the retention of memory devices before deployment to real world memory applications [36], [37]. Fig. 12 presents the retention characteristics (C-T analysis) of Al/Al₂O₃(13.68 nm)/ SiO₂(6.15 nm)/Si, MAOS structure. As depicted in inset of Fig. 12, the experimental data in log time scale which is required for aging analysis extrapolation of extracted data to 10 years. Here, the charge decay of MAOS devices is analysed with time after writing logic '1' and '0', respectively. A write pulse of ± 15 V in height and 100 ms in duration is applied and followed by a read voltage near flatband voltage of -1 V. As shown in inset of Fig. 12 the write pulse of -15 V corresponds to C_L and +15 V correspond to C_H, where, C_M is the mid capacitance between C_H and C_L. There is an exponential rise and decay with time noticed for C_L and $C_{\rm H}$, respectively. It is observed that $C_{\rm H}$ coincides with $C_{\rm M}$ at $\sim 10^5$ sec, hence the MAOS devices showed retention of $\sim 10^5$ sec. The moderate retention of MAOS devices may be due to absence of blocking layer and inability of traps sites in Al₂O₃ to hold the charges for longer durations. Thus, the MAOS devices are suitable for moderate retention electrically erasable read only type embedded memories applications.

IV. CONCLUSION

In Summary, ALD and PECVD based Al_2O_3 and SiO_2 thin films are used to fabricate Metal/Al_2O_3/SiO_2/Si, MAOS structure for charge trapping analysis of Al_2O_3 . The fabricated MAOS devices shows high memory window and lower leakage current density. The charge traps are found to be proportional to the alumina thickness and vertical charge leakage plays a dominant role in Al_2O_3 as compared to lateral charge spreading as revealed from KPFM analysis. Further, a simple method is proposed for trap density estimation at room temperature, which includes the effect of lift height and more sensitive to CPD value as compared to the conventional trap density estimation method. The trap density $\sim 1.07 - 2.01$ x 10^{10} traps/cm² is estimated using the proposed method for Al₂O₃ (13.68 nm)/SiO₂/Si structure. Moreover, trap density estimated for Al/Al₂O₃(13.68 nm)/SiO₂/Si structure from CCS method is $\sim 3.52 \times 10^{13}$ traps/cm². The significant variation in total charge density estimated from KPFM measurement and trap density estimated from constant current stress method is possibly due to the presence of supplementary traps sites at the metal-insulator (Al_2O_3) interface. Next, the trapping efficiency (n) is found to decrease from \sim 5.63 to \sim 5.02 % for MAOS structures with Al₂O₃ thickness \sim 13.68 nm and \sim 48.8 nm, respectively, attributes that traps closer to the Al₂O₃/SiO₂ interface are dominant contributors. The charge trap centroid is observed to shift close to the Al₂O₃/SiO₂ interface with decrease in thickness of alumina. Thus, because of high memory window at high voltage the Al/Al₂O₃/SiO₂/Si, MAOS system is suitable for high voltage electrically erasable read only type embedded memories applications. In future, the gate stack thickness should be reduced to few nano-meter and alternate high- κ materials must be investigated for bi-layer gate stacks that can hold the trapped charges for longer duration and also have higher retention.

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