Materials Science in Semiconductor Processing 12 (2009) 99–105

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Alteration of gate oxides thickness for SOC level integration

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ARTICLE INFO

Available online 16 September 2009

Keywords:
Alteration oxide thickness
C–V
J–E
D_{it} and FTIR

ABSTRACT

The integration of entire system on a chip (SOC) is the major challenge for the semiconductor industries. The successful implementation of SOC will require innovation in both circuit design and fabrication technology. However, from a process technology point of view, it can be seen that in order to provide design flexibility each of the sub-system may require different gate oxide thicknesses. In this work, $^{19}F^{+}$ implantation of variable doses on silicon is explored to achieve this goal. It has been observed that the differential oxide thickness can be achieved by varying the implanted dose of the fluorine on silicon, due to alteration in the oxidation rate. *C–V* and *J–E* characteristics are used to demonstrate the electrical behavior of fluorine implantation-based MOS devices. The stoichiometric composition analysis of dielectric materials is reported by FTIR measurements. The control over the oxide thickness, interface states, threshold voltage and stoichiometric composition of dielectric materials could play a vital role in the SOC level integration.

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1. Introduction

The evolution of microelectronics and its application in the computer technology have made a tremendous impact in all walks of human life. Moore's [1] law has driven much of the semiconductor revolution for the past 20 years. However, in today's integrated wireless communications environment, system-on-chip (SOC) solutions are becoming increasingly important for cost reduction as well as operational flexibility. System-on-chip solutions refer to the integrating different sub-systems onto the same chip. Combining logic circuits and several different memory elements on one chip with multiple supply voltages requires the use of multiple gate oxides thickness on the same wafer [2,3]. The successful implementation of SOC will require innovation in both circuit design and fabrication technology. However, from a process technology point of view, it can be seen that in order to provide process design flexibility each of the modules can require different gate oxide thicknesses [4]. SOC has capability to face this challenging task to integrate digital and analog circuits on the same chip. A trend of combining logic circuits and different memory elements on one chip or accommodating multiple supply voltages has increased the need for growing multiple gate oxide thicknesses on the same wafer. To meet these requirements of SOC technology demands new inter-level dielectrics of high quality and reliability, low stress, simplicity of process and ease to integration. Different techniques have been proposed to grow multiple gate oxide thicknesses in literature over the last few years [5–8]. One such technique is to grow the gate oxide throughout and etch back the gate oxide where thin oxides are required masking the thicker oxides regions [5]. The advantage of this technique is that it can be easily implemented with the existing processing technology. Imai et al. [4] has reported triple gate technologies where a thin gate oxide is grown for the core logic and pass transistors, a thicker oxide for the lower power CMOS areas and an even more thicker gate oxide for the *I*/*O* modules. Togo et al. [9] demonstrated a system-on-chip fabrication for dual gate CMOS field-effect transistors (FETs) with multiple-thickness gate oxides by using Ar^{+} and N^{+} implantation. King et al. [10] have demonstrated the method of using masked

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doi:10.1016/j.mssp.2009.08.003

oxygen implantation. The use of both Ar^+ and N^+ implantation produces a 20% difference in gate oxide thickness between the low-speed memory device region and the high-performance logic region for the integration of digital, analog, power management, *I/O*, FLASH, RAM, etc. on the same die in the same chip [3]. Hinriches and Preikszat [11] and Badawi and Anand [12] attempted oxygen implantation and demonstrated that severe damages occur in the substrate, casting oxygen implantation as an unsuitable technique for forming gate oxides. However, more recent studies have indicated that oxygen implantation could be used for sub-5 nm oxide technologies [13]. A class of materials that have received much attention recently is the halogens implantation-based dielectric materials. Enhancement in the oxidation rate due to different halogens (chlorine, iodine) and xenon species was compared for different oxidation and implants conditions [14,15]. Chlorine implantation in silicon has been found to enhance the oxidation rate and decrease in generation of stacking faults during thermal oxidation [16]. Fluorine-implanted silicon after annealing is expected to leave less residual damages due to its smaller size as compared to the other halogens. An obvious advantage of fluorine implantation-based dielectric films is their similarity with standard oxide films, less leakage current and hence their ability to be readily integrated into the process [17–19]. Not much attempt has been reported in the literature on fluorine implantation with a view of altering the oxide thickness for SOC level integration. In the present work, the low energy fluorine ions have been implanted at varying doses to alter the oxidation rate of silicon and thereby the differential thickness of grown ultra-thin oxides could be achieved.

2. Experimental

RCA cleaned p-type silicon wafers of ⟨1 0 0⟩ orientation and 10–30 Ω cm resistivity were used for these experiments. Fig. 1 shows the temperature–time cycle of furnace used for the oxidation to achieve a good thickness control and uniformity of grown oxide. One standard liter per minute (SLM) of oxygen was added to 19 SLM of nitrogen during ramping up to avoid the nitride micro-cluster formation. Wafers were loaded at 800 °C and furnace temperature was raised to 900 °C at a ramp rate of 10 °C/min up to 890 °C and at 3 °C/min to the final temperature.

The thickness of oxide grown during this cycle was found to be 8.1 nm. After oxidation, wafers are spun coated with positive photoresist and masked to expose 3/4th part of wafer towards major flat. After developing wafers were given oxide etch dip in 1:50 ($HF+H_2O$) to remove oxide from 3/4th part of wafers. The wafers were masked again to keep 1/2 portion of the wafers (opposite to major flat) covered with photoresist. This leaves the pre-grown oxide portion and some un-implanted portion covered with photoresist. The wafers were split into four sets, pre-grown, un-implanted, fluorine implanted with lower doses and higher doses. Wafers were split in three sets and implanted by the industry standard high current ion implanter EATON, NV10-80, (implant[1]) [1×10^{14},

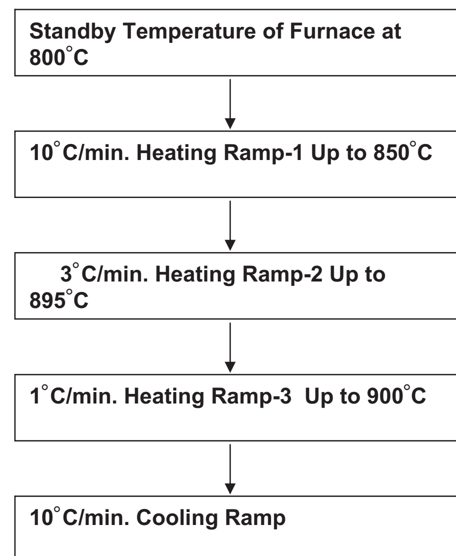

Fig. 1. Details of furnace oxidation cycles.

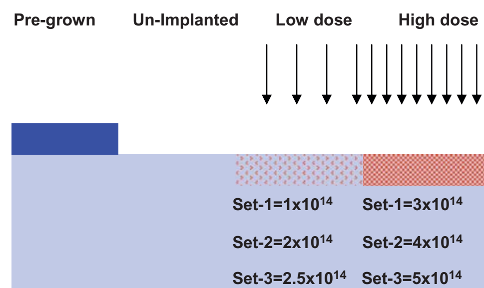

Fig. 2. Cross-sectional view of the wafers implanted with different fluorine doses.

2×10^{14} and 2.5×10^{14} ions/cm^2] as shown in Fig. 2. Then all the wafers were again masked to keep 3/4th part of the wafer (opposite to major flat) covered with photoresist. Second implant (implant[2]) is then carried out again on these three sets at 2×10^{14}, 2×10^{14} and 2.5×10^{14} ions/cm^2, respectively. In this way, the 1/4th portion of these sets of wafers received total dose (implant[1]+implant[2]) of 3×10^{14}, 4×10^{14} and 5×10^{14} ions/cm^2.

Then oxidation is carried out in the furnace at 900 °C for 5 min in presence of dry oxygen diluted with nitrogen and obtained thicknesses of 2.0, 2.1, 2.2, 2.3, 2.5, 2.7, 3.0 and 8.1 nm as measured using Rudolf Research's Ellipsometer (Auto EL-III). After the removal of the backside oxide, a thick layer of aluminum film was deposited for back contact. In the front side, gate electrodes of 100 μm × 100 μm area were patterned using photolithography and wet etching technique. Aluminum metal films for front and back contacts were deposited using DC sputtering. The MOS capacitors thus obtained were electrically characterized at room temperature by capacitance–voltage (*C–V*) at 1 MHz frequency and current–voltage (*I–V*) measurements using a Keithley 590 *C–V* Analyzer, 230 Voltage Source and Keithley 2602 source

meter. The stoichiometric analyses of ultra-thin dielectric films were carried out by ABB BOMAN FTIR system.

3. Results and discussions

C–V characteristics of MOS devices measured for pre-grown and for oxide films grown on p-type silicon before and after $^{19}F^{+}$ implantation at a dose of 1×10^{14}, 2×10^{14} and 2.5×10^{14} ions/cm^2 low dose (implant^1) and 2×10^{14}, 2×10^{14} and 2.5×10^{14} ions/cm^2 high dose (implant^2), respectively is shown in Fig. 3. Therefore, in this fashion the 1/4th portion of these sets of wafers anticipated total dose (implant^1+implant^2) of 3×10^{14}, 4×10^{14} and 5×10^{14} ions/cm^2 as shown in Fig. 2.

The gate voltage was swept from inversion to accumulation [+5 V to −5 V] during the C–V measurements. For pre-grown, un-implanted, low-dose fluorine-implanted and high-dose fluorine-implanted oxide, C–V characteristics of MOS devices show that the maximum and minimum values of computed capacitances are given in Table 1. The different values of capacitances for these devices may be endorsed to variation in oxide thickness or due to a possible alteration in the dielectric constant of grown oxide due to the incorporation of fluorine. However, the second possibility was ruled out by measuring the oxide thickness using Ellipsometry, because the effect of change in film characteristics on C–V and Ellipsometer measurements are shown in Table 2 [15].

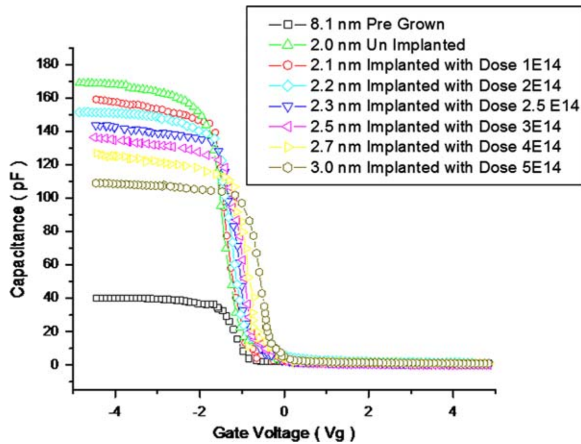

Fig. 3. C–V characteristics of MOS devices measured at 1 MHz for pre-grown and oxide films grown on p-type silicon before and after fluorine implantation at the different doses.

Table 1 compares the oxide thickness measured from the Ellipsometry and obtained using the C–V measurements. The results clearly indicate that within the experimental error, the measured thicknesses were same. So, we conclude that the change in capacitance was due to the change in oxide thickness rather than due the change in the dielectric constant as shown in Fig. 4.

The relationship for the Ellipsometry data are

$$T_{ox}\times\eta_f=\alpha(\Delta_{si}-\Delta) \quad (1)$$

where α, Δ_{Si} and η_f are constants that depend on the wavelength used, Δ is the measured Ellipsometric data and η_f refractive index of the film.

The refractive index η_f of a film is determined by

$$\eta_f=\left(\frac{\varepsilon}{\varepsilon_0}\right)^{1/2} \quad (2)$$

Table 2.
Effect of change in film characteristics on C–V and Ellipsometer measurements.

	C-V	Ellipsometer
$T_{ox}\uparrow$	T_{ox} Measured $\uparrow$	T_{ox} Measured $\uparrow$
$\varepsilon\downarrow$	T_{ox} Measured $\uparrow$	T_{ox} Measured $\downarrow$

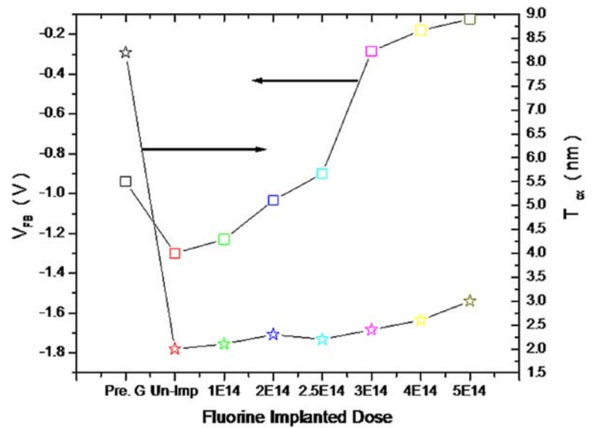

Fig. 4. V_{FB} and T_{ox} variation with fluorine ions doses of MOS devices.

Table 1.
Measured parameters of MOS devices with ultra-thin SiO_2.

Parameters	Wafers oxidized at 900 °C for 5 min							
	Samples							
	Pre-grown	Un-implanted	Dose 1×10^{14}	Dose 2×10^{14}	Dose 2.5×10^{14}	Dose 3×10^{14}	Dose 4×10^{14}	Dose 5×10^{14}
Oxide thickness measured by C–V (nm)	8.3	2.1	2.2	2.3	2.5	2.7	2.9	3.2
Oxide thickness measured by Ellipsometer (nm)	8.1	2.0	2.1	2.2	2.3	2.5	2.7	3.0
Oxide capacitance C_{max} (pF)	46	165	158	151	145	138	127	112
Oxide capacitance C_{min} (pF)	1.5	0.7	1.1	1.5	0.5	1.0	1.1	0.8

where ε and ε_0 are the dielectric constant film and free space, respectively.

These results clearly indicate that the oxidation rate has increased after fluorine implantation. *C–V* characteristics of MOS based on pre-grown oxide indicates a flat band voltage (V_{FB}) shift of 1.7 V along the negative voltage axis indicating the presence of high density of fixed positive charges (+Q) in the pre-grown silicon oxide film. Un-implanted region shows the flat band voltage shift of 1.3 V along the negative axis. The pre-grown SiO_2 layer was etched using HF-based etchant. This treatment forms Si–F (silicon–fluorine) network as previously observed by Kasi et al. [20] and results in a significant shift of the flat band (V_{FB}) voltage due to the reduction of fixed oxide charges within the thin dielectric films. After low dose at energy (10 keV) fluorine ions implantation at 1×10^{14}, 2×10^{14} and 2.5×10^{14} ions/cm^2 doses, the flat band voltage has been shifted from 0.89 to 0.24 V, respectively, along the negative voltage axis. After fluorine ions implantation at 3×10^{14}, 4×10^{14} and 5×10^{14} ions/cm^2 high doses at energy (10 keV), the flat band voltage has been shifted from 0.13 to 0.10 V, respectively, along the direction of positive voltage axis.

However, the shift in V_{FB} computed for the pre-grown oxide is -1.7 V with respect to the un-implanted and maximum fluorine dose-implanted silicon. In case of pre-grown oxide the absolute value flat band is -0.90 V, while the V_{FB} computed for un-implanted and the maximum fluorine-implanted dose (5E14) are -1.38 and -0.1 V, respectively. Therefore, the shift in V_{FB} between pre-grown and un-implanted device is 0.48 V (0.9–1.38 V). Similarly, the shift in un-implanted to the maximum fluorine-implanted dose (5E14) is 1.28 V (1.38–0.1 V). Hence, the net shift in V_{FB} from pre-grown oxide to the maximum fluorine implanted is 1.76 V (1.28+0.48 V). Hence, the flat band voltage shift of 1.7 V from pre-grown oxides to the fluorine implanted of 0.10 V gate oxides indicate the flexibility of altering the flat band voltage (V_{FB}) with low energy fluorine ion implantation as shown in Fig. 4. The similar results have also been reported by Perera Rohana et al. [21] and were attributed due to the reduction of the positive charges in the thin oxides.

As indicated in Fig. 5, there was a significant change in the threshold voltage (V_{TH}) of pre-grown, un-implanted and fluorine implanted at low-dose and high-dose samples. There could be fixed positive charges within the pre-grown oxide and the incorporation of fluorine was expected to compensate the fixed positive charges and hence results in the change of threshold voltage. Even in the case of un-implanted samples, there could be significant fluorine incorporation due to HF treatment [22–24]. Similarly, Fig. 5 shows the effective oxide charge (Q_{EFF}) variation with the fluorine incorporation. There is a decrease in the effective oxide charge due to fluorine incorporation in the oxide. The shift in the flat band voltage in the positive direction with fluorine ion implantation and reduction in the oxide charges implies that fluorine implantation contributes negative charges. Maegawa and co-workers [25–27] have reported the similar behavior of fluorine ion implantation in gate oxides.

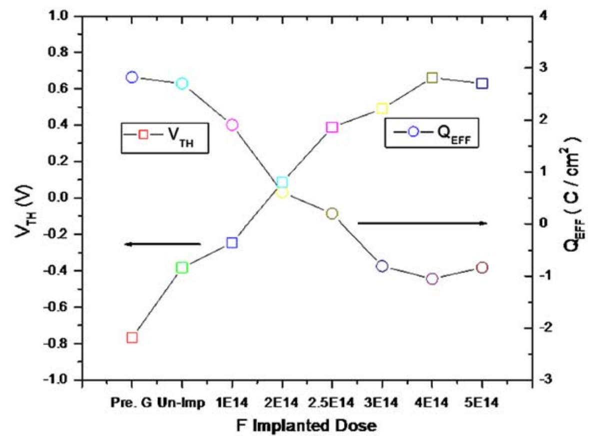

Fig. 5. V_{TH} and Q_{EFF} variation with fluorine ions doses for MOS devices.

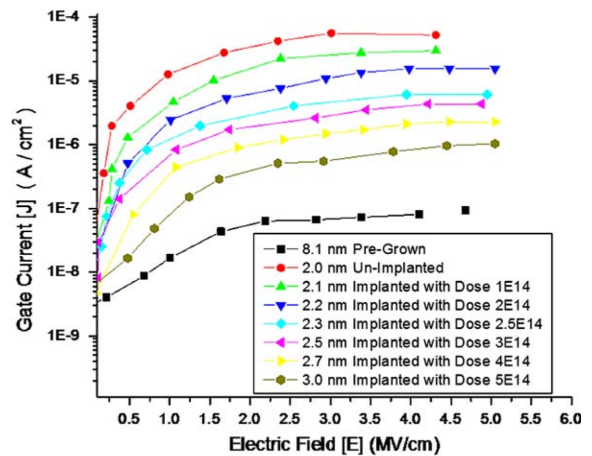

Fig. 6. J versus E of MOS device with ultra-thin SiO_2.

The V_{FB} and V_{TH} shifts are computed from the *C–V* measurements. As shown in Fig. 3, the pre-grown oxide indicates *C–V* shift towards the negative voltage axis as compared to un-implanted and fluorine implantion-based MOS devices. However, the pre-grown oxide have the oxide thickness of ~8.1 nm, in which the effect of net positive oxide charges may be neutralized by the bulk charges, while in case of un-implanted and fluorine-implanted samples the thickness of grown oxide varies from 2 to 3 nm. Hence, the effect of positive oxide charges is sufficient to result the significant shift in V_{FB} and V_{TH}. However, the high density of positive oxide charges could be compensated by the incorporation of fluorine, which introduces the negative charges within oxide either by oxide removal with HF or by fluorine ion implantation. It results a significant shift in V_{FB} and V_{TH} of devices. Therefore, as the fluorine implantation alters the oxidation rate of silicon, it could be one of the possible applications in controlling the flat band voltage/threshold voltage in addition to the channel doping.

Fig. 6 shows the gate leakage current density of MOS capacitors, as a function of gate electric field (E). As evident from Fig. 6, there is a significant reduction in the

gate leakage current with the electric field for increased dose of fluorine ions. It was attributed to the reduction of the gate oxides defects [24,25]. Fig. 7 shows the distribution of interface state density (D_{it}) in the Si band gap before and after fluorine incorporation within the oxide.

The interface trap density versus energy curve examines the trap densities near the mid-gap (E_t). The interface trap energy from mid-gap (E_t), was measured as the difference of silicon surface potential (ψ_s) and bulk potential (Φ_B) [26,27].

This measurement also implies the improvement in oxide quality due to the reduction of interface state density. The above results of significant variation in the oxide thickness and trapping properties of Si/SiO_2 interface clearly follow the two-step model to explain the bonding behavior of fluorine in oxide as shown in Fig. 8. First, fluorine diffuses and bonds to dangling bonds and weakened bonds in the silicon dioxide. After these interface regions have been saturated with fluorine, additional incorporation occurs primarily in the bulk. The fluorine will then break the Si–O bonds and displace

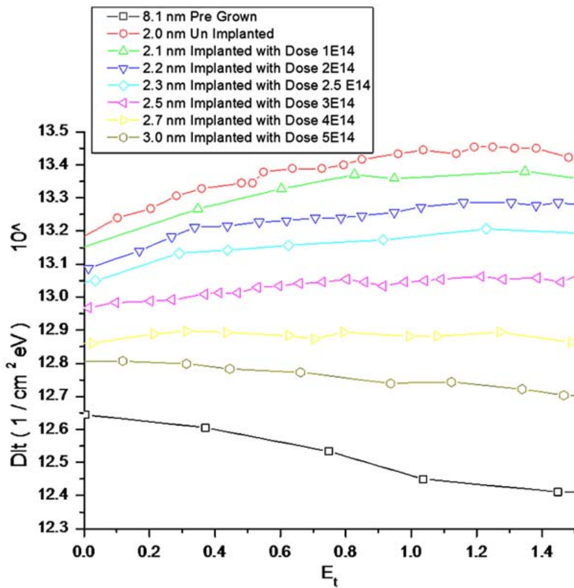

Fig. 7. Interface state density (D_{it}) versus interface trap energy density (E_t) of MOS device with ultra-thin SiO_2.

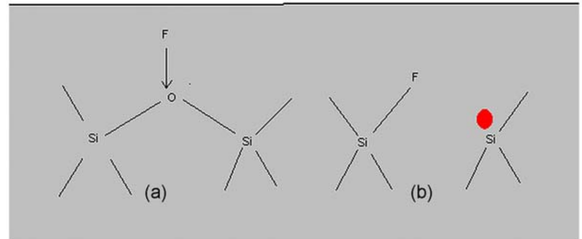

Fig. 9. Trapping mechanism for (a) fluorine displaces an oxygen in Si–O–Si bond. (b) The dangling bond on silicon atom act as a trap.

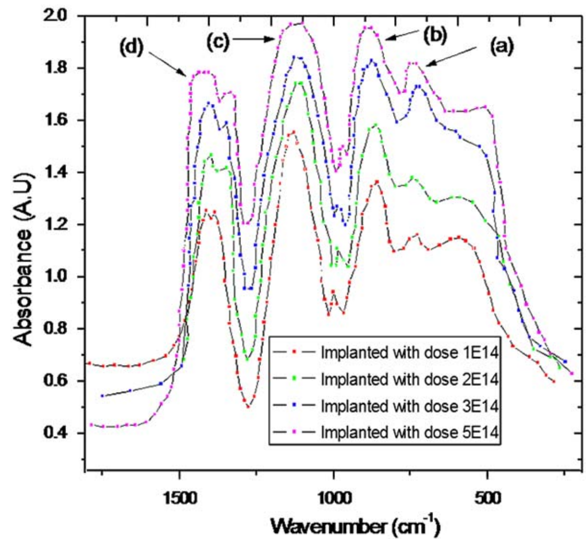

Fig. 10. FTIR spectra of un-implanted and F^+ implanted SiO_2 at 1×10^{14}, 2×10^{14}, 3×10^{14} and 5×10^{14} ions/cm^2, respectively.

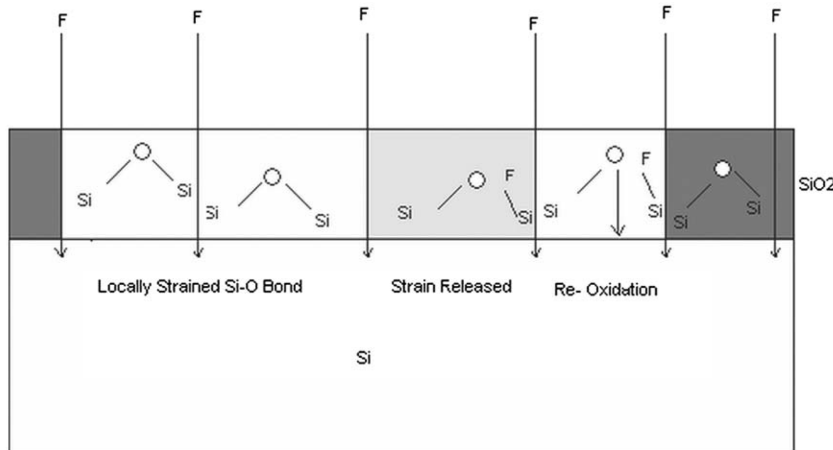

Fig. 8. Mechanism for additional oxide growth due to fluorine incorporation at Si/SiO_2 interfaces.

Table 3.
FTIR data for different thicknesses of un-implanted and F^+ implanted SiO_2 films.

Implanted dose	Oxide thickness (nm)	(a) Si–O bending at 750 cm^{-1}		(b) Si–O–Si bending at 808 cm^{-1}		(c) Si–O–Si stretching at 1078 cm^{-1}		(d) Si–O asymmetric stretching	
		Peak value	FWHM	Peak value	FWHM	Peak value	FWHM	Peak value	FWHM
Un-impl.	2.0	750	9.8	808	78.2	1078	87.9	1279	101.70
1×10^{14}	2.1	752	11.8	810	80.07	1080	90.46	1281	102.03
2×10^{14}	2.2	753	12.31	811	84.96	1081	91.02	1283	104.46
2.5×10^{14}	2.3	755	14.31	814	85.02	1083	93.00	1285	106.67
3×10^{14}	2.5	756	20.20	815	95.91	1085	103.91	1286	108.45
4×10^{14}	2.7	758	21.92	817	98.71	1087	105.40	1289	110.05
5×10^{14}	3.0	760	25.80	819	100.13	1090	109.44	1291	111.01

oxygen at these sites. Last, the free oxygen diffuses to the interfaces and oxidizes additional silicon. These phenomena result in the increase in oxide thickness.

When fluorine displaces an oxygen atom in the oxide, the dangling bond on a silicon atom can act as a hole trap, which results the variation in threshold voltage as shown in Fig. 9 [15,28].

Fig. 10 shows the Fourier transform infrared (FTIR) spectra of fluorine implanted thermally grown ultra-thin SiO_2 films. In the literature, FTIR spectrum of ultra-thin SiO_2 showed the four principal vibration band spectra. The lowest frequency band at around 750 cm^{-1} corresponds to Si–O bending, second one was 808 cm^{-1} corresponds to derived from the Si–O–Si bending vibration, the third one at around 1078 cm^{-1} corresponding to the Si–O–Si stretching and the fourth was at the 1279 cm^{-1} described to Si–O asymmetric stretching vibrations [29–33].

Fig. 10(a)–(d) represents the Si–O bending, Si–O–Si bending mode, Si–O–Si stretching mode and asymmetric stretching, respectively. The shifts in the full-width half-maximum (FWHM) and peak positions of fluorine implanted at various doses and un-implanted, not all were shown in Fig. 10 of dielectric films were listed in Table 3. The magnitude of FWHM increased with increasing film thickness, which reflected to the increased number of vibration modes in the thicker film as shown in Fig. 10 [32].

These results also attributed to stress relief during film growth and relaxation of bond strain due to shift in the asymmetric stretching mode to higher wave-numbers. Hence, the increase in FWHM indicates the variation in the Si–O bonds disorderness of SiO_2 film with the $^{19}F^+$ implantation [32,33]. The absorption band near 1230 cm^{-1} that indicates the crystal structure. In literature a peak at 1250 cm^{-1} was reported but no further interpretation of this vibration was given [32]. One possible hypothesis could be that the peak centered at 1254 cm^{-1} was due to an interface Si–O was largely constrained by the Si substrate. Therefore, one could expect a transition region in which the Si–O was not stoichiometric and where the Si–O tetrahedral was not completely distributed at a random manner. As a consequence, some atomic layers of ‘quasi-crystalline’ silicon oxide could be present at the Si–Si–O interface. This suggests that the number of Si–O units contributing to the peak at 1279 cm^{-1} increase with increasing oxide layer thickness, which was observed and shown in Fig. 10.

4. Conclusion

This paper depicts a new technique to alter the oxidation rate of silicon and results in the differential oxide thicknesses using low energy fluorine ion implantation for SOC level integration. The significant variation in V_{TH}, V_{FB} and Q_{EFF} have been found with the fluorine implantation dose, which could have possible applications in controlling these parameters in addition to the conventional channel doping. There is also a marked improvement in the quality of gate oxide as shown by the results of gate leakage current, the interface trap density and FTIR.

Acknowledgment

The authors would like to acknowledge the University Grant Commission (U.G.C.)-New Delhi for financial assistance, without whom this work would not have been possible.

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