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Nitrogen doped multilayer photo catalytically reduced graphene oxide floating gate: Al/PMMA/NrGO/SiO_2/p–Si/Au based hybrid gate stack for non volatile memory applications

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ABSTRACT

Photo catalytically assisted, multi–layer nitrogen doped reduced graphene oxide (ML–NrGO) is investigated as a promising charge storage layer in Al/PMMA/NrGO/SiO_2/p–Si/Au structure. A considerable memory window (ΔW) of ~3.3 V at ± 7 V sweep voltage and long data retention upto ~ 10^5 s is demonstrated as an encouraging candidature for emerging memory hierarchies. The clockwise hysteresis supports the hole charge trapping mechanism in the NrGO based structure. The ML–NrGO memory devices provide the rapid programming, saturation of the program transients, store more data at less cost and reduced ballistic transport in the plane perpendicular to NrGO. The facile, solution processable, cost effective device processing and stable retention of the fabricated ML–NrGO based Al/PMMA/NrGO/SiO_2/p–Si/Au flash memory structures proves to be a potential alternative for existing EEPROM based embedded applications and also for commercial scale production of flash memory based on flexible organic electronics.

1. Introduction

With the advancement of semiconductor technology and scaling of device features size, excessive efforts have been devoted to develop an electrically re–programmable, high performance, low–cost floating gate based non–volatile flash–memory (FG–NVFM) devices, for popular consumer electronics [1]. The operation of FG–NVFM is particularly interesting and mainly relies on capacitance modulation at the trapping sites available in the FG [2]. With the continuous downscaling of FG for high–density data storage at low operating voltages, the FG–NVFM structures have encountered several challenges like enhanced capacitive/parasitic coupling within neighboring FG, variation in threshold voltages finally leading to critical concerns of device performance and reliability [1,3]. The scaling of FG–NVFM has already reached its threshold; hence, new materials/approaches are required to meet the current and futuristic demand of reliability and performance of FG–NVFM for electronics devices. Driven by this demand, thin metal layer (~1 nm) and nanoparticles were considered as an alternative in the past, owing to their quantum confined characteristics [2,4]. But, due to inherent band gap restriction, reliability and variability like agglomeration/diffusion of metal into dielectrics; the metal layer and nanoparticle based FG–NVFM shows relatively narrow memory window (ΔW) and short retention characteristics [2–4].

Recently, graphene (monolayer thickness of ~0.3 nm) with excellent electronic properties has emerged as a potential FG material to exceed the performance of FG–NVFM [5]. The considerations for use of graphene are (i) high density of states (DOS) (8×10^{12} cm^{-2} eV^{-1} for monolayer and 4.4×10^{13} cm^{-2} eV^{-1} for multi–layer, (ML)); (ii) high work function (~4.2 eV for monolayer and 4.6 eV for ML (3–4)), and (iii) low dimensionality [3,5]. The high DOS, work function and a reduced ballistic component of conductivity along the perpendicular plane, supports the large ΔW in ML graphene based FM [3,5]. To date, CVD graphene based FM has been demonstrated [1,5], however, besides expensive, the CVD graphene based FM may lead to failure of the device due to pin–-holes [1]. Therefore, the solution processed, low–cost, derivatives of graphene, graphene oxide (GO), reduced graphene oxide (rGO) with monolayer thickness ≤ 1 nm, has attracted substantial interest from the scientific community and used as an effective FG material, channel in FETs, super capacitor electrode and sensors [6–18].

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Structurally, GO consists of a hexagonal carbon ring network with sp^2 hybridized carbon atoms and sp^3 hybridized carbon and hydrophilic functional groups [9,13]. GO with functional groups shows insulating characteristics, while on reduction, results into rGO which is conducting in nature. Several strategies for the GO reduction and formation of rGO is discussed in past [11]. The presence of functional groups, defects, high DOS and work function in GO and rGO provides quantized levels and contributes to the charge storage applications, as reported in Refs. [3,4,7]. Additionally, other advantages of using GO–rGO sheets as FG includes, (i) the band gap modulation based on the degree of oxidation and reduction, hence tuning the physiochemical and electronic properties, (ii) solubility of GO in a wide range of solvents, allowing controlled deposition, followed by reduction to rGO. Even though, GO sheet decorated with functional groups is thermally unstable at temperatures (>300 °C) owing to loss of attached functional groups between adjoining GO sheets [7,19]. Hence, GO based devices pose a serious concern for Si technology, therefore, rGO is being thought as a probable alternative.

Beside this, efforts have been made in order to enhance the electrical conductivity of rGO. Hence, doping seems to be an alternative way for tailoring the electronic, physiochemical properties [20–22]. Thus, nitrogen (N) doping in rGO is considered to be an excellent choice owing to the comparable atomic size, transfer of charge carriers forms strong bonds with carbon atoms [21,23–25]. The detailed mechanism for the doping of nitrogen in GO, rGO is reported in past [26–29]. Generally, the doping introduces chemically active sites, owing to the interaction between the positive charge in the nitrogen and negative charge in functional groups present in GO, which leads to polarization under electric filed, hence, the active sites and ease of polarizability in NrGO can be advantageous for memory storage applications [29–31]. However, existing N doping techniques, generally involve toxic reagents, ambient conditions, dedicated setup, are expensive and require high temperatures processing [21,22,24,32]. Therefore, the need of the hour is to explore a rapid, inexpensive, environment–friendly and scalable approach for the production of N doped GO/rGO for its use as FG in NVFM.

To address these challenges, the present work demonstrates a facile, cost effective, solution processable, photo–catalytic approach for the synthesis of engineered, multilayer nitrogen doped reduced graphene oxide (ML–NrGO) formulation, useful as FG material in Al/PMMA/NrGO/SiO_2/p–Si/Au, NVFM. In this work, we systematically investigated the charge storage capability and retention for the NrGO based Al/PMMA/NrGO/SiO_2/p–Si/Au FG–NVFM structures. The multilevel memory characteristics are measured using capacitance–voltage (C–V) characteristics with low sweep voltages of ±7 V. Subsequently, the leakage characteristics are evaluated by the current density–voltage (J–V) characteristics, while, the retention characteristics of the fabricated FG–NVFM structure is estimated based on the capacitance–time (C–T) measurements at room temperature.

2. Material and methods

2.1. Materials

All chemicals were of analytical grade and used without any further purification. Graphite powder (99.999% pure, size < 100 μm), Ethanol, Hydrogen Peroxide (H_2O_2), Sodium Nitrate ($NaNO_3$), Ammonia solution (NH_3 ~ 25%), Potassium permanganate ($KMnO_4$), Hydrochloric acid (HCl) were purchased from Merck. Sulphuric acid (H_2SO_4) and NMP from Fisher Scientific and Alfa Aesar. De–ionized (DI) water (Elga make, UK) resistivity of 18.2 MΩ cm was used in the present study for cleaning, solution preparation and dilution. UV lamp source (130 w, 253 nm, G64HO75, Arklite make) with an intensity of ~10 mW/cm^2 at distance of ~6 cm (measured by UVC Light Meter 850010, SPER Scientific make), was used as a source for the NGO reduction. During the exposure, the temperature of the UV chamber was maintained below 40 °C to avoid thermal reduction of GO.

2.2. Synthesis of GO and NGO

The synthesis of GO was carried out based on modified Hummers method, as reported in past [13,33]. To a brief note, the graphite powder is subjected to oxidation under constant stirring and the reaction is carried out in an ice bath (<5 °C) to result into graphite oxide. To obtain GO powder, the graphite oxide solution was consecutively centrifuged, washed with DI water until pH ~7 and finally dried in a vacuum oven. The aqueous GO solution (~1 mg/ml) in DI water was prepared using mild sonication for 120 min. For N doping in GO, NH_3 solution (~150 ml) was added to the GO solution, kept on a hot plate at 50 °C under constant stirring for 72 h, finally drying the solution in vacuum oven result in brownish NGO powder. During doping of nitrogen, the NH_3 molecules are expected to react more with the hydroxyl (–OH) and epoxy functional groups in GO rather than on the carbon surface, owing to the requirement of low formation energies for reaction between functional groups (~2.51 eV) and nitrogen rather than with carbon (~5.61 eV) [27], hence leading to the formation of pyridine–N as compared with pyrrolic and graphitic N [26,27]. The reaction of N with the functional groups results into water molecule and NH_2, further adsorbed on the carbon surface [26,29]. Additionally, it is reported that the interaction between pyridine N and charged carboxylic functional group in NrGO induce polarizations under an electric field, hence results into ON and OFF state for memory devices [29].

2.3. Fabrication of Al/PMMA/N–rGO/SiO_2/p–Si/Au FG–NVFM

A 2 inch, p–type Si wafer (1–10 Ωcm) with ⟨100⟩ orientation was cleaned using standard RCA cleaning. For high quality, tunnel oxide growth, the cleaned Si wafers were subjected to Rapid Thermal Oxidation (RTO) using AS – One RTP System (ANNEALSYS, France Make) from room temperature to 900 °C under N_2 followed by O_2 at 800 sccm, for 90 s (as shown in Fig. 1). The ramp up and down conditions was maintained around 25 and 3 °C/sec, respectively. The thickness of the RTO grown SiO_2 was measured by J. A. Woolman Imaging Ellipsometer and found 5 ± 0.2 nm. Thereafter, Au (~100 nm) bottom contact was made using e–beam evaporator after etching the back side buffer oxide to result into SiO_2/p–Si/Au. The as synthesized NGO powder was dispersed in DI: Ethanol in a ratio (1:2) and spin–coated onto SiO_2/p–Si/Au wafer at 2000 rpm for 45 s at an acceleration of 100 rpm/sec and dried at 50 °C for 3 min. The NGO is dispersed in a mixture of DI: Ethanol, as GO forms stable, uniform dispersion with DI water and ethanol [34], which finally results in deposition of uniform NGO film over SiO_2/p–Si/Au substrates. After drying, NMP (~10 μl) was drop casted on NGO/SiO_2/p–Si/Au and heated at 70 °C for 4 min. For the photo catalytic reduction, the NGO/SiO_2/p–Si/Au samples were then subjected to UV irradiation for 45 min and sample to UV tube distance was ~6 cm and later on, PMMA (950 A1) was spun coated, at 1000 rpm for 60 s at an acceleration of 100 rpm/sec, and dried at 80 °C for 5 min. The thickness estimate for PMMA was performed using NanoMap–LS (AEP Technologies, USA) and was found to ~ 50 nm.

Finally, the PMMA/NrGO/SiO_2/p–Si/Au samples were subjected to top metal, Al deposition (thickness ~150 nm) under high vacuum at ~ 1.5×10^{-6} mbar and the Al is patterned with standard lithography. Fig. 1 (a) shows the schematic process flow for the

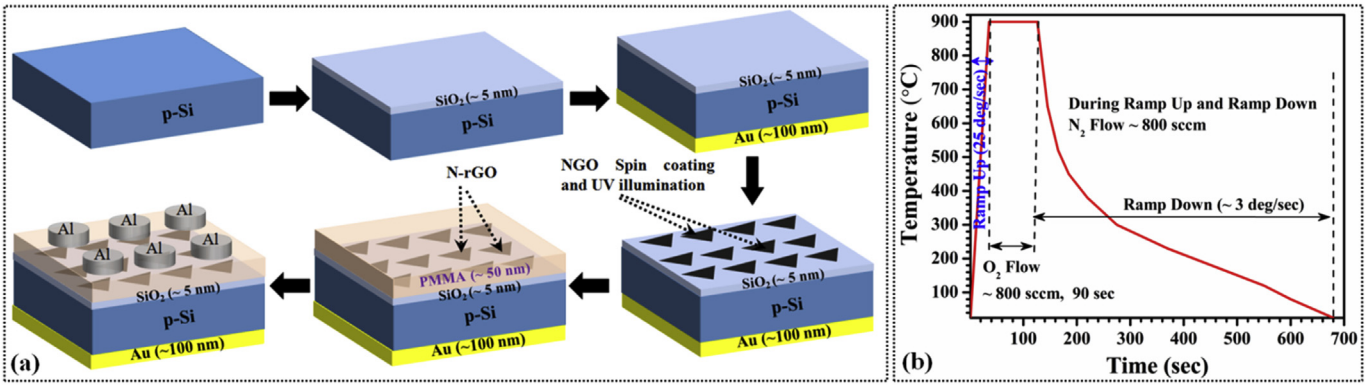

Fig. 1. (a) Schematic process flow for the fabrication of Al/PMMA/NrGO/SiO2/p–Si/Au memory structure, (b) Timeline for the RTO of SiO_2.

fabrication of Al/PMMA/NrGO/SiO_2/p–Si/Au, FG–NVFM device. The electrical characterizations, Capacitance – Voltage (C – V), Current density – Voltage (J – V) and Capacitance – Time (C – T) were carried out at room temperature using KEITHLY 4200 SCS system. The chemical and surface analysis was recorded using Horiba LabRAM based micro–Raman Spectroscopy and Dimension Icon from Bruker based AFM, respectively, at room temperature.

3. Results and discussion

Fig. 2 (a) shows the AFM tapping mode image (3 × 3 μm) for the NrGO sheets over SiO_2/p–Si wafer. AFM analysis confirms the presence of ~1.5–1.7 nm thick rGO sheets, which is consistent with its 4–6 layer of rGO sheets. Additionally, the doping of nitrogen in the rGO sheets can clearly be seen from the AFM image. For Raman spectroscopy, the synthesized GO and NrGO films were deposited over cleaned Si and dried. The characteristic D and G bands for GO and NrGO are shown in Fig. 2 (b). The first peak near 1337 cm^{-1} corresponds to the defect induced D band peak, while the second peak around 1583 cm^{-1} corresponds to the characteristics sp^2 hybridized carbon, G band peak. For GO, the estimated I_D/I_G GO is ~0.93, while for NrGO is ~1.2, signifying the formation of a large number of small graphitic domains and defects in NrGO compared to GO [11]. The high I_D/I_G ratio for NrGO also signifies the modulation of electronic and physical properties, thus provides a large number of trapping sites. As shown in FTIR spectrum (Fig. 2(c)), that carbon (C=C) peak for GO (sp^3 hybridized) and NrGO (sp^2 hybridized) around 1614 and 1654 cm^{-1}, respectively. The spectrum for GO shows the presence of hydrophilic functional groups, hydroxyl (–OH), carbonyl (C=O), epoxy (C–O–C) and carboxyl (O=C–OH) at 3357, 1727, 1372 and 1044, 976 cm^{-1}, respectively [11,13,35]. Conversely, for NrGO, the spectrum confirms the doping and presence of new carbon–nitrogen (C–N) and nitrogen–hydrogen (N–H) vibrational modes at 1402, 1028 and 3281 cm^{-1}, respectively [36].

The charge storage analysis for fabricated Al/PMMA(~50 nm)/NrGO/SiO_2(~5 nm)/p–Si/Au FG–NVFM device were performed using cyclic C–V measurements at a frequency of 1 MHz. The cyclic C – V curves were obtained by sweeping the gate voltage from inversion (V_{g+}) to accumulation (V_{g-}) and accumulation (V_{g-}) to inversion (V_{g+}) for forward and reverse sweep, respectively (Fig. 3 (a)). Here, the ΔW is defined as the flat band voltage (V_{fb}) shift from forward and reverse gate voltage sweep in cyclic C–V characteristics [37]. In the present investigations, we have performed cyclic C–V measurements with three different sweep voltages, first 3 V to – 5 V, second ±5 V and third ±7 V at 1 MHz frequency.

The ΔW corresponding to first, second and third sweep is demarcated as "A" (Black), "B" (Red) and "C" (Blue) (Fig. 3 (a)). As shown in the cyclic hysteresis of C–V curves (Fig. 3 (a)), that the Al/PMMA/SiO_2/p–Si/Au system follows a clockwise upward arrow curve in forward sweep and clockwise downward arrow curve in reverse sweep. It clearly indicates that there is a significant flat band voltage shift towards positive gate voltages during the reverse sweep and is in line with the previous reports [3,4,38,39]. The cyclic C – V hysteresis results the change in ΔW of around 1.85, 2 and 3.3 V as compared to control samples (Pt/SiO_2 (~5 nm)/p–Si/Au and Al/PMMA (~50 nm)/SiO_2 (~5 nm)/p–Si/Au) at different gate voltage sweeps from 3 to – 5 V, ± 5 V and ±7 V, respectively. It attributes the significant increase in charge trapping and de trapping in the NrGO sheets with an increase in electric field. Also, the clockwise nature of the cyclic hysteresis window indicates the hole trapping

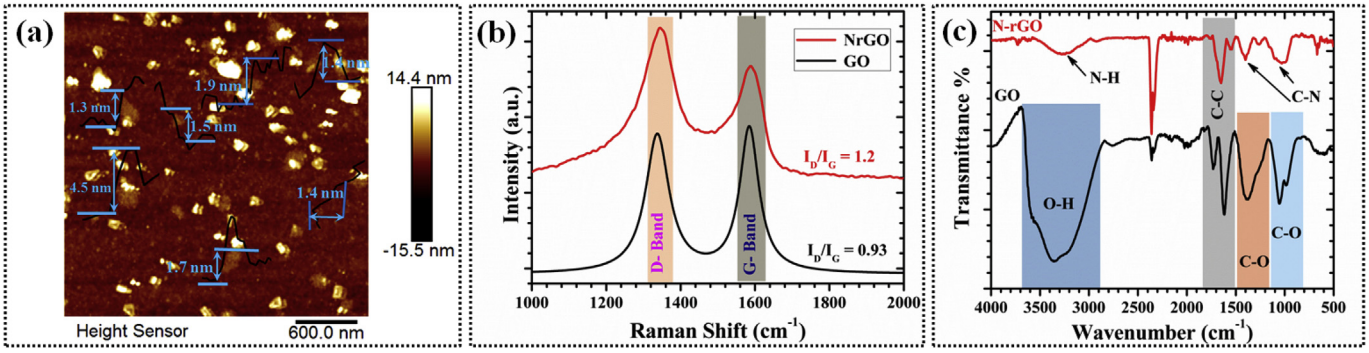

Fig. 2. (a) AFM image of NrGO sheets on SiO_2/p–Si wafer showing height analysis of different NrGO sheets (b) Raman Spectroscopy of GO and NrGO films (c) FTIR spectra for GO and NrGO.

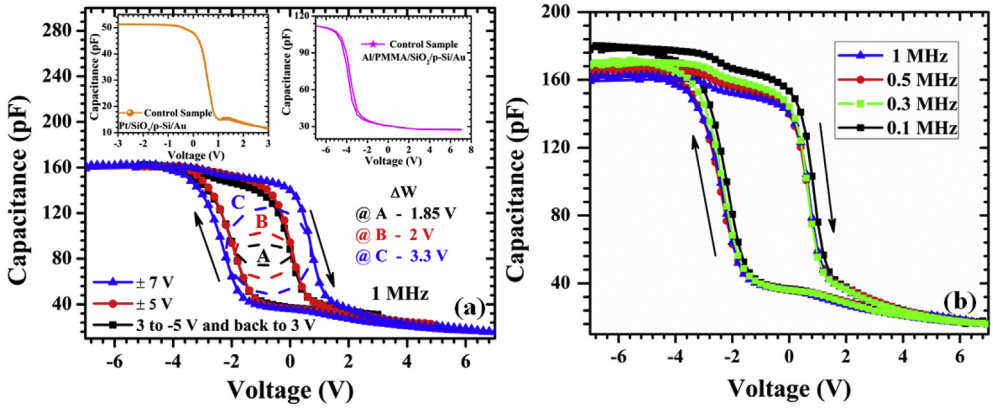

Fig. 3. Cyclic C–V characteristics of Al/PMMA/NrGO/SiO2/p–Si/Au FG–NVFM for (a) different sweep voltages at 1 MHz; (b) with variation in frequency from 0.1 to 1 MHz. Inset in (a) shows the Cyclic C–V characteristics for the control samples Pt/SiO_2/p–Si/Au and Al/PMMA/SiO_2/p–Si/Au showing negligible hysteresis.

in the NrGO layer [3,4,38,39]. The hole trapping may be possible due to the presence of defects in the N–rGO [4,28,29]. Over than above, the observed ΔW (~3.3 V @ ± 7 V) for NrGO based Al/PMMA/NrGO/SiO_2/p–Si/Au, FG–NVFM is considerably higher or comparable with counterparts; CNT (ΔW ~ 0.3 V @ ± 3 V), graphene (ΔW ~ 2 V @ ± 7 V), GO (ΔW ~ 1.4 V @ ± 5 V), rGO (ΔW ~ 7.5 V and 9.4 V @ ± 14 V and ±20 V, respectively) based NVFM [3–5,7,40], also summarized in Table 1.

Further, the total number of charge carriers stored in the FG, ML–NrGO (N_{MLNrGO}) are computed with following relation [3,41],

$$N_{MLNrGO} = \frac{\Delta W \times \varepsilon_0 \times \varepsilon_{PMMA}}{q \times t_{PMMA}}$$

Where, ε_0, ε_{PMMA}, q and t_{PMMA} are the permittivity of the free space, the dielectric constant of the blocking layer, electronic charge and thickness of the blocking layer, respectively, hence, the computed N_{MLNrGO} is ~1.5×10^{12} cm^{-2}. Even though, the calculated charge carriers are slightly less than the as reported for ML graphene and derivatives [3–5,41]. It might be possible due to suppression of DOS near the Fermi energy level as an effect of N–doping [28,42], incorporation of low dielectric constant blocking layer with respect to reported; Al_2O_3 (ε_{Al2O3} ~ 8), HfO_2 (ε_{HfO2} ~ 19) [3–5,41]. Besides this, the presence of thicker blocking layer (t_{PMMA} ~ 50 nm) as compared with Al_2O_3 (15 nm) and HfO_2 (30 nm) reported in Refs. [3–5,41], may be another possible reason for lower N_{MLNrGO}. Although, the presence of substantial higher memory window (ΔW) ~ 3.3 V @ ± 7 V with respect to ± 20 V, ± 18 V, ±15 V earlier reported, reveals the potential candidature of Al/PMMA/NrGO/SiO_2/p–Si/Au structures for low voltage, FG–NVFM applications [3–5,41]. More than this, the C–V characteristics of the fabricated Al/PMMA/NrGO/SiO_2/p–Si/Au FG–NVFM exhibits two interesting features, favorable for memory devices. Firstly, the hysteresis is centered close to 0 V, dictate the low voltage operation with distinguishable low and high states and secondly fast switching (from inversion to accumulation and back) response with respect to driving voltage [43]. Fig. 3 (b) shows the trivial right shifted C–V curves and negligible variation of V_{fb} (~0.3 V) as a function of variation in frequency (0.1–1 MHz) for the fabricated Al/PMMA/NrGO/SiO_2/p–Si/Au, FG–NVFM. The C–V curves as a function of frequency for the fabricated structures, evidently confirm that the significant large ΔW at low voltage is due to charge trapping and detrapping in the NrGO layer and not due to random defects, dielectric polarization or ionic displacement [44]. The minimal increase in the accumulation capacitance and slightly right shifted V_{fb} at lower frequencies during forward sweep may be attributed to the different response time of trapped/detrapped charges, available traps and driving voltage [44].

Fig. 4 (a) shows the |J|–V characteristics for Al/PMMA/NrGO/SiO_2/p–Si/Au, FG–NVFM. The measured |J| for the fabricated Al/PMMA/NrGO/SiO_2/p–Si/Au structure at dc voltage of 10 V is ~7 nA/cm^2. The lower leakage current density (ΔW ~ 3.3 V @ ± 7 V & |J| ~ 1.9×10^{-8} A/cm^2 @ − 1 V) is an indication of the elevated

Table 1
Summary and Comparison of the present work (NrGO floating gate) with previously reported CNT, GO, rGO based flash memory structures.

Floating Gate	Blocking Layer	Blocking layer Thickness (nm)	Sweep Voltages (in V)	Memory Window (in V)	Ref
Multi layer rGO	Al_2O_3	15	±8	~1.5	[3]
			±10	~2.6	
			±14	~4.2	
			±18	~6.8	
Multi layer rGO	Al_2O_3	22	±14	~3	[4]
			±16	~5.8	
			±18	~8	
			±20	~9.4	
Single layer graphene	Al_2O_3	~35	±7	~2	[5]
Multi layer graphene	Al_2O_3	~35	±7	~6	
GO	Al_2O_3	~15	− 5 to 8	~2.3	[7]
			− 5 to 14	~7.5	
rGO	Al_2O_3	~15	±4	1.4	
CNT	HfAlO	–	±3	0.4	[40]
NrGO	PMMA	~50	±3	1.85	This work
			+3 to − 5	2	
			±7	3.3	

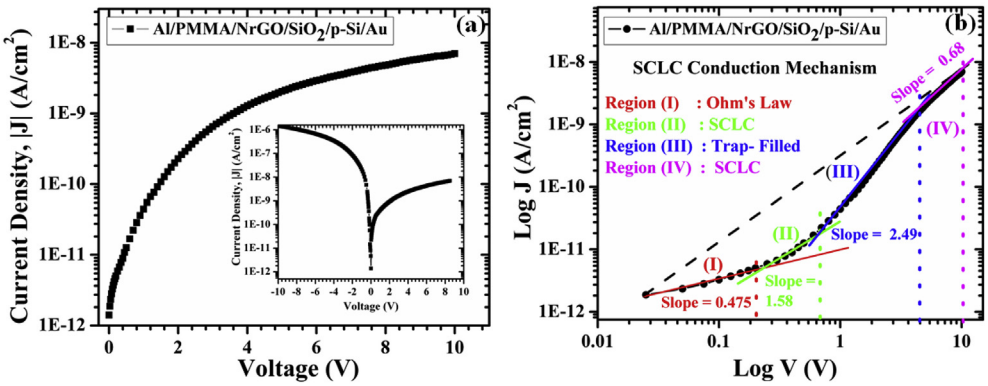

Fig. 4. (a) |J|–V characteristics for Al/PMMA/NrGO/SiO_2/p–Si/Au FG–NVFM; (b) Log |J|– Log (V) plot for positive applied voltage (0–10 V) at room temperature for Al/PMMA/NrGO/SiO_2/p–Si/Au FG–NVFM confined within a "triangle". Inset in (a) shows the |J|–V for ± 10 V.

reliability and feasibility to use Al/PMMA/NrGO/SiO_2/p–Si/Au, for flash memory applications [5]. Under applied bias the charge carriers from the p–Si tunnels through the thin SiO_2 layer and are trapped in the NrGO floating gate. The various tunneling mechanisms are explained in Fig. 4 (b). With the NrGO layer (Al/PMMA/NrGO/SiO_2/p–Si/Au devices) and low applied bias, the injected charge carriers may be trapped at the available defects close to the NrGO/SiO_2 interface or at the NrGO layer and result in the significant memory window. Whereas, with the increase in applied bias, the memory window increases as clearly perceived from the results (Fig. 3 (a)). It might be due to the trapping of charge carriers at the sites available in bulk/multi layer NrGO or at interface close to the PMMA/NrGO interface. But as shown in |J|- V curve, Fig. 4 (a) the gate leakage of ~ nA order, clearly reveals that charge carriers are surely trapped in above stated possible layers and corresponding interfaces.

Additionally, a double log (Log J – Log V) plot to clearly understand the different current conduction mechanisms in the fabricated Al/PMMA/NrGO/SiO_2/p–Si/Au, FG–NVFM structures is shown in Fig. 4 (b) [44,45]. At low voltages, region (I), the J–V characteristics correspond to the Ohm's behavior (liner region, $J \propto V$), implying higher thermally generated carriers density compared with the injected carrier density at the interface between Al and PMMA [45]. While, the further increase in the bias voltage, region (II), greater than transition voltage (V_{tr}), V_{tr} = ~0.2 V, a strong injection in the J–V characteristics are noticed resembling a space charge limited current (SCLC). In this region, the significantly large number of charges are injected in to the PMMA, thus, the injected charges are trapped in the available trapping sites/defects in the ML–NrGO leading to a redistribution of charges. Hence, the available trap sites/defects in the ML–NrGO are filled, a space charge appears, leading to memory–switching characteristics [44,45]. Beyond this in region III, the further increase in applied bias (>V_{tr}) may increase the density of injected carriers in PMMA, hence the charges can be trapped in ML–NrGO which in turn leads to in a trap–filled limit (TFL) condition. During TFL, due to high applied bias the charges may penetrate to the SiO_2 thus, resembles the transition of the J–V curve from trapped to trap free and hence, the current suddenly rises from low trap limited values to high trap. The bias voltage required to fill the traps is termed as trap–filled limit voltage (V_{TFL}), V_{TFL} = ~0.66 V. Beyond V_{TFL}, SCLC (square region, $J \propto V^2$), region (IV), a space charge layer is build up, the trap in the ML–NrGO are saturated. Thus, the current is majorly governed by the space charge and no more free carriers are injected.

The retention (C–T) characteristics of the fabricated Al/PMMA/NrGO/SiO_2/p–Si/Au memory devices with a write pulse of ±7 V in height and 100 ms in duration and followed by read voltage near V_{fb} of – 0.5 V is shown in Fig. 5. The write pulse of – 7 V and +7 V corresponds to C_{LOW} and C_{HIGH}, respectively, while the C_{MID} ((C_{HIGH} + C_{LOW})/2) corresponds to the mid capacitance. As clearly noticed from the Fig. 5 (0–~500 s), that there is an exponential rise in C_{LOW} and also an exponential decay in C_{HIGH} with respect to time. It depicts from the C–T characteristics that, till ~10^4 s, the C_{HIGH} and C_{LOW} remain distinguishable with ~30% charge loss, and on further extrapolation, it is observed that C_{HIGH} coincides with C_{MID} at ~10^5 s or beyond. Hence the ML–NrGO based Al/PMMA/NrGO/SiO_2/p–Si/Au FG–NVFM devices shows retention for upto ~10^5 s. The obtained retention for the ML–NrGO based Al/PMMA/NrGO/SiO_2/p–Si/Au NV–FGFM is considerably higher or comparable than its counterparts CNT, GO, rGO based NV–FGFM (~10^4 s) [3–5,7,40,45]. Thus, the fabricated Al/PMMA/NrGO/SiO_2/p–Si/Au FG–NVFM devices are suitable for EEPROM type embedded memories and organic flexible electronics applications.

4. Conclusions

To conclude, we demonstrate ML–NrGO sheets as a potential contender for charge storage in Al/PMMA/NrGO/SiO_2/p–Si/Au, FG–NVFM devices. The significantly large ΔW and strong retention at low sweep voltages are impressive for such ultrathin 2D sheets and point to the unique properties on NrGO. ML–NrGO owing to a high work function and high DOS is opted in the present investigations as compared with the single layer NrGO. Additionally, with the ML–NrGO we observe a rapid and clear saturations of the program transients, thus indicates reduced ballistic transport

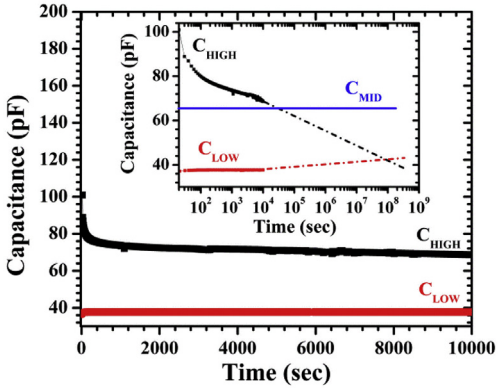

Fig. 5. C–T characteristics of Al/PMMA/NrGO/SiO_2/p–Si/Au FG–NVFM. inset shows the C_{HIGH}, C_{MID} and C_{LOW} capacitances.

perpendicular to the NrGO. The advantage of the present FG–NVFM is that the cost effective NrGO with ease of solution–processable and ink–jet printable, makes it compatible with low temperature applications, i.e., memory storage system based on flexible organic electronics.

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