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Design of a Charge Sensitive Amplifier for Particle Detection Application in BCD 180 nm Technology

H. Shrimali,^a A. Joshi,^a E. Ruscino,^b I. Yadav,^{a,1} S. Sharma,^a V. Liberali,^c
and A. Andreazza^c

^a*School of Computing and Electrical Engineering, Indian Institute of Technology Mandi, India*

^b*INFN Sezione di Genova, Italy and Università degli Studi di Genova, Via Dodecaneso, 33, 16146 Genova, Italy*

^c*INFN Sezione di Milano, Italy and Università degli Studi di Milano, Via Festa del Perdono, 7, 20122 Milano, Italy*

E-mail: indu_i@students.iitmandi.ac.in

ABSTRACT: This paper presents the design of charge sensitive amplifier (CSA) for silicon particle detection. This is the first attempt to design an analog processing circuit of the 47×6 silicon detector matrix in BCD 180 nm technology. A unit sensor pixel is realized as a diode with a dimension of $250 \times 50 \mu\text{m}^2$ and the analog front end of the sensor is confined in the sensor diode itself to achieve 100 % fill factor. A single stage, single ended, low power and area efficient folded cascode amplifier is designed as a basic building block of the CSA. Further, an on-chip corner control circuit is designed to achieve cross-corner (process variations) functionality. The proposed corner control circuit is kept outside the sensor matrix and reduces the power consumption in the CSA. The complete CSA and the corner control circuit occupy $65 \times 25 \mu\text{m}^2$ and $38 \times 21 \mu\text{m}^2$ area per pixel respectively. Noise floor of the CSA within the signal band is $201 \text{ nV}/\sqrt{\text{Hz}}$ and it typically consumes $11 \mu\text{A}$ from a 1.8 V of supply voltage (V_{DD}).

KEYWORDS: Analogue electronic circuits, Particle tracking detectors, Front-end electronics for detector readout.

¹Corresponding author.

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1 Introduction

The high voltage and high resistivity CMOS pixel detectors are gaining popularity for the large area pixel trackers of the large hadron collider (LHC) [1–3]. The capacitively coupled pixel detector is a CMOS sensor whose output is captured by an analog front end and it is then coupled to a readout chip designed to operate in LHC environment through a thin dielectric layer using hybrid IC design techniques [4–6]. A three well process (Figure 1(a)) is particularly attractive for particle detectors since it is possible to obtain 100% fill factor theoretically. However, achieving 100% fill factor while maintaining signal integrity is a challenging task.

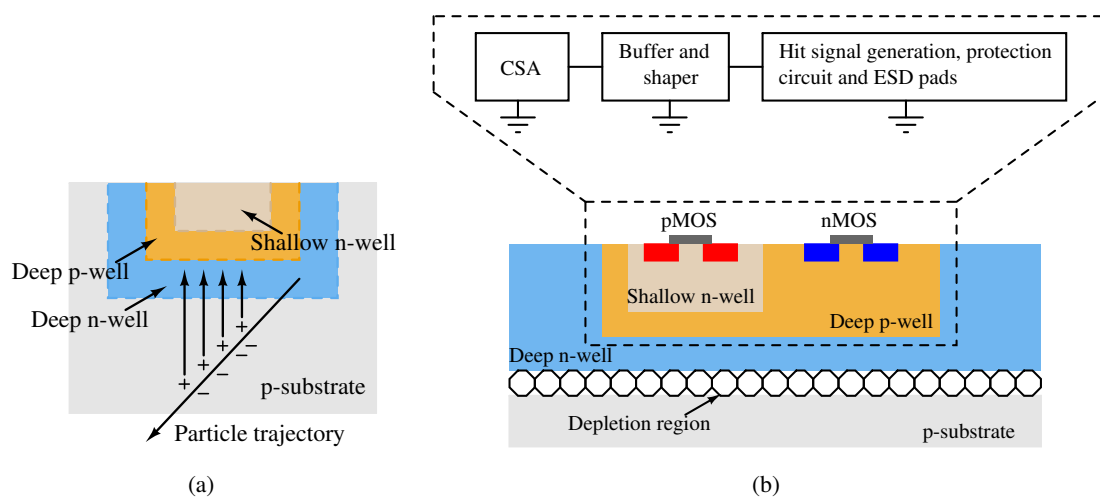


Figure 1. (a) A triple well process where charge collection is done by deep n-well electrode and shallow n-well is used for pixel electronics, (b) simplified section of unit pixel cell and the block diagram of analog signal processing circuit.

Figure 1(b) shows the block diagram of front end analog signal processing circuit. STMicroelectronics' 180 nm BCD8 technology is a triple well process in which deep n-well acts as a collecting electrode, a shallow n-well contains the pMOS transistors of the pixel electronics [7, 8] and the nMOS transistors are hosted in the deep p-well. An excursion of particle from the substrate will generate a negative voltage spike at the cathode of the pixel. This signal is AC coupled to the charge sensitive amplifier (CSA) [9]. Design of the CSA is critical because single ended architecture itself is prone to both process variations and signal degradation. In addition to this, current mirrors which generate the bias voltage for proper operation of the amplifier contribute the common mode noise. Increasing the size of input transistor of such an amplifier does not improve noise performance because of the bias current limitation [9].

This paper presents the design of CSA of a silicon detector with 100 % fill factor. This is the first work presenting the analog front end of 47×6 pixel matrix in BCD process technology and it investigates the technique of pixel detector circuit implementation to achieve better noise performance and process reliability. The design is targeted to be compatible for hybridization with front end I4 (FE-I4) chip of ATLAS experiment [10, 11]. A current injection circuit is designed to simulate the sensor's operation. Further, an on-chip corner control circuit is included in the pixel matrix separately to obtain process independent functionality.

2 Analog signal processing circuits

2.1 Current injection circuit: simulation environment for the particle detector

The proposed simulation environment to emulate the effect of particle injection at the n-well of the sensor diode is shown in Figure 2(a). A parasitic diode between the p-substrate and the deep

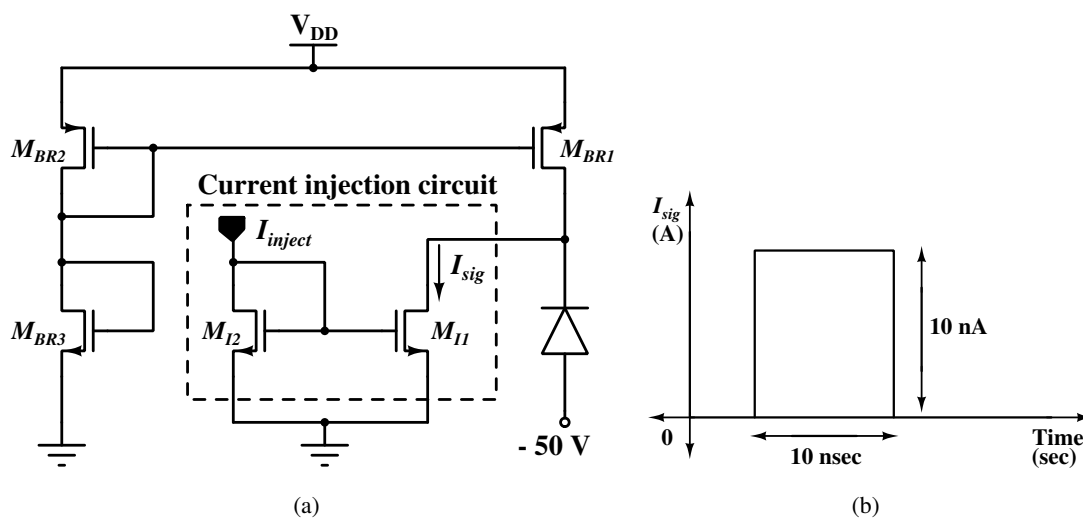


Figure 2. (a) The schematic of current injection circuit, (b) variable width injected current signal at the deep n-well of the diode.

n-well realizes the pixel sensor. This diode is connected in reverse bias condition by connecting the p-substrate to a negative potential, (-50 V). The deep n-well is biased using a high value resistance which is connected to a positive voltage with respect to the substrate. This bias resistor

is implemented using transistor M_{BR1} . The bias resistance helps to deplete larger portion of the substrate and the n-well, and also prevents the sensor signal from coupling to the supply rail. STMicroelectronics' BCD8 process technology with bipolar, CMOS and DMOS devices provides such a functionality; where high voltage sensing can be isolated from low voltage electronics [12].

When a charged particle crosses the depletion region, it generates on an average 100 electron-hole pairs per micrometer depleted width. Depending on the size of the depletion region, it corresponds to a signal of $1000 e^-$ to $20000 e^-$ [9]. The equivalent current can be injected at the cathode terminal of the diode using the dashed block in Figure 2(a) to simulate the behaviour of sensor and measure the response of its front end electronics. The width of transistor M_{I2} is 100 times greater than the width transistor M_{I1} . Therefore, a few nano Ampere current pulses can be obtained from a larger external input signal. The external current injection (I_{inject}) is implemented using an off-chip pulse generator and a $1 \text{ k}\Omega$ resistor. As shown in Figure 2(b), the effect of number of electron charge generated by particle hit can be varied by varying the pulse width of external current input signal. The relation between current pulse input and the number of electrons is $i_H \cdot t_W = n \cdot e^-$, where, t_W is the pulse width, i_H is the pulse height, $e^- = 1.60 \times 10^{-19} \text{ C}$ is the electron charge and n is the number of electrons.

2.2 Charge sensitive amplifier (CSA)

A single stage amplifier with negative capacitive feedback is designed to function as the CSA. The CSA consists of a gain stage, a DC blocking capacitor and a DC biasing circuit. In the case of particle hit, the detected transient signal at the n-well of the sensor diode is amplified by the CSA. The CSA with DC biasing circuit is shown in Figure 3. The complete schematic of folded cascode

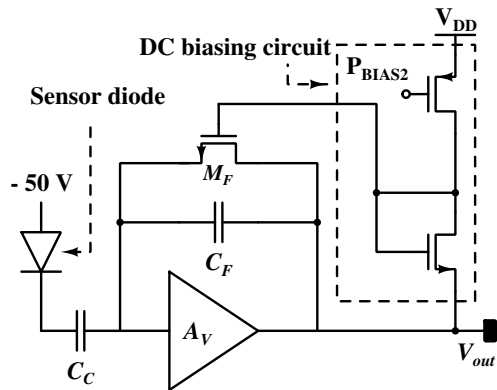


Figure 3. The schematic of charge sensitive amplifier including the DC biasing circuit for resistive feedback.

amplifier used in the CSA is shown in Figure 4. A pMOS devices is better in terms of noise because of its relatively slow mobility compared to an nMOS transistor. Hence, the CSA is designed using a pMOS input stage. The pMOS transistors of the pixel are placed in shallow n-well to reduce the cross-talk noise.

A resistive feedback formed by the transistor M_F provides the DC bias to the input transistor [13, 14]. Further, the buffer circuit using of a common drain amplifier (not shown here for simplicity)

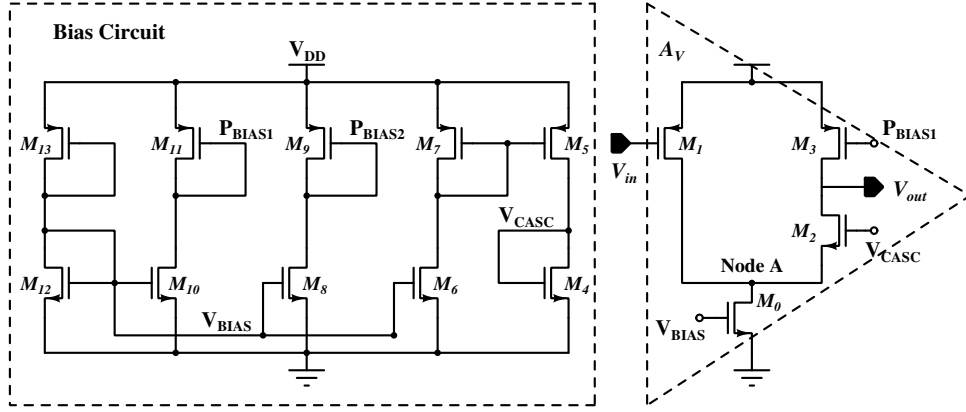


Figure 4. The complete schematic of single stage single ended folded cascode amplifier used in the CSA.

is connected at the output of CSA to drive the capacitive load of 1 pF. The RC-CR circuit formed by the buffer also behaves as a low pass filter to limit the band of signal.

Analysis of the CSA

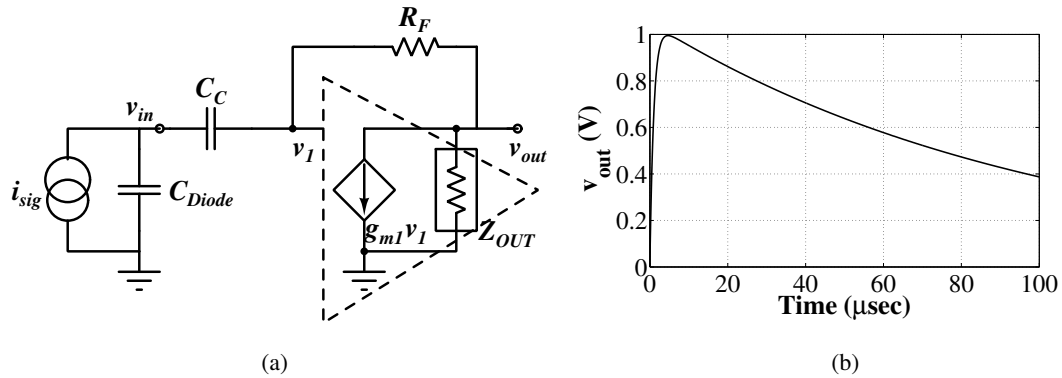


Figure 5. (a) Equivalent model of the CSA to calculate closed loop transfer function, (b) an example case study to understand the transient response of the CSA.

The output resistance of the amplifier (R_{OUT}) and the resistance across the node A (R_A) are calculated as follows:

$$R_{OUT} = g_{m2}r_{o2}(r_{o1}||r_{o0})||r_{o3}, \quad R_A = \frac{1}{g_{m2}}||r_{o1}||r_{o0}, \quad (2.1)$$

where, g_{mi} and r_{oi} are the transconductance and the output resistance of i^{th} transistor.

$C_L = C_{GD2} + C_{GD3} + C_{IBUFF}$ and $C_A = C_{GD0} + C_{GD1} + C_{GS2}$ are the total capacitances seen at node V_{out} and A respectively. Moreover, $R_{OUT} \gg R_A$ and C_L is relatively larger than C_A because of the input capacitance of buffer stage (C_{IBUFF}). Therefore, the amplifier can be reduced to a first order system with voltage gain, $A_V(s) = \frac{-A_{dc}}{(1+s/\omega_{p1})}$; where, $\omega_{p1} = \frac{1}{R_{OUT}C_L}$ is the dominant pole in the amplifier's transfer function. A_{dc} is the gain of amplifier at low frequency.

The equivalent small signal model used to derive the transfer function of the CSA is shown in Figure 5(a). A 90 fF metal-oxide-metal (MOM) capacitor, C_C is used to filter out the DC signal from the detected transient signal. The closed loop transfer function (v_{out}/v_{in}) is therefore expressed as:

$$A_{CL}(s) = \frac{-s \cdot R_F \cdot C_C \cdot A_{dc}}{\left(1 + \frac{s}{\omega_{p1}}\right) (1 + s \cdot R_F \cdot C_C) + A_{dc}} \quad (2.2)$$

As shown in Figure 2(b), $i_{sig}(t)$ can be modelled as a $\delta(t)$ function. Hence the transient response of CSA is formulated as:

$$v_{out}(t) = \frac{-C}{p_1 - p_2} [e^{-p_2 t} - e^{-p_1 t}], \quad (2.3)$$

where, C is a constant, p_1 and p_2 are closed loop poles. Eq. 2.3 is plotted in Figure 5(b) as an example. The exponentially decaying response is because of the resistive feedback provided by the transistor M_F . This feedback acts as a continuous reset. It stabilizes the CSA and discharges the feedback capacitor after the amplification.

The noise performance of the CSA is an important aspect of the processing circuit unit for AC and transient analyses. Noise is a trade-off between gain, area and power consumption. The noise in CSA is worth analyzing because single ended architecture tends to contribute noise if not designed carefully. In addition to noise contribution by transistors M_0 , M_1 and M_3 ; common mode noise arises from the current mirrors used to generate the bias current of amplifier. Analysis reveals that the presence of finite resistance at node A in Figure 4 is the reason behind the noise contribution from transistor M_0 and current mirror M_{11} . The output noise from the current mirror transistors can be reduced by connecting a big capacitor between the gate of the current mirror transistor and the reference node [15]. The value of the capacitor depends on the requirement of the noise reduction. Figure 6(a) shows the input referred noise of the amplifier plotted for different values of capacitance at the gate M_0 . It is possible to achieve nearly $25 \mu V_{rms}$ improvement in the noise performance by connecting a 3 pF capacitor. However, area overhead introduced by this capacitor makes this technique impractical in this scenario. So, we resort to increase the gate capacitance by increasing the width of tail current M_0 and by generating bias voltage for the succeeding circuit from the current mirror M_{11} . This increases the gate-source capacitance (C_{GS}) to reduce noise by decoupling it to ground. Moreover, noise reduction is achieved by increasing the length of transistors M_0 , M_3 , M_{11} and M_{12} . The increment in the channel length reduces the channel length modulation and decreases the transconductance of respective device.

2.3 Corner control circuit

The single ended folded cascode amplifier in the CSA has a technological and architectural drawback when subjected to power and area constraints. It is difficult to achieve cross corner functionality without compromising on power budget. To overcome this drawback, we predict the circuit operation at every corner and provide a corrective measure to lift the gain at this corner. The simulations at low gain corner reveal that the current flowing through the tail current source (M_0 in Figure 4) drops severely and M_0 enters into the linear region. As shown in the Figure 6(b), a separate corner control circuit is designed to enhance gain of the amplifier at process corners. The circuit is only active for a given corner and is stagnant otherwise. Working of this circuit relies on tuning the switching

threshold of back to back inverters at different corners and controlling an additional current source connected in parallel with the tail current of the CSA. While operating in a low gain corner, the controlling branch (dashed block in Figure 6(b)) generates a DC voltage (V_{CNTL}) which is greater than the switching threshold of the inverter formed by M_{17} and M_{18} . This turns on the switch to connect the current source (I_{CNTL}) at node A in Figure 4. V_{CNTL} is less than the switching threshold of the inverter in other corners and hence no current flows through M_{23} . The corner control circuit consumes $4.6 \mu A$ when idle and $23.8 \mu A$ when active. It can be noted that without this circuit, $20 \mu A$ current source would have been required to achieve cross corner functionality.

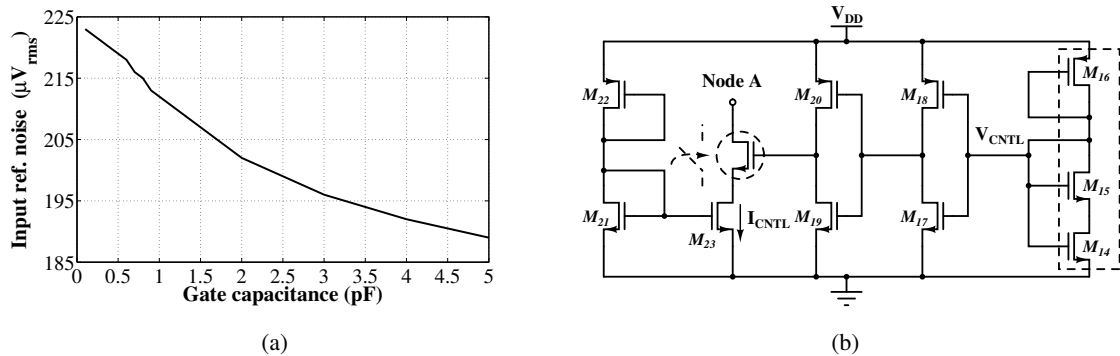


Figure 6. (a) Input referred noise of the CSA for different values of the gate capacitance of M_0 , (b) the schematic of corner tuning circuit used to obtain cross-corner functionality.

3 The Layout and the Simulation Results

The complete chip contains 282 sensor pixels, 12 current injection circuits and 147 control circuits and is designed in a BCD 180 nm technology. The area of sensor diode is $250 \times 50 \mu m^2$. However, the pixel diode is designed with the area of $271.73 \times 54.35 \mu m^2$ considering the scaling factor of 0.92 of STMicroelectronics' technology [12]. The CSA occupies $65 \times 25 \mu m^2$ of the diode. The layout of CSA is shown in Fig 7(a). Fig 7(b) shows the layout of the complete chip. The area of the complete chip is $3317 \times 4398 \mu m^2$.

Figure 8(a) shows the AC response of CSA. The effect of zero frequency (because of AC coupling) in the circuit is visible from the Figure 8(a). Noise performance of the amplifier is plotted in Figure 8(b). The CSA has thermal noise floor of $201 \text{ nV}/\sqrt{\text{Hz}}$ and the input referred noise is $168 \mu V_{rms}$ in the signal band of 225 kHz to 1.225 MHz. The transient response of CSA is shown in Figure 9. A current pulse with amplitude of 30 nA and width of 30 ns (5617 electrons) is injected into the sensor diode. The inset in Figure 9 shows the negative voltage spike generated at the deep n-well of the sensor. As explained in Section 2.2, the output of CSA achieves a peak of 1.62 V and decreases thereafter because of the feedback action.

4 Conclusion

The pixel array is designed compatible with front end I4 (FE-I4) chip of ATLAS experiment. Maximum fill factor is achieved by hosting the front end analog circuitry into the diode sensor area.

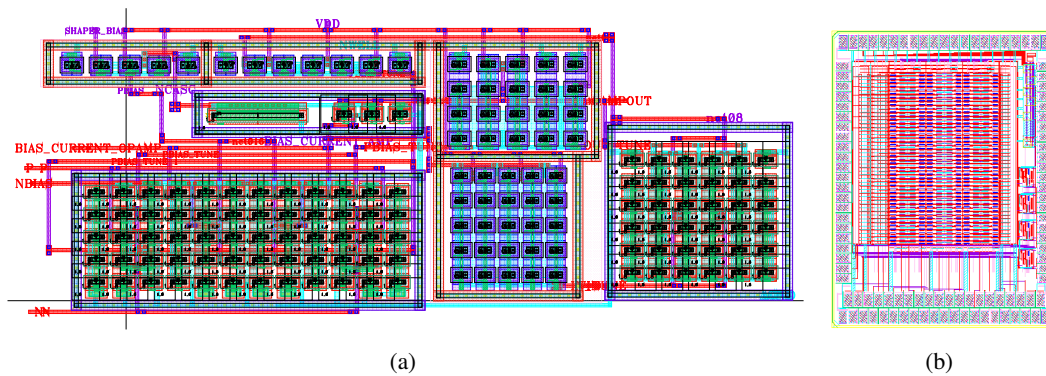


Figure 7. (a) Layout of the CSA, (b) layout of the complete chip showing pixel arrangement and ESD pads.

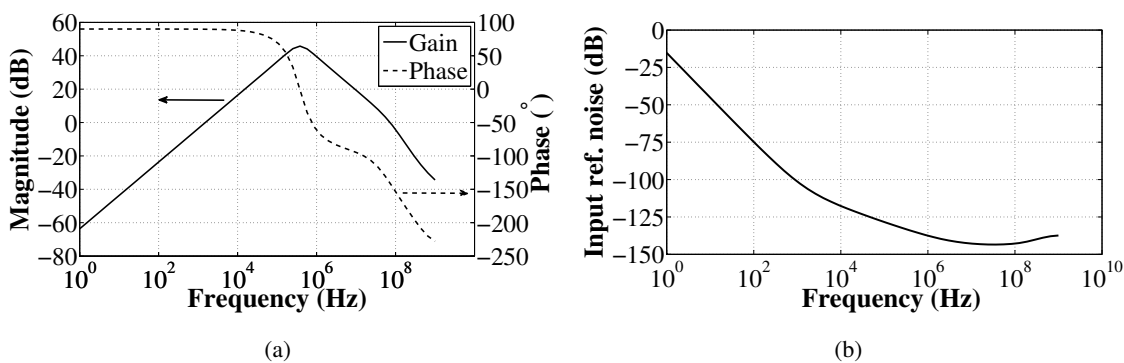


Figure 8. (a) Magnitude and phase response of the designed CSA, (b) input referred noise of the CSA.

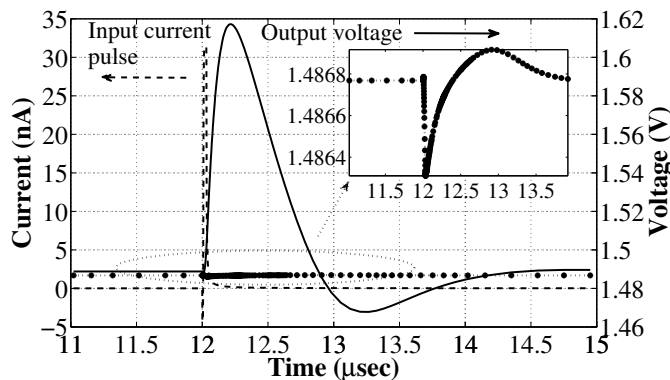


Figure 9. Transient response of the CSA when current pulse with amplitude of 30 nA and width of 30 nsec is injected into the sensor diode.

The simulation environment consists of a current injection circuit to emulate the effect of particle injection. The single stage, single ended folded cascode amplifier is used as the core of CSA. The on-chip corner control circuit shows the process independent performance. The proposed corner control circuit occupies only $38 \times 21 \mu\text{m}^2$ area and reduces current consumption in the CSA from $30 \mu\text{A}$ to $15.6 \mu\text{A}$ per pixel.

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