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Frequency dispersion and dielectric relaxation in postdeposition annealed high-κ erbium oxide metal–oxide–semiconductor capacitors

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The origin of frequency dispersion in postdeposition rapid thermal and furnace annealing treated Pt/Er_2O_3/Si/Pt, metal–insulator–semiconductor–metal (MISM) structure is systematically investigated. The cause of frequency dispersion in Pt/Er_2O_3/Si/Pt, MISM structure is attributed to the dielectric relaxation in high-κ Er_2O_3, after suppressing the extrinsic effects such as parasitic, lossy interfacial layer, surface roughness, polysilicon depletion, quantum confinement, and oxide tunneling. Further, the Havrilian–Negami law is used to model the frequency dispersion in postdeposition rapid thermal and furnace annealing treated Pt/Er_2O_3/Si/Pt, MISM structure up to 250 kHz. It is suggested that to obtain an accurate capacitance value, the dissipation factor must be minimum for the MISM structure with nanometer scale oxides/insulators. Additionally, a methodology is proposed for simple and efficient correction of measured capacitance from capacitance–voltage and capacitance–frequency characteristics. Moreover, the flatband voltage shift/hysteresis, frequency dependent border traps are estimated ~0.45 V, ~3.35×10^{12} traps/cm^2 and ~0.18 V, ~1.84×10^{12} traps/cm^2 for postdeposition rapid thermal and furnace annealing treated Pt/Er_2O_3/Si/Pt, MISM structures, respectively. Therefore, postdeposition furnace annealing treatment is superior to achieve high-quality high-κ Er_2O_3 (κ ~16), with low frequency dispersion of ~9% up to 250 kHz and minimal hysteresis (~0.18 V) for next-generation complementary metal–oxide–semiconductor technology. *Published by the AVS.* https://doi.org/10.1116/1.4995809

I. INTRODUCTION

Scaling of integrated-circuit (IC) endures to be an unprecedented potential for the Si-technology in order to increase the functionality, performance, and also fuel market expansion. As the scaling of complementary metal–oxide–semiconductor (CMOS) transistor feature dimensions is approaching the nanometric regime, revolutionary challenges including the replacement of conventional gate oxide is becoming inevitable. High-κ dielectrics have emerged as a promising solution to continue the performance improvement of CMOS technology in accordance with Moore's law.[1–3] The state-of-the-art CMOS technology utilizes HfO_2 based gate dielectric with an ultrathin SiO_2 buffer layer, overall dielectric constant of gate stack (~<10),[4] and hysteresis (~0.29 V).[5] The next-generation IC's technology demands superior quality high-κ gate dielectrics (κ >10) in direct conformal contact with active silicon, not only for MOSFET's with low hysteresis but also for nonvolatile memories.[6–9] Numerous high-κ dielectrics are investigated in the past decade such as Al_2O_3, La_2O_3, HfO_2, and Y_2O_3, but with high hysteresis of ~0.58, ~0.32, ~0.29, and ~0.23 V, respectively.[5,10] Among the alternate high-κ dielectrics, erbium oxide (Er_2O_3) has attracted the scientific community for CMOS technology due to its high-κ (~8–20), the higher conduction band offset (~3.5 eV), thermodynamic and kinetic stability, and lower leakage current density.[11–19]

For high-κ gate dielectrics, the dielectric constant (κ) is one of the major parameter, which is fundamentally extracted from capacitance–voltage (C-V) measurements in the accumulation region of the metal–oxide–semiconductor (MOS) structure and theoretically independent of frequency.[20,21] However, with the scaling of thickness of high-κ gate dielectric in the nanometer regime, frequency dispersion is perceived in the accumulation region of C-V characteristics, which becomes an impediment for parameter extraction, such as dielectric constant, oxide thickness, trap densities, the maximal width of the depletion layer, channel length, mobility, threshold voltage, bulk doping profile, and the distribution of the charges in dielectrics.[22–26] Moreover, frequency dispersion in high-κ dielectrics is considered as a major hurdle for their adoption in CMOS technology.[27–31] The frequency dispersion in high-κ gate dielectrics is generally classified into two types: (1) extrinsic causes and (2) intrinsic causes. The extrinsic causes are as follows: (1) parasitic effects, due to parasitic resistances and capacitances; (2) lossy interfacial layer effect, due to the interfacial layer with thickness comparable to high-κ thickness; (3) surface roughness effect, due to high rms surface roughness (>1 nm) of high-κ thin films; (4) polysilicon depletion effect, due to Poly-Si gate used in the MOS structure; and (5) quantum confinement and oxide tunneling effects, caused in ultrathin gate oxides (<6 nm). On the other hand, the intrinsic cause of frequency dispersion can be observed after suppressing the extrinsic causes and is basically the frequency dependence of κ value (also called "dielectric relaxation").[25,26] In addition, the intrinsic frequency dispersion is also related to the grain size in nanostructured crystalline materials and to the postdeposition annealing treatment.[21,28,29]

Majority of high-κ dielectrics suffer from the leakage problem due to the formation of polycrystalline phase during postdeposition annealing treatment in CMOS processing and results in the degradation of device reliability. Additionally,

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the epitaxial growth of single crystal high quality, high-κ oxides are difficult to account for process technology and also not cost effective. Therefore, exploitation of amorphous high-κ oxide as a possible future alternative perspective with minimum carriers scattering, better diffusion barrier, lower interface defects, superior thermal stability, and excellent electrical and physical properties is still an open challenge. In our previous work, superior quality amorphous Er_2O_3 thin films are reported for CMOS application.[18,19] However, limited literature is found regarding the frequency dispersion, dielectric relaxation, and hysteresis in amorphous gate dielectrics at nanometer thicknesses, especially Er_2O_3 high-κ dielectric, which forms the basis of this paper.

In this paper, the cause of frequency dispersion in postdeposition rapid thermal annealing (RTA) and furnace annealing (FA) treated high-κ Er_2O_3 based MOS capacitors is systematically investigated for the first time. After considering all the extrinsic causes of frequency dispersion, i.e., parasitic, lossy interfacial layer, surface roughness, polysilicon depletion, quantum confinement, and oxide tunneling effects, the intrinsic cause of frequency dispersion, i.e., dielectric relaxation in erbium oxide, is taken into account. Furthermore, the Havrilian–Negami (HN) mathematical model is used to fit the experimental data and to extract the dielectric relaxation parameters. Additionally, a methodology is proposed for simple and efficient correction of measured capacitance from capacitance–voltage and capacitance–frequency characteristics. Moreover, the modified single frequency correction technique with approximated series resistance (R_S) is compared with the dual-frequency correction technique. Finally, the hysteresis and border traps for postdeposition RTA and FA treated Pt/Er_2O_3/Si/Pt, MISM structure are estimated and explained with the proposed graphical band model.

II. EXPERIMENT

The metal–insulator–semiconductor–metal (MISM) capacitors were fabricated on P-type ⟨100⟩ oriented silicon (1–10 Ω cm). After standard Radio Corporation of America cleaning and hydrofluoric acid dip, deposition of Er_2O_3 ultrathin films was carried out using Techport RF-magnetron sputtering system from an erbium target (99.99%). The measured distance of erbium target from wafers was ∼7 cm. First, before sputtering on the active silicon surface, presputtering was done at 300 K, 60 W, and pressure of Ar/O_2 (45:5 sccm) for 10 min to eliminate the impurities on the target surface. Second, the deposition of ultrathin Er_2O_3 films was carried out at the RF power 60 W, 300 K, and pressure of Ar (50 sccm). Third, the ultrathin films of Er_2O_3 deposited Si samples were subjected to RTA treatment at 973 K for 30 s at fixed ramp-up rate (30 °C/s) in N_2 (one set) and with FA treatment at 973 K for 30 min in N_2 (other set) to improve the quality of the dielectric. After this, few samples were kept as backup for supplementary meteorological characterizations and the remaining samples were used for the top gate electrode formation. Finally, for the electrodes of the MISM structure, Pt thin films (∼60 nm) were sputtered with a circular area of $\sim 1.256 \times 10^{-3}$ cm^2 on top via a shadow mask and on the bottom after backside native oxide removal using standard buffered hydrofluoric acid (BHF) solution for back ohmic contact. For all the aforesaid sputter processes, the base and process pressures were maintained at $\sim 5 \times 10^{-6}$ and $\sim 6 \times 10^{-3}$ torr, respectively. The Pt/Er_2O_3/Si/Pt, MISM structures are fabricated in a standard Class 1000 clean room. The thickness (optical) of the deposited Er_2O_3 ultrathin films was measured to be ∼8.21 nm, using an Accurion EP3 imaging ellipsometer. Finally, the Pt/Er_2O_3/Si/Pt, MISM structure was electrically characterized at room temperature by C-V and capacitance–frequency (C-F) measurements in the parallel model using the Agilent B1500A system. The stoichiometry of Er_2O_3 thin films was analyzed by x-ray photoelectron spectroscopy (XPS) of Kratos Analytical, Ltd. (Kratos AXIS-165).

III. RESULTS AND DISCUSSIONS

Figure 1 shows the measured C-V characteristics of postdeposition RTA [Fig. 1(a)] and FA [Fig. 1(b)] treated

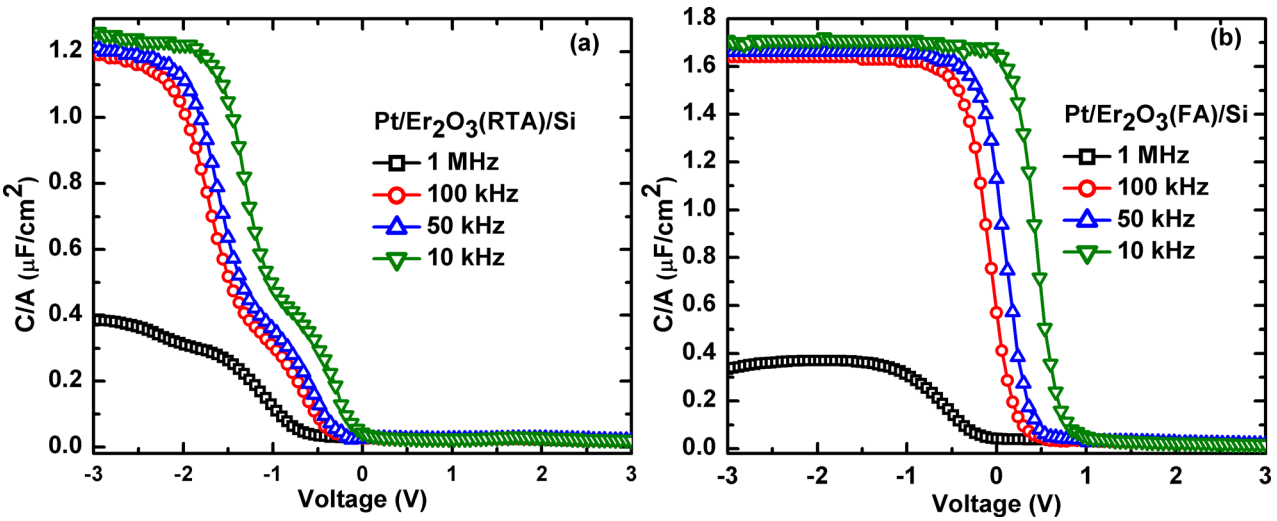

FIG. 1. (Color online) Measured C-V characteristics of (a) Pt/Er_2O_3 (RTA)/Si/Pt and (b) Pt/Er_2O_3 (FA)/Si/Pt, MOS capacitors with variation in frequency.

Pt/Er_2O_3/Si/Pt, MISM structure with the variation in frequency of 10 kHz, 50 kHz, 100 kHz, 1 MHz, and gate voltage sweep from accumulation (−3 V) to inversion (+3 V). From the C-V curves, noticeable frequency dispersion is observed in the flatband voltage (V_{fb}), the threshold voltage (V_{th}), and accumulation capacitance (C_{acc}). The parameters (V_{fb}, V_{th}) at frequency as extracted from the C-V curves are ∼(−2.25, −0.49 V) at 1 MHz, ∼(−1.99, −0.21 V) at 100 kHz, ∼(−1.90, −0.08 V) at 50 kHz and ∼(−1.62, 0.11 V) at 10 kHz, for Pt/Er_2O_3 (RTA)/Si/Pt, MISM structure and ∼(−0.96, −0.26 V) at 1 MHz, ∼(−0.26, 0.49 V) at 100 kHz, ∼(−0.1, 0.58 V) at 50 kHz, and ∼(0.23, 0.92 V) at 10 kHz for Pt/Er_2O_3 (FA)/Si/Pt, MISM structure. Here, the left shifted C-V curves of the Pt/Er_2O_3 (RTA)/Si/Pt, MISM structure is attributed to higher positive effective oxide charges originated in Er_2O_3 due to structural reorientation/relaxation and the formation of interfacial Er–O/Si–O bonds during RTA treatment.[32] Moreover, this significant variation in V_{fb} and V_{th} with variation in frequency is attributed to the frequency dependent border traps/slow states located close to the Er_2O_3/Si interface that exchange mobile charges with silicon.[33] Also, for Pt/Er_2O_3 (FA)/Si/Pt, MISM structure, the V_{fb} at low frequencies (10, 50, and 100 kHz) is higher than the ideal one (−0.50 V), which is attributed to the trapped charges in Pt/Er_2O_3/Si system.[34] In addition, the variation in accumulation capacitance (C_{acc}) from ∼1.26 to ∼0.38 μF/cm^2 and ∼1.71 to ∼0.33 μF/cm^2 is observed with variation in the frequency from 10 kHz to 1 MHz for Pt/Er_2O_3 (RTA)/Si/Pt and Pt/Er_2O_3 (FA)/Si/Pt, MISM structures, due to the extrinsic or the intrinsic cause of frequency dispersion. Therefore, the frequency dispersion in C-V measurements is investigated for extrinsic causes before proceeding to intrinsic causes in high-κ Er_2O_3 dielectrics.

Among the extrinsic causes, (1) the parasitic effects (Fig. 2) include the parasitic resistances and capacitances, e.g., cables, series contact, and bulk series resistance,[35–38] although two are of practical importance, i.e., (a) the imperfect back contact of the silicon substrate, and (b) the series resistance R_S of the quasineutral silicon substrate between the depletion layer edge beneath the gate and the back contact, including various contact resistances and cable resistances. Also, it is reported that the parasitic effects can be minimized by depositing a thin metal film at the back side of the silicon substrate.[30] Therefore, in this study, the back metal (Pt) contact was deposited just after back side native oxide etching by standard BHF solution to minimize the parasitic effects. In addition, open corrections are performed and included during measurements, to minimize the effect of cables resistances (R_S') and capacitances (C_S') shown in Fig. 2. Hence, the parasitic effects are neglected as a cause of frequency dispersion in this investigation. Moreover, the C-V characteristic curves are free from kinks at low frequencies signifies high-quality Er_2O_3/Si interface.[39] (2) The lossy interfacial layer effect which is due to the interfacial layer between the high-κ and silicon substrate is investigated by the interface analysis of the Er_2O_3/Si structure. For this, the cross-sectional HRTEM images Er_2O_3 (RTA)/Si and Er_2O_3 (FA)/Si interface are analyzed and reported in our previous work.[19] From the cross-sectional HRTEM images of the Er_2O_3/Si structure, it is observed that there is negligible lossy interfacial layer after postdeposition FA treatment and the Er_2O_3 (FA)/Si resulted in the sharp interface. However, an interfacial layer is observed in Er_2O_3 (RTA)/Si system, which decreases the overall dielectric constant measured from the Pt/Er_2O_3 (RTA)/Si/Pt, MISM structure. This lossy interfacial layer is due to a high ramp-up rate in RTA treatment that results in structural reorientation/relaxation at the Er_2O_3 (RTA)/Si interface and originates defects/effective oxide charges at the Er_2O_3/Si interface owing to the formation of Er–O and Si–O bonds onto the interface.

Further, XPS analysis is performed to confirm the possibility of lossy interfacial layer or erbium silicate ($ErSiO_x$) at the Er_2O_3/Si interface in the case of postdeposition RTA and FA treated Er_2O_3 thin films on Si. The core level Er 4d XPS spectra of postdeposition RTA and FA treated Er_2O_3 thin films on Si are shown in Figs. 3(a) and 3(d), respectively. Here, the single Er 4d peak observed at ∼169 eV could not be deconvoluted to multiple Gaussian–Lorentzian subordinate peaks. This signifies the formation of Er_2O_3 thin films with negligible erbium silicate. Further, the core level O 1s XPS spectra of postdeposition RTA and FA treated Er_2O_3 thin films on Si is shown in Figs. 3(b) and 3(e), respectively. The O 1s XPS spectra are deconvoluted to two Gaussian–Lorentzian subordinate peaks observed at ∼532.7 and ∼530.9 eV, respectively. The energy state at ∼532.7 eV is attributed to oxygen in Er_2O_3 whereas the energy state at ∼530.9 eV is attributed to the presence of interfacial Si–O bonds. These are readily visible in postdeposition RTA treated Er_2O_3 thin films as compared to postdeposition FA treated Er_2O_3 thin films on Si. Finally, the core level Si 2p XPS spectra of postdeposition RTA and FA treated Er_2O_3 thin films on Si are shown in Figs. 3(c) and 3(f), respectively. The Si 2p XPS spectra of postdeposition RTA treated Er_2O_3 thin films are deconvoluted to multiple Gaussian–Lorentzian subordinate peaks at ∼99.3, ∼101.9,

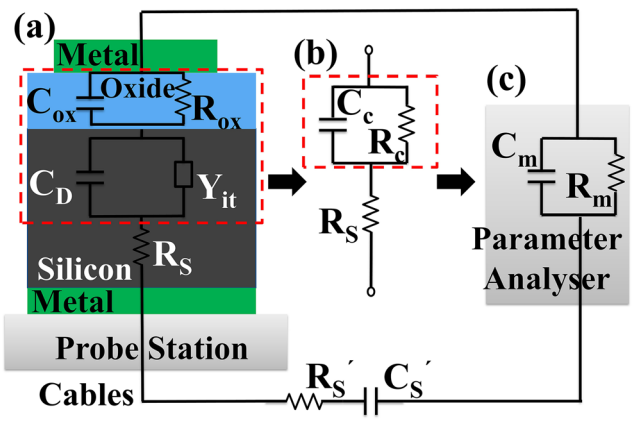

FIG. 2. (Color online) Frequency dispersion in the accumulation region of C-V measurements due to parasitic effects. (a) Equivalent circuit model including the oxide capacitance (C_{ox}), oxide resistance (R_{ox}), depletion layer capacitance of silicon (C_D), admittance due to interface states between silicon and oxide (Y_{it}), silicon substrate series resistance (R_S), cables capacitance (C_S'), and cable resistance (R_S'). (b) Equivalent circuit with corrected capacitance (C_c) and corrected resistance (R_c) which can be extracted by considering series resistance (R_S) from, (c) the measured capacitance (C_m) and the measured resistance (R_m) obtained from parameter analyzer.

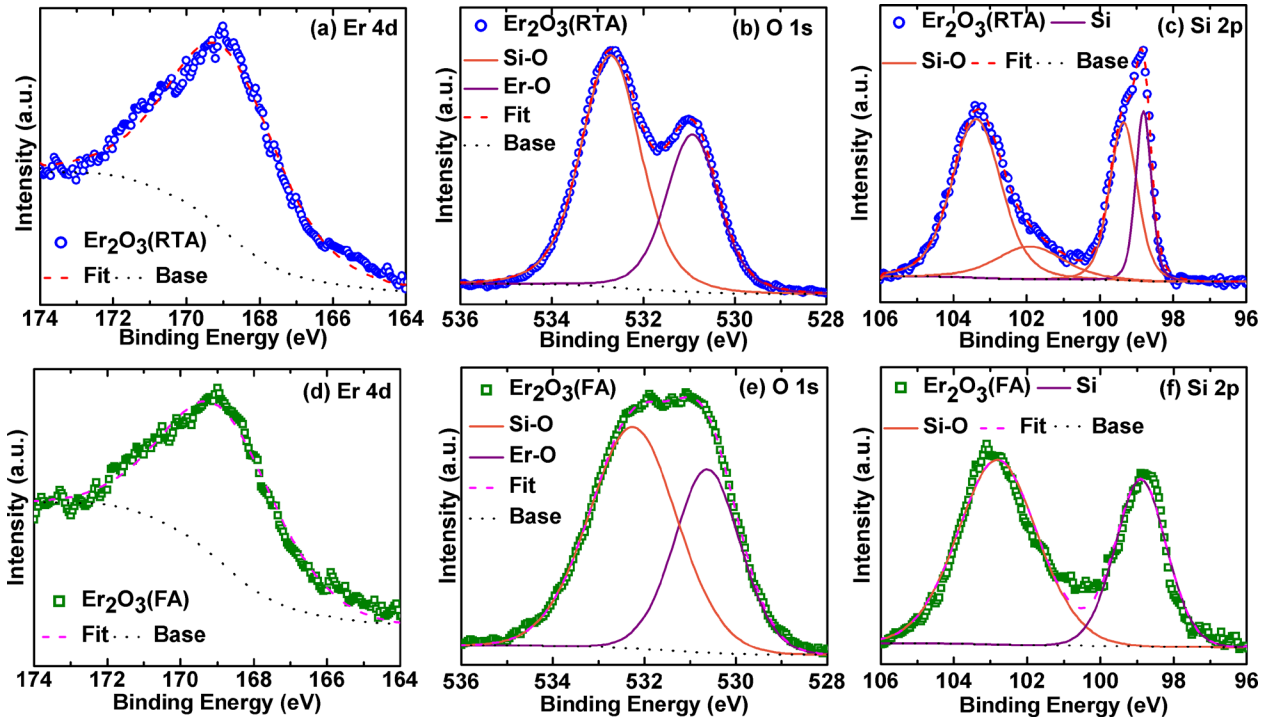

FIG. 3. (Color online) XPS spectra of Er 4d [(a) and (d)], O 1s [(b) and (e)] and Si 2p [(c) and (f)] peaks for the postdeposition rapid thermal annealed (RTA) and furnace annealed (FA) Er_2O_3 thin films on Si, respectively.

and ~103.4 eV, attributed to the formation of interfacial SiO_x, and ~98.8 eV endorsed to Si. On the other hand, the Si 2p XPS spectra of postdeposition FA treated Er_2O_3 thin films are deconvoluted to two Gaussian–Lorentzian subordinate peaks at ~98.9 and ~102.8 eV. The energy state at ~98.9 eV is ascribed to Si whereas the energy state at ~102.8 eV is recognized to the presence of interfacial Si–O bonds. This signifies that a minimal interfacial SiO_x layer (lower than the RTA treated Er_2O_3 thin films) is also present in the FA treated Er_2O_3/Si system without the formation erbium silicate ($ErSiO_x$).[17] Therefore, the lossy interfacial layer may be a reason for frequency dispersion in Er_2O_3 MOS capacitors. (3) The surface roughness effect, which is due to high rms surface roughness (>1 nm) of high-κ thin films. For this, the surface topography of Er_2O_3 ultrathin films is investigated with a standard tapping mode atomic force microscopy technique, reported in our previous work.[19] The rms surface roughness measured from 5×5 μm^2 scan area of postdeposition RTA and FA treated Er_2O_3 thin films is ~0.60 and ~0.45 nm, respectively, which reveals that the Er_2O_3 thin films are smooth enough and surface roughness does not contribute to the frequency dispersion in present investigations. (4) Polysilicon depletion effect is neglected, as the metal gate is used for fabricated Pt/Er_2O_3/Si/Pt, MISM structures. (5) Quantum confinement and oxide tunneling effects are generally neglected if the gate oxide thickness is >6 nm and not in the direct tunneling regime. Nevertheless, this is confirmed by the dissipation factor/instrumental errors. The dissipation factor (<1%) is also a proof for the lower leakage current in the MISM structure. The dissipation factor (D) is given by[40]

$$D = \frac{G_m}{2\pi f C_m}, \tag{1}$$

$$\%\,\text{error} = 0.1\sqrt{(1 + D^2)}, \tag{2}$$

where f, G_m, and C_m is the measured frequency, conductance, and capacitance, respectively. The % error for these measurements is <1% (shown in the inset of Fig. 4); therefore, the instrumental errors are minimal and the frequency dispersion due to the leakage current in the fabricated Pt/Er_2O_3/Si/Pt, MISM structure is eradicated. In addition, the grain size effect is also reported to be a source of frequency dispersion,[31] but it is also neglected in this investigation because the amorphous Er_2O_3 thin films are revealed from the grazing incidence x-ray diffraction analysis (reported elsewhere[19]).

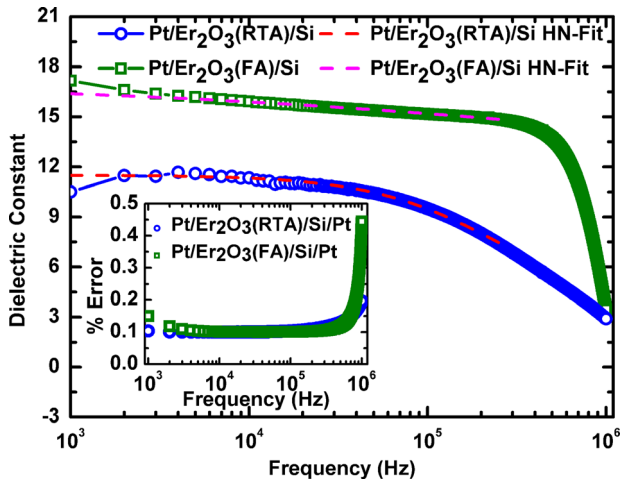

FIG. 4. (Color online) Frequency dependence of dielectric constant, extracted from C-F measurements in Er_2O_3 MOS capacitors. The inset shows the % instrument error with the variation in frequency obtained from Eqs. (1) and (2).

Therefore, the lossy interfacial layer in the Pt/Er_2O_3/Si/Pt, MISM structure is only expected to contribute to the κ value in the Er_2O_3 gate oxide. Except that all the extrinsic causes of frequency dispersion in high-κ based MOS capacitors are ruled out and this brings to the intrinsic causes of frequency dispersion, i.e., the frequency dependent κ value or dielectric relaxation in high-κ Er_2O_3 (FA).

For dielectric relaxation measurements, the Er_2O_3 MOS capacitors are electrically characterized at a fixed bias of -2 V in strong accumulation and the capacitance is measured with the variation in frequency. Further, the dielectric constant (κ) is estimated using the following relation:

$$K = \frac{C_{acc} t_{ox}}{\epsilon_o A}, \tag{3}$$

where C_{acc} is the accumulation capacitance of the MISM structure, ε_o is the permittivity of free space, A is the area of the gate electrodes, and t_{ox} is the thickness of the gate oxide. Figure 4 shows the calculated dielectric constant with the variation in frequency, extracted using Eq. (3), from C-F characteristics of Pt/Er_2O_3 (RTA)/Si/Pt and Pt/Er_2O_3 (FA)/Si/Pt, MISM structure. It is clearly observed that the κ value of RTA-treated Er_2O_3 ($\sim$11.5) is lower as compared to that of the FA-treated Er_2O_3 ($\sim$16.4), due to significant thickness of low dielectric constant lossy interfacial layer formed at the Er_2O_3/Si interface during the RTA treatment, which decreases the overall dielectric constant of the gate oxide. Additionally, the RTA-treated Er_2O_3 high-κ dielectric shows variation in dielectric constant from $\sim$11.5 to $\sim$7.4 with the variation in frequency from 1 to 250 kHz and further a sharp decrease to $\sim$2.9 at 1 MHz. On the other hand, the FA treated Er_2O_3 high-κ dielectric shows variation in dielectric constant from $\sim$16.4 to $\sim$14.9 with variation in frequency from 1 to 250 kHz and further a sharp decrease to $\sim$3.5 at 1 MHz. Hence, Er_2O_3 high-κ dielectric suffers from dielectric relaxation and the sharp decrease in the κ value at 1 MHz is attributed as the reason for the decrease in accumulation capacitance at a high frequency (1 MHz), although the FA treated Er_2O_3 showed improved frequency dispersion of $\sim$9.14% as compared to the RTA-treated Er_2O_3 of $\sim$35.65% up to 250 kHz and suitable for CMOS applications. Moreover, to interpret this frequency dispersion behavior of high-κ dielectrics, various dielectric relaxation mathematical models are proposed in literature, such as Curie–von Schweidler law, Debye law, Cole–Cole equation, Cole–Davidson, and HN.[21] Out of these, the HN model is the most advanced model because it combines both Cole–Cole and Cole–Davidson model with two fitting parameters, i.e., α and β related to the width and asymmetry of loss peak, respectively. Here, the aforesaid models were fitted with the measured K-F characteristics of Fig. 4, and the HN model fits best with the experimental results (from 1 to 250 kHz) as shown by the solid lines in Fig. 4. However, an abrupt decrease was observed above 250 kHz, which cannot be explained in terms of the HN relaxation model. The HN complex equation ($\in^*$) is as follows:

$$\in^*(\omega) = \in^{\infty} + \frac{\in_s - \in_{\infty}}{\left[1 + (i\omega\tau)^{1-\alpha}\right]^{\beta}}, \tag{4}$$

$$\in'(\omega) = \in^{\infty} + \frac{(\in_s - \in_{\infty})\cos(\beta \text{Ø})}{\left[1 + 2(\omega\tau)^{1-\alpha}\sin\left(\frac{\pi\alpha}{2}\right) + (\omega\tau)^{2(1-\alpha)}\right]^{\beta/2}}, \tag{5}$$

$$\in''(\omega) = \in^{\infty} + \frac{(\in_s - \in_{\infty})\sin(\beta \text{Ø})}{\left[1 + 2(\omega\tau)^{1-\alpha}\sin\left(\frac{\pi\alpha}{2}\right) + (\omega\tau)^{2(1-\alpha)}\right]^{\beta/2}}, \tag{6}$$

$$\text{Ø} = \tan^{-1}\left(\frac{(\omega\tau)^{1-\alpha}\cos\left(\frac{\pi\alpha}{2}\right)}{1 + (\omega\tau)^{1-\alpha}\sin\left(\frac{\pi\alpha}{2}\right)}\right), \tag{7}$$

where $\in'$ and $\in''$ are the real and imaginary parts of the H-N complex equation, respectively. The fitting parameters α ($0 < \alpha < 1$) and β ($0 < \beta < 1$) are related to the width and asymmetry of the loss peak, respectively. The parameters such as $\in'$, $\in_s$, $\in_{\infty}$, ω, and τ indicate the κ value, static dielectric constant, dielectric constant at a high frequency (1 MHz), angular frequency $\omega = 2\pi f$, and the relaxation time, respectively. The best fit of H-N equation (shown in Fig. 4) is found at $\alpha = \sim 0.87$, $\beta = \sim 0.44$, and $\tau = \sim 3 \times 10^{-7}$ s for the FA treated Er_2O_3 and $\alpha = \sim 0.41$, $\beta = \sim 0.96$, and $\tau = \sim 6.19 \times 10^{-7}$ s for the RTA treated Er_2O_3. Thus, it is attributed that the Pt/Er_2O_3 (FA)/Si/Pt, MISM structure showed superior dielectric relaxation behavior suitable for next-generation CMOS applications. Here, the mechanism behind the dielectric relaxation in high-κ Er_2O_3 may be due to (1) the combination of unbound Er^+ ions with the trap charges that generate dipole moment, and/or (2) ion movement of unbound Er^+ ions in the oxide that results in the dielectric relaxation,[41,42] and/or (3) contribution from the interfacial Si–O bonds at the Er_2O_3/Si interface.

From Fig. 4, a sharp decrease in the κ value is observed above 250 kHz. A similar kind of sharp decrease in the κ value above $\sim$300 kHz was observed by Lee *et al.*[43] and Kim *et al.*[44] But, sharp frequency dispersion was not observed even in gigahertz range when the same experiment was carried out in a network analyzer; therefore, the frequency dispersion above 300 kHz is attributed to uncompensated parasitic effects and is not clear.[43] Hence, to account this situation, the parasitic effects must be carefully reconsidered. Here, the sharp decrease in the κ value between 250 kHz and 1 MHz is ascribed to the uncompensated parasitic effects due to the instrumental error/dissipation factor at high frequencies as shown by the percentage error [obtained from Eqs. (1) and (2)] in the inset of Fig. 4. It is observed that the instrumental error is $\lesssim$0.1% below 250 kHz and increases to $\sim$0.5% at 1 MHz. Therefore, it is recognized that for accurate measurements, the instrumental error must be minimum for the MISM structure with nanometer scale oxides. Here, it must also be noted that the instrumental error at frequencies below 2 kHz also increases above 0.1%, due to the inability of the LCR meter to measure the capacitance at large conductance/resistance values.[45] Hence, it is attributed that in this work

for accurate parameter extraction, ~10 to ~250 kHz is the desired frequency range, although this frequency range can be improved by adopting high frequency layouts that work for gigahertz range also. Tao *et al.*[30] reported that the parasitic effects can be minimized by depositing a thin metal film at the back side of silicon substrate. But this is suspicious because the series resistance of the silicon substrate comes in series with the resistance of imperfect back ohmic contact and contributes as a parasitic effect in the measurement.

To compensate the parasitic effects variety of models and corresponding correction methods are proposed in literature: (1) single frequency C-V measurement followed by correction with approximated R_S (Ref. 34); (2) combining single frequency C-V and I-V measurement for correction;[46] (3) dual frequency C-V measurement to obtain an averaged corrected capacitance value [Eq. (8)];[47] (4) combining dual frequency C-V and I-V measurements to obtain corrected capacitance;[48] and (5) dual frequency correction considering the series inductance, and series resistance[49]

$$C_c = \frac{f_1^2 C_{m1}\left(1+D_1^2\right) - f_2^2 C_{m2}\left(1+D_2^2\right)}{f_1^2 - f_2^2}. \tag{8}$$

However, frequency dispersion is still observed with the use of above methods. Of these methods, the dual frequency C-V correction technique[47–49] assumes that there is no frequency dispersion in dielectric constant of high-κ oxide, although the real high-κ oxides show small frequency dependence as observed in this study. In addition, the dual frequency technique[47] gives a kind of averaged resultant C-V curve which is obtained from two different measured C-V curves and this technique gives unacceptable value of corrected capacitance (of order 10^{-2}) when applied on C-F raw data for adjacent frequency values (e.g., 1, 1.9 or 1.9, 2.8 kHz, etc.). Therefore, a method is required which can accurately and easily provide the corrected capacitance from both C-V and C-F measurements. The electrical equivalent circuit for Pt/Er_2O_3 (FA)/Si/Pt MOS capacitor[34] is shown in Fig. 2. The measured impedance (Z_m) of the circuit shown in Fig. 2(c) is given by

$$Z_m = \frac{R_m - j\omega {R_m}^2 C_m}{1+\omega^2 {R_m}^2 {C_m}^2}. \tag{9}$$

The corrected impedance (Z_c) of the circuit shown in Fig. 2(b) is given by

$$Z_c = R_S + \frac{R_c - j\omega {R_c}^2 C_c}{1+\omega^2 {R_c}^2 {C_c}^2}. \tag{10}$$

Here, the values of R_m and C_m are obtained from a parameter analyzer, but C_c, R_c, and R_S are not known. Using Eqs. (9) and (10), three unknown parameters, C_c, R_c, and R_S, cannot be determined. Therefore, after equating real, imaginary parts of Eqs. (9) and (10) and after rigorous mathematical calculations, C_c and R_c are obtained as a function of R_m, C_m, and R_S, as follows:

$$C_c = \frac{\left(1+\omega^2 {R_m}^2 {C_m}^2\right) - \left(\omega^2 {R_m}^4 C_m^2\right)}{\left(R_m - \left(1+\omega^2 {R_m}^2 C_m^2\right) R_S\right)^2}, \tag{11}$$

$$R_c = \frac{\left(R_m - \left(1+\omega^2 {R_m}^2 C_m^2\right) R_S\right) {R_m}^2 C_m}{\left(1+\omega^2 {R_m}^2 {C_m}^2\right)^2 - \left(\omega^2 {R_m}^4 C_m^2\right)}. \tag{12}$$

Here, the value of R_S is not known. Although the work reported by Zhang *et al.*[48] and Lu *et al.*[46] assumed that the dc resistance ($R_{dc} = V_{dc}/I_{dc}$) calculated from I-V curve (Fig. 5) is equal to the sum of R_c and R_S, which gives an extra equation to compute the value of R_S, it needs to be pointed out that the values of R_c and R_S are extracted from the C-V curve, which is obtained using a small signal analysis with a small ac signal superimposed on a dc signal. But the I-V characteristics are obtained using purely dc analysis and the resistance obtained from the I-V curve must be related to the resistance at a very low frequency. From Fig. 5, the dc resistance at −2 V bias is ~10.58 MΩ and the value of R_c using Eq. (12), assuming $R_S = 0$, obtained from the C-F curve varies from ~61.2 kΩ to ~78.4 Ω with the variation in frequency from 1 kHz to 1 MHz, for Pt/Er_2O_3 (FA)/Si/Pt, MOS capacitors. Therefore, it is concluded that the parallel resistance component (R_c) increases with the decrease in frequency and the assumption $R_{dc} = R_c + R_S$ does not hold because R_c and R_S are functions of frequency and R_{dc} is nothing but the resistance at a very low frequency. In fact, from the equivalent circuit in Fig. 2(b), it is clear that at very low frequencies, C_c acts as an open circuit and the impedance of circuit [Fig. 2(b)] becomes $R_c + R_S$. Therefore, the assumption $R_{dc} = R_c + R_S$ holds only at very low frequencies.

Using Eq. (11), C_c is obtained as a function of frequency, provided R_S is known. However, the value of R_S is not determined up till now; therefore, two extreme boundary conditions are assumed, i.e., (1) when $R_S = 0$, then $C_c = C_m$ and $R_c = R_m$; (2) when $R_S = R_m/1+\omega^2 {R_m}^2 {C_m}^2$, $C_c = \infty$ and $R_c = 0$. The real value of R_S at any time t is $0 \le R_S \le (R_m/1 + \omega^2 {R_m}^2 {C_m}^2)$ and the impact of R_S on the corrected dielectric constant extracted from corrected capacitance C_c is shown in Fig. 6. It is evident from Fig. 6 that when $R_S = R_m/1+\omega^2 {R_m}^2 {C_m}^2$, the dielectric constant increases at higher

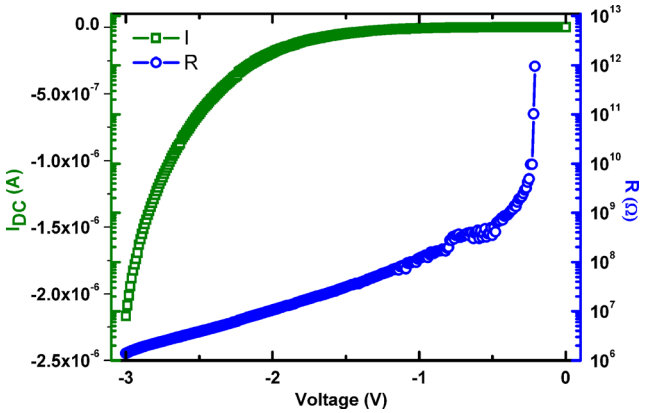

FIG. 5. (Color online) Leakage current (I-V) characteristics on the left axis, and differential resistance (V_{dc}/I_{dc}) on the right axis for Pt/Er_2O_3 (FA)/Si/Pt, MOS capacitors.

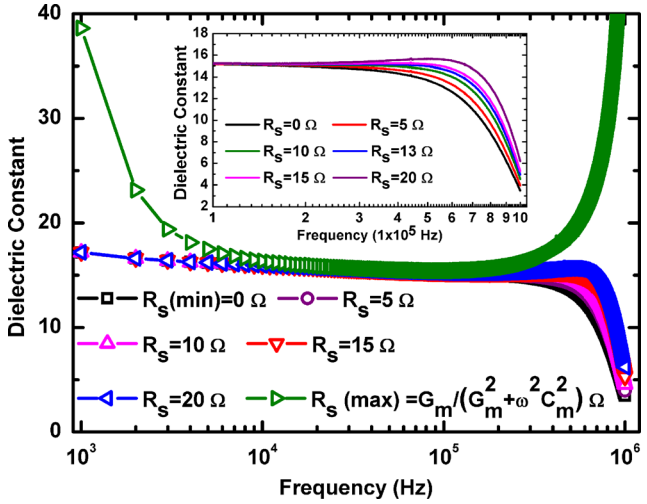

FIG. 6. (Color online) Impact of R_S on the corrected dielectric constant extracted from corrected capacitance (C_c) of Er_2O_3 MOS capacitors. The inset shows the approximation of R_s using C-F curves.

frequencies, which is not true. Although the dielectric constant follows the typical behavior for small values of R_S (0–13 Ω) as shown in the inset of Fig. 6, beyond 13 Ω the dielectric constant again increases at high frequencies. Hence, it is verified that the values of R_S is small with a minor impact on the value of dielectric constant and the frequency dispersion at ≤250 kHz is related to the dielectric relaxation in high-κ Er_2O_3, although the frequency dispersion above a certain critical frequency, i.e., ∼250 kHz, is attributed to the inability of the parameter analyzer to accurately measure the capacitance value and high dissipation factor (D). Therefore, for accurate estimation of the capacitance value, a data set must be chosen such that the dissipation factor is minimum. Similarly, guidelines are suggested earlier by Vogel *et al.*[45] to improve the accuracy of the corrected capacitance extraction method.

From the above discussions, it is revealed that ∼10 to ∼250 kHz is the desired frequency range for the estimation of corrected capacitance. Figure 7 shows the corrected C-V characteristics of Pt/Er_2O_3 (FA)/Si/Pt, MOS capacitors with variation in frequency using (a) dual frequency technique using Eq. (8), (b) at $R_S = R_{max}$ using Eq. (12), and (c) at a reasonable critical value of R_S = 13 Ω, beyond which the κ value increases with the increase in frequency. Here, it is observed that the dual frequency technique[47] gives an averaged value of two measured capacitance data set [Fig. 7(a)] with an assumption that intrinsic frequency dispersion in oxide material is negligible. But in real MOS devices, frequency dispersion is observed either due to the parasitic effects or the intrinsic property of the oxide material. When the dual frequency technique is applied on the current investigation of 1 MHz–100 kHz C-V curves, it gives the value of accumulation capacitance ∼10.4 nF corresponding to a dielectric constant value of ∼76 which is not acceptable. Similarly, when single frequency C-V measurement followed by correction with approximated R_S is used,[34] i.e., at $R_S = R_{max}$, strong upturn is observed in the accumulation region around the applied voltage of −3 V, as shown in Fig. 7(b). Also, this technique, when applied to C-F characteristics (Fig. 6), gives a value of κ which increases with the increase in frequency, especially at higher (250 kHz–1 MHz) and lower (≤10 kHz) frequencies. Here, the R_S value is obtained by assuming that the measured capacitance is equal to the series combination of oxide capacitance and series resistance.[34] However, in the proposed methodology, R_S is not obtained with this assumption, instead a boundary condition is imposed on R_S and the corresponding C-F curves are plotted for different values of R_S, and a critical value of R_S is extracted from the C-F characteristics in Fig. 6. Here, the critical value of R_S is defined as the value beyond which the κ value increases with increase in frequency and is extracted from C-F characteristics to be ∼13 Ω. Although it must be noted that when the dataset is chosen such that the dissipation factor is minimum, then both the dual frequency technique and the proposed R_S approximation technique using C-V and C-F curves gives accurate results. Nevertheless, the proposed methodology is also applicable on the C-F curves which proves it as a simple, efficient, and superior technique for capacitance correction, using simple C-V, C-F characteristics, and Eq. (11).

Up till now, the frequency dispersion in the accumulation region is systematically investigated, but still justification is required regarding the V_{fb} and V_{th} shifts with the variation in frequency observed in Fig. 1. Earlier, it is attributed that significant V_{fb} and V_{th} shift with the variation in frequency is due to the frequency dependent border traps located close to the Er_2O_3/Si interface that exchanges mobile charges with silicon.[33] The shift in the flatband voltage (ΔV_{fb}) is a serious

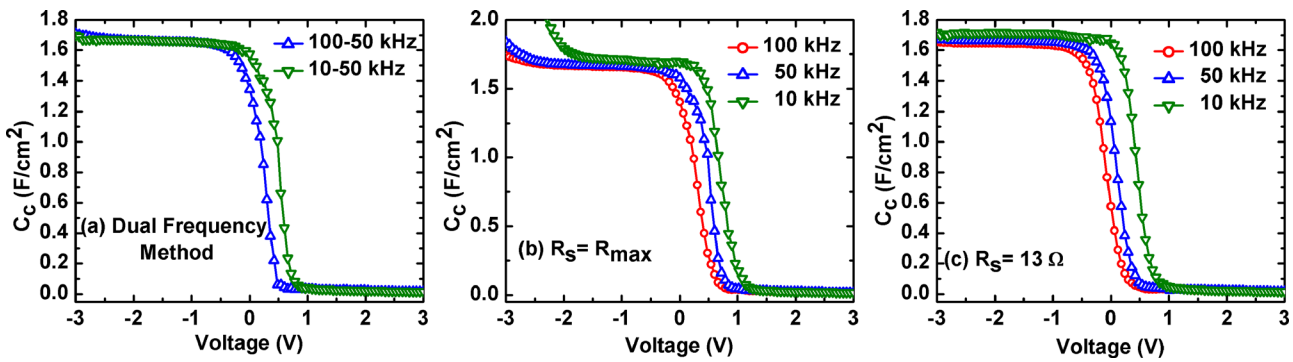

FIG. 7. (Color online) Corrected C-V characteristics of Pt/Er_2O_3 (FA)/Si/Pt, MOS capacitors with the variation in frequency using (a) dual frequency technique [Eq. (8)]; (b) at $R_S = R_{max}$, and (c) R_S =13 Ω using Eq. (12).

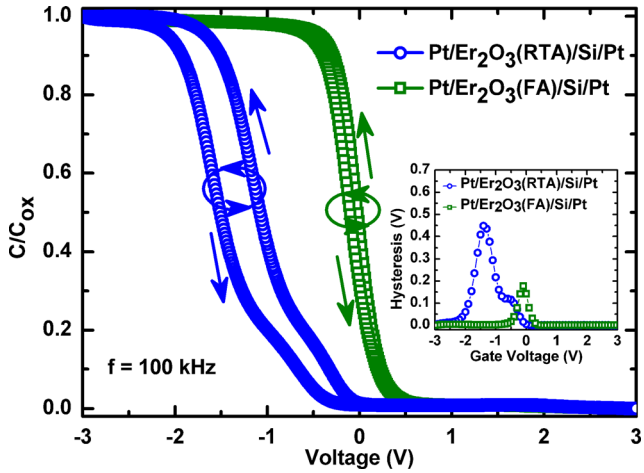

FIG. 8. (Color online) Normalized cyclic C-V characteristics of Pt/Er_2O_3 (RTA)/Si/Pt and Pt/Er_2O_3 (FA)/Si/Pt, MISM structures at 100 kHz. The inset shows the hysteresis extracted by subtracting the capacitance value obtained from the forward and reverse gate voltage sweeps for Pt/Er_2O_3 (RTA)/Si/Pt and Pt/Er_2O_3 (FA)/Si/Pt, MISM structures at 100 kHz.

issue for CMOS device application perspective with metal/high-κ gate stacks, which is due to border traps or slow states located near the oxide/Si interface.[10,33,50–52] The quantitative analysis of border traps is evaluated by the hysteresis obtained from the cyclic C-V curves in the dual mode. Here, hysteresis is defined by the flatband voltage shift (ΔV_{fb}) extracted from the forward (inversion to accumulation) and reverse (accumulation to inversion) gate voltage sweeps. Figure 8 shows the normalized cyclic C-V characteristics of Pt/Er_2O_3 (RTA)/Si/Pt and Pt/Er_2O_3 (FA)/Si/Pt, MISM structure at 100 kHz. The counter-clockwise hysteresis, extracted by subtracting the capacitance value obtained from forward and reverse gate voltage sweeps, is ~0.45 and ~0.18 V for Pt/Er_2O_3 (RTA)/Si/Pt and Pt/Er_2O_3 (FA)/Si/Pt, MISM structures at 100 kHz, respectively, and attributed to the frequency dependent slow border traps that respond at lower frequencies.[33] The high hysteresis (~0.45 V) for Pt/Er_2O_3 (RTA)/Si/Pt, MISM structure is attributed to a significant thickness of the lossy interfacial layer, where the deformation of highly covalent Si–O bonds results in a large driving force for oxygen movement in high-κ Er_2O_3 and a higher number of charge traps.[10] On the other hand, the astonishing low hysteresis (~0.18 V) for Pt/Er_2O_3 (FA)/Si/Pt, MISM structure is attributed to high-quality Er_2O_3 (FA)/Si interface and lower number of border traps.[53] Also, this exceptionally low hysteresis of ~0.18 V in Pt/Er_2O_3 (FA)/Si/Pt, MISM structure is much lower than the hysteresis reported for Al_2O_3 (~0.58 V), La_2O_3 (~0.32 V), HfO_2 (~0.29 V), and Y_2O_3 (~0.23 V) alternate high-κ dielectrics.[28,54] Therefore, Er_2O_3 is a potential alternate gate dielectric for next-generation IC technology. Moreover, the border state density (N_{bt}) in Er_2O_3 high-κ is estimated by the following relation, assuming interface states have minimal contribution to hysteresis:[50]

$$N_{bt} = \frac{C_{acc}\Delta V_{fb}}{qA}, \tag{13}$$

where C_{acc}, ΔV_{fb}, q, and A is the accumulation capacitance at 100 kHz, hysteresis, electronic charge, and top electrode area, respectively. The value of N_{bt} estimated for Pt/Er_2O_3 (RTA)/Si/Pt and Pt/Er_2O_3 (FA)/Si/Pt, MISM structure is ~3.35×10^{12} and ~1.84×10^{12} traps/cm^2, respectively. Further, to better explain the role of border traps in flatband voltage shifts of high-κ based MOS capacitors, a graphical/band model is proposed as shown in Fig. 9.

Figure 9(a) shows the schematic of metal/insulator/semiconductor (MIS) structure, showing the location of border

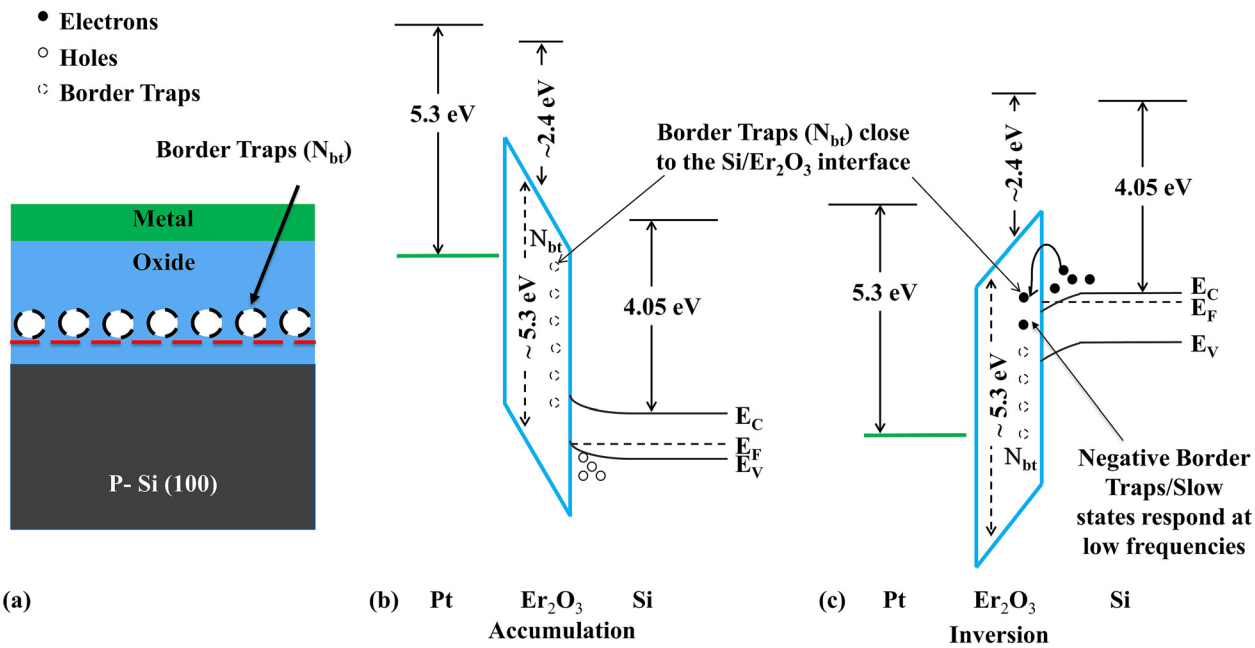

FIG. 9. (Color online) (a) Schematic showing the location of border traps/slow states in the MIS structure. The energy band diagram for the Pt/Er_2O_3/Si structure in (b) accumulation (−3 V) and (c) inversion (+3 V) regions.

traps close to the insulator/Si interface. The role of these border traps becomes significant for nanoscale devices with ultrathin insulator films.[50] Figures 9(b) and 9(c) show the energy band diagram of the Pt/Er_2O_3/Si, MIS structure, using the work function of Pt (~5.3 eV), Er_2O_3 electron affinity (~2.4 eV), and Er_2O_3 energy band gap (~5.3 eV).[55] In Fig. 9(b), when the gate voltage (V_g) = −3 V, the device is in the accumulation region, i.e., the surface below the insulator/Si interface is occupied by holes. In Fig. 9(c), when $V_g = +3$ V, the device is in the inversion region, i.e., the surface below the insulator/Si interface is now inverted and occupied by electrons. At lower frequencies, when the voltage is swept from accumulation to inversion, the negative border traps respond to the applied voltage frequency excitation and attracts few holes to the silicon surface; therefore, higher voltage is now required to create the inversion region. Hence, at lower frequencies, there is a right shift of V_{fb}, V_{th}, and C-V curves (Fig. 1) due to the negative border traps (Fig. 9).

IV. CONCLUSIONS

In summary, the cause of frequency dispersion in postdeposition RTA and FA treated Er_2O_3 MOS capacitors is systematically investigated. The extrinsic causes, i.e., parasitic, lossy interfacial layer, surface roughness, polysilicon depletion, quantum confinement, and oxide tunneling effects are considered before proceeding to the intrinsic cause of frequency dispersion in high-κ Er_2O_3 (FA), whereas significant thickness of the lossy interfacial layer in Er_2O_3 (RTA) is attributed as a cause of reduced dielectric constant of the gate oxide. The cause of frequency dispersion in Er_2O_3 MOS capacitors is attributed to the dielectric relaxation which is an intrinsic cause of frequency dispersion in high-κ Er_2O_3. Further, the HN law is used to model the frequency dispersion (up to 250 kHz) at fitting parameters $\alpha = \sim 0.87$, $\beta = \sim 0.44$, and $\tau = \sim 3 \times 10^{-7}$ s for the FA treated Er_2O_3 and $\alpha = \sim 0.4$, $\beta = \sim 0.96$, and $\tau = \sim 6.19 \times 10^{-7}$ s for the RTA treated Er_2O_3. The sharp decrease in the κ value at 1 MHz is attributed as the reason for the decrease in accumulation capacitance at high frequency. Moreover, it is suggested that the instrumental error/dissipation factor must be minimum for the MISM structure with nanometer scale oxides/insulators for accurate capacitance value. A modified simple and efficient single frequency R_S approximation technique using C-V and C-F characteristics is proposed to obtain the corrected capacitance value. Additionally, the frequency dependent border traps are estimated for Pt/Er_2O_3 (RTA)/Si/Pt (~3.35×10^{12} traps/cm^2) and Pt/Er_2O_3 (FA)/Si/Pt (~1.84×10^{12} traps/cm^2), MISM structures. Hence, the frequency dispersion in Er_2O_3 MOS capacitors flatband voltage and accumulation capacitance is attributed to the frequency dependent slow states/border traps and dielectric relaxation in Er_2O_3, respectively. Therefore, the FA treated Er_2O_3 high-κ dielectric (κ ~16), low frequency dispersion (~9%) up to 250 kHz, and minimal hysteresis (~0.18 V) is promising for next generation CMOS device applications. In future, the frequency dispersion is Er_2O_3 is needed to be demonstrated using special high frequency layouts to prove its potential application in gigahertz RF devices as well.

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[1]International Technology Roadmap for Semiconductors (ITRS) (2013), available at http://www. itrs2.net/2013-itrs.html.
[2]G. He, L. Zhu, Z. Sun, Q. Wan, and L. Zhang, Prog. Mater. Sci. **56**, 475 (2011).
[3]J. Robertson, Eur. Phys. J. Appl. Phys. **28**, 265 (2004).
[4]E. R. Hsieh, Y. D. Wang, S. S. Chung, J. C. Ke, C. W. Yang, and, and S. Hsu, *IEEE Symposium on VLSI Technology*, Honolulu (2016), pp. 1–2.
[5]T. Nabatame, M. Kimura, H. Yamada, A. Ohi, T. Ohishi, and T. Chikyow, Thin Solid Films **520**, 3387 (2012).
[6]C. Zhao, C. Z. Zhao, S. Taylor, and P. R. Chalker, Materials **7**, 5117 (2014).
[7]M. H. Kryder and C. S. Kim, IEEE Trans. Magn. **45**, 3406 (2009).
[8]D. K. Sharma, R. Khosla, and S. K. Sharma, Solid State Electron. **111**, 42 (2015).
[9]R. Khosla, D. K. Sharma, K. Mondal, and S. K. Sharma, Appl. Phys. Lett. **105**, 152907 (2014).
[10]K. Kita and A. Toriumi, Appl. Phys. Lett. **94**, 132902 (2009).
[11]V. Mikhelashvili, G. Eisenstein, F. Edelman, R. Brener, N. Zakharov, and P. Werner, J. Appl. Phys. **95**, 613 (2004).
[12]N. R. Aghamalyan, R. K. Hovsepyan, E. A. Kafadaryan, R. B. Kostanyan, S. I. Petrosyan, G. H. Shirinyan, A. K. Abduev, and A. S. Asvarov, J. Contemp. Phys. **47**, 236 (2012).
[13]M. Miritello, R. Lo Savio, A. M. Piro, G. Franzò, F. Priolo, F. Iacona, and C. Bongiorno, J. Appl. Phys. **100**, 13502 (2006).
[14]F.-H. Chen, J.-L. Her, Y.-H. Shao, Y. H. Matsuda, and T.-M. Pan, Nanoscale Res. Lett. **8**, 18 (2013).
[15]X. Wang, Y. L. Zhu, M. He, H. B. Lu, and X. L. Ma, Acta Mater. **59**, 1644 (2011).
[16]M. P. Singh, C. S. Thakur, K. Shalini, N. Bhat, and S. A. Shivashankar, Appl. Phys. Lett. **83**, 2889 (2003).
[17]R. Xu, Q. Tao, Y. Yang, and C. G. Takoudis, Appl. Surf. Sci. **258**, 8514 (2012).
[18]R. Khosla, P. Kumar, and S. K. Sharma, IEEE Trans. Device Mater. Reliab. **15**, 610 (2015).
[19]P. Kumar, R. Khosla, and S. K. Sharma, Surf. Interfaces **4**, 69 (2016).
[20]E. K. Liu, B. S. Zhu, and J. S. Luo, *Semiconductor Physics*, 4th ed. (National Defence Industry, Beijing, 1999).
[21]C. C. Zhao, C. C. Zhao, M. Werner, S. Taylor, and P. Chalker, Nanoscale Res. Lett. **8**, 456 (2013).
[22]B. Ricco, P. Olivo, T. N. Nguyen, T. S. Kuan, and G. Ferriani, IEEE Trans. Electron Devices **35**, 432 (1988).
[23]L. M. Terman, Solid State Electron. **5**, 285 (1962).
[24]S. W. Lee, IEEE Trans. Electron Devices **41**, 403 (1994).
[25]C. L. Huang, J. V. Faricelli, and N. D. Arora, IEEE Trans. Electron Devices **40**, 1134 (1993).
[26]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (Wiley, New York, 2007).
[27]C. Z. Zhao, S. Taylor, M. Werner, P. R. Chalker, R. T. Murray, J. M. Gaskell, and A. C. Jones, J. Appl. Phys. **105**, 044102 (2009).
[28]C. Z. Zhao, S. Taylor, M. Werner, P. R. Chalker, J. M. Gaskell, and A. C. Jones, J. Vac. Sci. Technol., B **27**, 333 (2009).
[29]C. Z. Zhao, M. Werner, S. Taylor, P. R. Chalker, A. C. Jones, and C. Zhao, Nanoscale Res. Lett. **6**, 48 (2010).
[30]J. Tao, C. Z. Zhao, C. Zhao, P. Taechakumput, M. Werner, S. Taylor, and P. R. Chalker, Materials **5**, 1005 (2012).
[31]C. Z. C. Zhao, C. Z. C. Zhao, M. Werner, S. Taylor, P. Chalker, and P. King, Nanoscale Res. Lett. **8**, 172 (2013).
[32]T. Huang, K. M. Wong, M. Li, X. Zhu, and K. M. Lau, Phys. Status Solidi C **9**, 919 (2012).

[33]D. M. Fleetwood, IEEE Trans. Nucl. Sci. **43**, 779 (1996).
[34]E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 2003).
[35]W. H. Wu *et al*., IEEE Electron Device Lett. **27**, 399 (2006).
[36]E. J. Lerner, IBM J. Res. Dev. **4**, 6 (1999).
[37]K. Ahmed, E. Ibok, G. C. F. Yeap, Q. Xiang, B. Ogle, J. J. Wortman, and J. R. Hauser, IEEE Trans. Electron Devices **46**, 1650 (1999).
[38]C.-H. Choi *et al*., IEEE Electron Device Lett. **20**, 292 (1999).
[39]N. M. Murari, R. Thomas, S. P. Pavunny, J. R. Calzada, and R. S. Katiyar, Appl. Phys. Lett. **94**, 142907 (2009).
[40]W. K. Henson, K. Z. Ahmed, E. M. Vogel, J. R. Hauser, J. J. Wortman, R. D. Venables, M. Xu, and D. Venables, IEEE Electron Device Lett. **20**, 179 (1999).
[41]C. T. Dervos, E. Thirios, J. Novacovich, P. Vassiliou, and P. Skafidas, Mater. Lett. **58**, 1502 (2004).
[42]H. Choosuwan, R. Guo, A. S. Bhalla, and U. Balachandran, J. Appl. Phys. **93**, 2876 (2003).
[43]B. Lee, T. Moon, T. Kim, D. Choi, B. Park, B. Lee, T. Moon, and T. Kim, Appl. Phys. Lett. **87**, 12901 (2005).
[44]Y. Kim, J. Oh, T. G. Kim, and B. Park, Appl. Phys. Lett. **78**, 2363 (2001).
[45]E. M. Vogel, W. K. Henson, C. A. Richter, J. S. Suehle, S. Member, H. Kirklen, C. A. Richter, and J. S. Suehle, IEEE Trans. Electron Devices **47**, 601 (2000).
[46]Y. Lu *et al*., J. Vac. Sci. Technol., B **27**, 352 (2009).
[47]K. J. Yang and C. Hu, IEEE Trans. Electron Devices **46**, 1500 (1999).
[48]X. Zhang, C. Cheng, H. Zhu, T. Yu, D. Zhang, and B. Chen, IEEE Electron Device Lett. **37**, 1328 (2016).
[49]H. T. Lue, C. Y. Liu, and T. Y. Tseng, IEEE Electron Device Lett. **23**, 553 (2002).
[50]E. Verrelli, G. Galanopoulos, I. Zouboulis, and D. Tsoukalas, Thin Solid Films **518**, 5579 (2010).
[51]T. M. Briere, A. S. Beddar, and M. T. Gillin, Med. Phys. **32**, 3346 (2005).
[52]S. Zeyrek, A. Turan, and M. M. Bülbül, Chin. Phys. Lett. **30**, 77306 (2013).
[53]K. Iwamoto *et al*., Appl. Phys. Lett. **92**, 132907 (2008).
[54]D. W. Davidson and R. H. Cole, J. Chem. Phys. **19**, 1484 (1951).
[55]S. Z. Li, C. L. Gan, H. Cai, C. L. Yuan, J. Guo, P. S. Lee, and J. Ma, Appl. Phys. Lett. **90**, 263106 (2007).