Applied Physics Letters

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Cite as: Appl. Phys. Lett. **112**, 252102 (2018); https://doi.org/10.1063/1.5030020
Submitted: 18 March 2018 . Accepted: 02 June 2018 . Published Online: 18 June 2018

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Integration of graphene oxide buffer layer/graphene floating gate for wide memory window in Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au non-volatile (FLASH) applications

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(Received 18 March 2018; accepted 2 June 2018; published online 18 June 2018)

The excellent electronic properties of graphene such as high density of states, work-function, and low dimensionality promote the usage of graphene as an efficient floating gate (FG) layer for downscaled, high density non-volatile flash memories (NVFMs). However, the chemical inertness of graphene requires a buffer layer for the uniform deposition of a high-k blocking layer (high-k blocking oxide/buffer layer/graphene/SiO_2/p-Si/Au). Herein, FG-NVFM devices are fabricated using few-layer graphene as a FG followed by deposition of spin-coated monolayer graphene oxide (GO) as a buffer layer. The simple, stress free deposition of GO decorated with the functional groups is anticipated for the uniform deposition of blocking oxide (Aluminum oxide, Al_2O_3) over GO/graphene/SiO_2/p-Si/Au. Beyond this, it improves the interface (Al_2O_3/GO/graphene), leading to enhanced memory characteristics for the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM structure. The electrical characterizations of the fabricated FG-NVFM devices show a significantly wide memory window of ~4.3 V @ ±7 V at 1 MHz and robust retention up to $\sim 2 \times 10^{13}$ s (>15 years). These observations clearly reveal an efficient potential of graphene for FG and GO as a buffer layer for the future NVFM device applications. *Published by AIP Publishing*. https://doi.org/10.1063/1.5030020

Floating Gate non-volatile flash memory (FG-NVFM) is the most commonly used storage technology in the majority of consumer electronics.[1–5] In this regard, for high-density data storage, further downscaling of poly-silicon based FG is a challenge, owing to its inherent physical issues leading to ballistic transport of carriers, impact ionization in the blocking dielectric, and device reliability.[2,5,6] An important figure of merit for NVFM is large memory window (δW) and long term data retention with low operating voltages.[5] As per the industry standards, for reliable memory functionality, a δW of ~1.5 V and data retention of ~>10 years (before the NVFM losses ~50% of the stored charge) are essential.[5,7] Therefore, to overcome the challenges faced with poly-silicon FG and to meet the benchmarks of NVFM, ultra-thin metal (~1 nm) was demonstrated as an alternate FG in NVFM.[8] But the use of metal FG imposes its own fundamental issues like diffusion/agglomeration into the dielectrics (tunnel and blocking), resulting in increased leakage current.[1,2,6,9]

Driven by this, graphene (monolayer thickness ~0.3 nm) has attracted attention of the scientific community, as an alternate scaled FG layer for NVFM applications.[2,5–7,10] The interest in graphene is owing to its intrinsic properties such as high density of states (DOS), high work function ($\Phi_{graphene}$), and excellent thermal and chemical stability.[2,5–7,10] Specifically, for NVFM involving graphene as a FG, graphene sandwiched between the two dielectrics (tunnelling and blocking) forms a potential well owing to the high $\Phi_{graphene}$.[5] Hence, it results in the large δW and long-term data retention.[2,5–7,10] In fact, $\Phi_{graphene}$ varies with the number of layers owing to its interlayer screening, more pronounced for multilayer (≥3 layer) graphene, and tends to saturate beyond six layers.[5,6,11–15] Therefore, an accurate control over the number of graphene layers over a large area is desirable for electronic device applications and is a challenge.[5,6] Several reports on the graphene growth by mechanical and chemical exfoliation and epitaxial growth on SiC by chemical vapor deposition (CVD) are described in the past.[16] However, for electronic device applications, CVD has emerged as an imperative method for the large area defect-free graphene growth along with an efficient control over the number of layers.[17]

Furthermore, for nano-electronic device applications, the interface of graphene with the high-k blocking dielectric is extremely important.[4,7] The chemical inertness and non-availability of dangling bonds on the graphene surface lead to interface reliability for high-k/graphene based nano-scaled devices.[5,18] However, few research groups have reported low-temperature atomic layer deposition (ALD) of dielectrics over graphene; unfortunately, the deposition leads to negative effects, such as generation of additional defect sites in the graphene, and degrades the device performance.[18] Therefore, in order to obtain a reliable interface between the dielectric and graphene, deposition of the metal/polymer buffer layer over graphene was reported in the past.[18] Hong *et al.*[5] demonstrated graphene-NVFM, utilizing an aluminum (~1.1 nm) layer deposited over graphene and oxidized in air, to serve as a buffer layer for ALD of Al_2O_3 (~35 nm). As already discussed and established, the metal layer leads to increased leakage current in the fabricated devices[2,6,9] and degrades the graphene electronic and intrinsic properties.[18] On the other hand, deposition of the polymeric buffer layer through the spin coating is found to be a cost effective and

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efficient route and does not hamper the intrinsic properties of graphene FG.[18]

The present work demonstrates the stress-free deposition of the graphene oxide (GO) buffer layer (via spin-coating) over CVD grown few (∼3–4) layer graphene (GO/graphene/SiO_2/p-Si/Au). The intention for the use of the monolayer GO buffer layer is (i) utilization of functional groups for the pin hole free deposition of the blocking layer and (ii) low dimensionality and controlled deposition.[7,19,20] However, the few layer graphene with high $\Phi_{graphene}$, DOS, reduced conductivity in the c-axis, and low dimensionality favors its use as a FG in NVFM applications.[2,5–7,10] Additionally, ultrathin SiO_2 serves as a tunneling layer, while the high-k, Al_2O_3 is used as a blocking layer in the present study.[2,6]

In order to investigate the electrical characteristics of few-layer CVD graphene FG based NVFM, a set of devices were fabricated as per the process flow shown in Figs. 1(a)–1(i). First, 2-in. p-Si wafers (1–10 Ω cm) with ⟨100⟩ orientation were cleaned using the standard RCA cleaning procedure [Fig. 1(a)]. Second, for ultrathin, high-quality SiO_2 tunnel oxide growth, the cleaned p-Si wafers were loaded to Rapid Thermal Oxidation (AS-One) at 25 °C under N_2 flow (∼800 sccm). Afterwards, the temperature was raised to 900 °C (ramp up ∼25 °C/s), and for SiO_2 growth, an oxygen flow of ∼800 sccm at 900 °C for 90 s was maintained. Finally, the temperature was ramped down from 900 °C to 25 °C at a rate of ∼3 °C/s under a N_2 flow of ∼800 sccm [Fig. 1(b)].[7] In the third step, the SiO_2/p-Si/SiO_2 wafers were subjected to backside buffer oxide etch [Fig. 1(c)] and then the back metallization was performed (Au, ∼100 nm) using an e-beam evaporator (TECHPORT) to result into SiO_2/p-Si/Au [Fig. 1(d)] in the fourth step. For few-layer CVD graphene, cleaned Cu foils (∼25 μm thick) were loaded to the tube furnace at ∼25 °C and subsequently purged with Ar (∼100 sccm) for 20 min. Thereafter, the temperature of the furnace was ramped up (∼30 °C/min) to ∼980 °C under a H_2:Ar flow of ∼100:10 sccm at a pressure of ∼7 mbar and annealed for next 60 min. For graphene growth, at ∼980 °C, a mixture of CH_4:H_2:Ar 10:100:10 was injected into the furnace for 30 min at a pressure of ∼8.5 mbar. As a next step, cooling was performed at a rate of ∼20 °C/min under a H_2 flow of ∼100 sccm up to ∼600 °C and an Ar flow of ∼20 sccm till ∼40 °C [Fig. 1(j)]. For the transfer of graphene sheets over SiO_2/p-Si/Au, the PMMA (950 A1) thin film was spin-coated over graphene/Cu foils at 1000 rpm for 60 s and was kept on a hot plate at 100 °C for 5 min.[21] Here, PMMA protects the graphene layer and acts as a rigid support during the transfer process.[22] While, for Cu etching, the PMMA/graphene/Cu structure was kept in ammonium persulphate solution (0.1 M) for ∼4 h and was rinsed with DI water. After Cu etching, in the fifth step, the PMMA/graphene layer was gently scooped over the SiO_2/p-Si/Au substrates, and thereafter, PMMA was removed using the acetone bath [Fig. 1(e)].[22,23] As discussed previously, the residues of metal over the transferred graphene degrade the device performance.[2,5,6,9,24,25] Conversely, the presence of undesirable PMMA residue over the transferred graphene may also increase the surface roughness and thereby degrade the interface, leading to non-uniform deposition of the blocking oxide and resulting in lower memory window, increased gate leakage current, and reduced reliability of the fabricated FG-NVFM.[2,5,6,9,22,26–29] Therefore, μ-Raman spectroscopy measurements were performed to ensure the quality of the transferred few-layer graphene on SiO_2/p-Si/Au substrates.[5] The μ-Raman spectra show very low intensity "D" (∼1350 cm^{-1}) band peak "I_D" as compared to the "G" (∼1580 cm^{-1}) band peak "I_G" and result in I_D/I_G ∼ 0.08 and 0.1 for graphene/Cu and graphene/SiO_2/p-Si/Au, whereas "2D" (∼2700 cm^{-1}) band peak "I_{2D}" with respect to the "I_G" results in the I_{2D}/I_G ∼1.1 [Fig. 1(k)] for both graphene/Cu and graphene/SiO_2/p-Si/Au. These outcomes clearly demonstrate the presence of few (3–4) layers of graphene, and a very low intensity "D" band peak in Raman spectra signifies a defect free graphene growth and transfer, as reported in the past.[5,30] The defect free graphene used in the present work refers to the absence of undesirable defects and residues of metals or polymers over the transferred graphene.[22,27–29,31] After that, in the sixth step, the GO synthesized using the modified Hummers method,[19] at a concentration of 1 mg/ml in DI water, was spin-coated over the graphene/SiO_2/p-Si/Au substrates at 1000 rpm for 2 min and dried at 50 °C for 5 min [Fig. 1(f)]. The μ-Raman spectroscopy [Fig. 1(k)] was performed to confirm the presence of GO/graphene stack and GO over the desired substrates. Here, the Raman signature peaks of GO

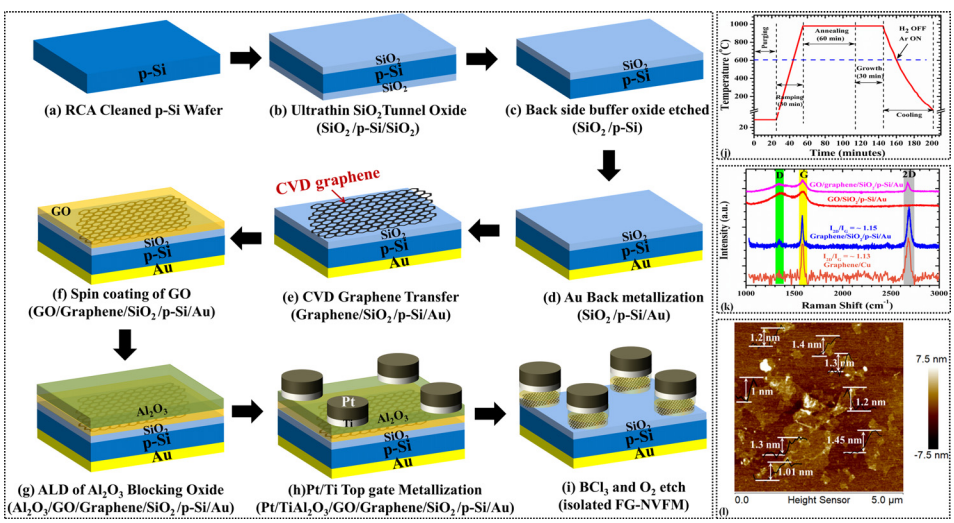

FIG. 1. (a)–(i) Schematic process flow for the fabrication of CVD graphene based Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM structure, (j) time line for the CVD graphene growth on Cu, (k) Raman Spectra for graphene/Cu, graphene/SiO_2/p-Si/Au, GO/SiO_2/p-Si/Au, and GO/graphene/SiO_2/p-Si/Au, and (l) AFM height profile analysis of GO sheets for a scan area of 5×5 μm^2.

and graphene are in line with the previous reports.[16,21] The tapping mode atomic force microscopy (AFM) measurement for a scan area of $5 \times 5\ \mu m^2$ [shown in Fig. 1(l)] clearly depicts that the GO sheets are distributed all over the sample surface, and the height profile analysis on the individual GO sheets confirms the thickness of ~1 nm, consistent with the GO monolayer thickness reported in the literature.[32,33] To double check the thickness of GO used in the present work, an alternate imaging spectroscopic ellipsometry based mapping technique with variable wavelength (λ, 400–800 nm) using a Nanofilm EP4 (Accurion system) over a region of $\sim 400 \times 400\ \mu m^2$ was used.[34–36] Herein, for the calculation of optical constants and thickness mapping of GO sheets, a Cauchy model was used which confirmed the presence of monolayer (~1 nm) GO and validated the AFM results.[34–36] Afterwards, as a seventh step, Al_2O_3 was deposited over GO/graphene/SiO_2/p-Si/Au using trimethylaluminum and water as precursors at ~200 °C through ALD (BENEQ 300) [Fig. 1(g)]. For top gate electrode formation, Ti/Pt (10 nm/90 nm) was sputtered over the Al_2O_3/GO/graphene/SiO_2/p-Si/Au and patterned by standard lithography techniques [Fig. 1(h)]. The circular top gate electrode diameter was ~80 μm. To isolate each FG-NVFM device, the undesirable Al_2O_3 and GO/graphene layers (present outside the device region) were removed using BCl_3 plasma ~15 s and O_2 plasma ~2 min, respectively [using Oxford Plasma Lab, Fig. 1(i)]. In addition, from each of the aforesaid device fabrication steps, reference samples were held in reserve for further electrical, chemical, and physical characterizations, optimization of various parameters, and fabrication of control samples. The thickness of the ultrathin SiO_2 and Al_2O_3 films (measured using a J. A. Woolman Imaging Ellipsometer) was found to be $\sim 5 \pm 0.1$ nm and $\sim 15 \pm 0.2$ nm, respectively. Electrical characterization and charge storage capability of the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM structures and control samples (Pt/Ti/Al_2O_3/GO/SiO_2/p-Si/Au, Pt/Ti/Al_2O_3/graphene/ SiO_2/p-Si/Au, Pt/Ti/Al_2O_3/SiO_2/p-Si/Au, and Pt/Ti/SiO_2/p-Si/Au) were systematically characterized by Capacitance-Gate Voltage (C-V), Gate leakage current density-Gate Voltage (|J|-V), and Capacitance-Time (C-T) measurements using a Keithley 4200 SCS attached to a cascade probe station.

Figure 2 shows the cyclic C-V measurements for the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM devices and their control samples as a function of different sweep voltages: ±3 V, ±5 V, and ±7 V at 1 MHz. While performing the cyclic C-V measurements, the gate voltage swept from inversion (V_{g+}) to accumulation (V_{g-}) (forward sweep) and accumulation (V_{g-}) to inversion (V_{g+}) (reverse sweep). As depicted from the C-V curves, compared to control samples, the Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au shows a significant flat band shift between forward and reverse sweeps, also termed as δW. The observed δW for the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM [Fig. 2(a)] is around 1.87 V @ ±3 V (marked as "A"), 3.38 V @ ±5 V (marked as "B"), and 4.38 V @ ±7 V (marked as "C"). Also, the cyclic C-V measurements show remarkable characteristics favourable for memory devices such as (i) clockwise hysteresis centred ~0 V, indicating the low voltage operation of the fabricated NVFM with considerable high/low capacitance states and (ii) fast switching of capacitance during forward and reverse sweeps. The obtained large δW under low sweep voltages is sufficient for reliable data storage, thus confirming the ability of few-layer graphene as a potential FG layer in NVFM.

Furthermore, an additional hump at the mid depletion in the cyclic C-V for Pt/Ti/Al_2O_3/graphene/SiO_2/Si/Au [Fig. 2(c)] during forward and reverse sweeps is noticed. Whereas, for Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM as shown in Fig. 2(a), this hump in the mid depletion region vanishes. It clearly perceived that there is an existence of electrically active traps at the interface of Al_2O_3/graphene and responded at −2 to −3 V for the Pt/Ti/Al_2O_3/graphene/SiO_2/p-Si/Au structure. However, once these electrically active traps at the Al_2O_3/graphene interface are filled, due to fermi level pinning they become electrically inactive, which is evidently revealed from C-V characteristics of the Pt/Ti/Al_2O_3/graphene/SiO_2/p-Si/Au structure [Fig. 2(c)] from −3 to −5 V gate voltage sweep. Therefore, to enhance the reliability and long term retention of fabricated FG-NVFM, in the present work, an additional mono-layer of GO is deposited between Al_2O_3 and graphene, which facilitates the high quality and uniform deposition of Al_2O_3 for the Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au structure with an improved interface as clearly depicted in Fig. 2(a).

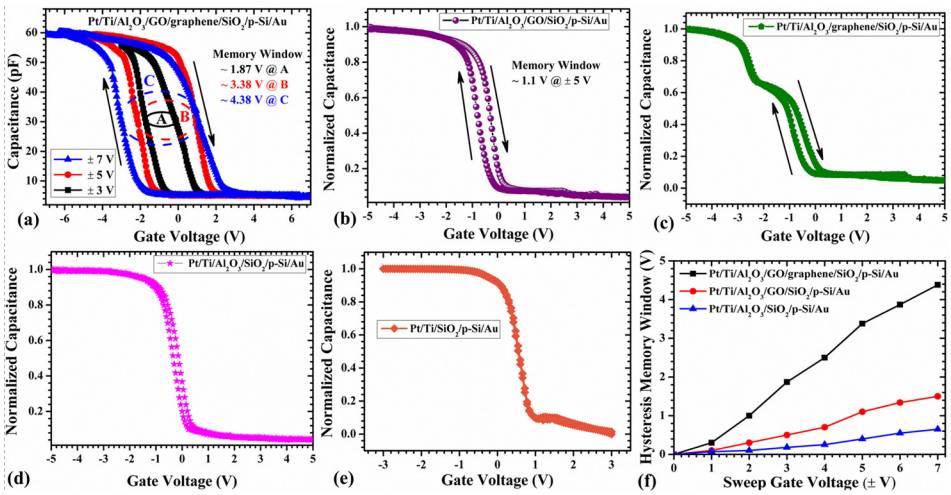

FIG. 2. Cyclic Capacitance-Gate Voltage measurements at 1 MHz for (a) Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM under different sweep voltages; Control Samples (b) Pt/Ti/Al_2O_3/GO/SiO_2/p-Si/Au, (c) Pt/Ti/Al_2O_3/graphene/SiO_2/p-Si/Au, (d) Pt/Ti/Al_2O_3/SiO_2/p-Si/Au, (e) Pt/Ti/SiO_2/p-Si/Au, and (f) Summary of the obtained memory window with respect to various fabricated device structures.

Table I summarizes and presents a comparison of the present work with the previously reported NVFM with CNT, graphene, GO, rGO, and NrGO as FG layers. Additionally, the total number of charge carriers stored per unit area ($N_{graphene}$) in the FG can be calculated from the following relation:[1,2,5,6,10]

$$N_{graphene} = \frac{\delta W \times C_{Al_2O_3}}{q}, \quad (1)$$

where $C_{Al_2O_3} = \frac{\varepsilon_0 \times \varepsilon_{Al_2O_3}}{t_{Al_2O_3}}$, with ε_0 being the permittivity of the free space, and ε_{Al2O3} and t_{Al2O3} the relative permittivity and measured thickness of ALD Al_2O_3, respectively, along with q being the electronic charge. Therefore, based on Eq. (1), the computed $N_{graphene}$ at ± 7 V is $\sim 2 \times 10^{13}$ cm^{-2} and is found comparable to the reported DOS for few-layer graphene ($\sim 4.4 \times 10^{13}$ cm^{-2}eV^{-1}).[1,2,5,6]

For the real world applications, the retention (C-T) characteristics of the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM were investigated. The retention in NVFM refers to the potential lifetime of the data stored without electrical refreshing. As shown in Fig. 3, the C-T analysis of the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM with a write pulse of ± 7 V was applied for 0.1 s with a read voltage of ~ -1 V, which is close to the flat band voltage.[7] Based on the voltage of the write applied pulse, the C-T characteristics result in high (C_{HIGH} @ -7 V) and low (C_{LOW} @ $+7$ V) capacitance states, while the average (50%) of the two capacitance states is the mid capacitance $C_{MID} = (C_{HIGH} + C_{LOW})/2$. The C-T characteristics for the fabricated FG-NVFM can be divided into two regions. In the first region for $\sim 10^2$ s, where an exponential decay in C_{HIGH} and exponential rise for C_{LOW} are noticed, attributing to narrowing δW. In the second region, beyond $\sim 10^3$ s, the C_{HIGH} and C_{LOW} states saturate and seem parallel to each other, dictating excellent long-term charge retention characteristics. On further extrapolation of the C-T characteristics ($>10^4$ s), the C_{HIGH} and C_{LOW} remain distinguishable for $\sim 10^{13}$ s, ahead of time the C_{LOW} coincides with C_{MID} at $\sim 2 \times 10^{13}$ s. Hence, the retention of the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM is approximately >15 years. The observed retention in the fabricated FG-NVFM is considerably higher than the reported retention value in the literature for CNT, GO, rGO, and NrGO-based FG-NVFM.[2,5–7,32,37] Therefore, the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM structure is suitable for next generation NVFM applications operating at low voltages.

TABLE I. Comparison and Summary of the FG-NVFM.

FLASH memory structure	δW ($\sim$in V) @ gate voltage (in V)	Retention (in s)	References
TaN/Al_2O_3 ($\sim$22 nm)/Multi-layer rGO ($\sim$1.5 nm)/SiO_2 ($\sim$8 nm)/p-Si	3 @ $\pm$14 5.8 @ $\pm$16 8 @ $\pm$18 9.4 @ $\pm$20	…	2
Au/Al/Ti/Al_2O_3 ($\sim$35 nm)/graphene ($\sim$0.3 nm)/SiO_2 ($\sim$5 nm)/p-Si	2@$\pm$7	$\sim 10^8$	5
Au/Al/Ti/Al_2O_3 ($\sim$35 nm)/graphene ($\sim$1.5 nm)/SiO_2 ($\sim$8 nm)/p-Si	6@$\pm$7		
Al/PMMA ($\sim$50 nm)/NrGO ($\sim$1.5 nm)/SiO_2 ($\sim$5 nm)/p-Si	1.8 @ $\pm$3 2 @ +3 to -5 3.3 @ $\pm$7	$\sim 10^5$	7
TaN/Al_2O_3 ($\sim$15 nm)/Multi-layer rGO ($\sim$1.5 nm)/SiO_2 ($\sim$8 nm)/p-Si	1.5 @ $\pm$8 2.6 @ $\pm$10 4.2 @ $\pm$14 6.8 @ $\pm$18	…	6
TaN/Al_2O_3 ($\sim$15 nm)/GO ($\sim$1 nm)/SiO_2 ($\sim$5 nm)/p-Si	2.3 @ 5 to 8 7.5 @ -5 to 14	…	32
TaN/Al_2O_3 ($\sim$15 nm)/rGO/SiO_2 ($\sim$8 nm)/p-Si	1.4 @ $\pm$4		
Pt/HfAlO/CNT/HfAlO/p-Si	0.4 @ $\pm$3	$\sim 10^4$	37
Pt/Ti/Al_2O_3 ($\sim$15 nm)/GO ($\sim$1 nm)/graphene ($\sim$1.5 nm)/SiO_2 ($\sim$5 nm)/p-Si/Au	1.87 @ $\pm$3 3.38 @ $\pm$5 4.38 @ $\pm$7	$\sim 2 \times 10^{13}$	This work

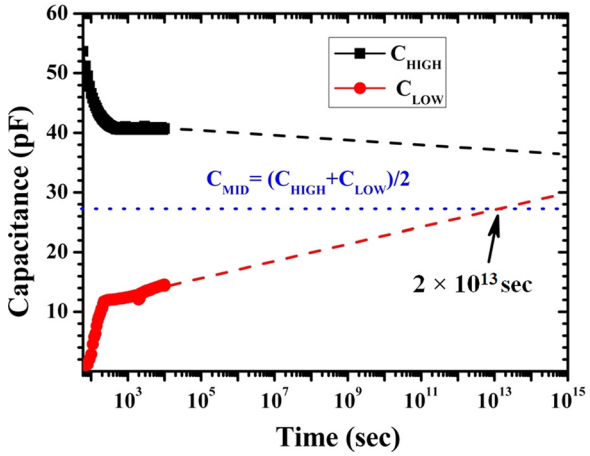

FIG. 3. Data Retention (C-T) characteristics for the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM.

The gate leakage current density ($|J|$) as a function of gate voltage (V) characteristic for the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM structure is shown in Fig. 4. The measured $|J|$ of $\sim 4 \times 10^{-5}$ A/cm^2 @ -10 V for the fabricated NVFM structure is comparable with the reported literature.[5] On the other hand, the significantly higher δW ($\sim$4.38 V) and minimal leakage current density ($\sim 5 \times 10^{-7}$ A/cm^2 @ -1 V) are indications of the

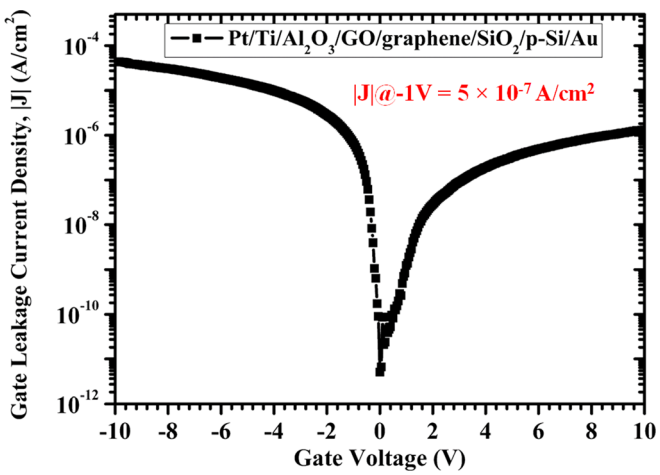

FIG. 4. Leakage Current Density-Gate Voltage ($|J|$-V) plot for the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au FG-NVFM structure.

enhanced reliability and feasibility for the use of the Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au structure for NG-NVFM applications.[5]

In summary, the considerably wide memory window and long term data retention for the fabricated Pt/Ti/Al_2O_3/GO/graphene/SiO_2/p-Si/Au suggest the potential of graphene and GO as a FG and buffer layer for NVFM applications. The low dimensionality, high work function, and high density of states support the use of graphene as FG, while the GO buffer layer over graphene favors the uniform and pin hole free deposition of blocking layer (Al_2O_3). The benefits of the fabricated FG-NVFM are as follows: first, it can be utilized for fabrication of low-cost memories, and second, the compatibility of the adopted approach with the existing semiconductor processing, thus paving the way for future electronic applications.

The authors thank the C4DFED and AMRC, IIT Mandi, for the graphene growth and electrical and material characterization facilities. The authors are also thankful to CeNSE, IISC Bangalore, (under INUP) for the deposition of tunnel and blocking layers and etching facilities for the fabrication of device structures. M.S. also thanks IIT Mandi for the financial support.

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