Realization and Performance Analysis of Facile-Processed $\mu$-IDE-Based Multilayer HfS$_2$/HfO$_2$ Transistors

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Abstract—A new and interesting field-effect transistor (FET) structure based on multilayer HfS$_2$ as a channel material, integrated with Al $\mu$-interdigitated electrodes ($\mu$-IDES) and HfO$_2$ as a gate dielectric is reported for the first time. The electrical performance of Al/HfO$_2$/HfS$_2$/Al$_{\mu}$-IDE-based FETs exhibited the threshold voltage of $\sim$−2.72 V, generous subthreshold swing (SS) of $\sim$70 mV/dec, substantial $I_{ON}/I_{OFF}$ ratio of $\sim10^4$, transconductance of $\sim$1.5 $\mu$S, and a significantly high electron mobility of $\sim$56.7 cm$^2$/Vs at $V_{ds} = 1$ V, and low gate leakage current of $\sim$47 nA/cm$^2$ at $V_{gs} = −1$ V. Therefore, moderate threshold voltage, generous SS, robust current saturation, ultralow off-state leakage current, and low operating voltage of the fabricated Al/HfO$_2$/HfS$_2$/Al$_{\mu}$-IDE FETs show its potential for next-generation (NG) low-power FET applications.

Index Terms—$\mu$-Interdigitated electrodes ($\mu$-IDES), HfO$_2$, HfS$_2$, low leakage current, low subthreshold swing (SS).

I. INTRODUCTION

TRANSITION METAL dichalcogenides (TMDs) have captivated significant attention of the scientific fraternity to overcome the current limits of silicon-based technology due to their versatile properties, such as high carrier mobility of extremely thin channel regime, mechanical flexibility, high optical absorption coefficient, and potential for large-scale growth and processing [1]–[4]. Moreover, TMDs have enabled the fabrication of atomically thin layers with low density of dangling bonds and low surface roughness due to the weak van der Waals forces between the adjacent layers of the corresponding bulk materials [5].

Manuscript received March 6, 2019; revised April 27, 2019 and May 9, 2019; accepted May 11, 2019. Date of publication June 5, 2019; date of current version June 19, 2019. This work was supported in part by the Ministry of Human Resource Development, Government of India, and in part by the Science and Engineering Research Board, Government of India, through the National Post Doctoral Fellow (N-PDF) Scheme under Grant PDF/2016/003135. The review of this paper was arranged by Editor K. Alam. (Corresponding authors: Hitesh Shrimali; Satinder K. Sharma.) S. Sharma, S. Das, H. Shrimali, and S. K. Sharma are with the School of Computing and Electrical Engineering, IIT Mandi, Mandi 175005, India (e-mail: hitesh@iitmandi.ac.in; satinder@iitmandi.ac.in).

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Digital Object Identifier 10.1109/TED.2019.2917323

Of late, numerous TMDs have been investigated, such as MoS$_2$, MoSe$_2$, WS$_2$, WSe$_2$, HfS$_2$, HfSe$_2$, ReS$_2$, and so on [4], [6]–[10]. Among these, hafnium disulfide (HfS$_2$) was earlier considered as a semi-insulating material because the measured conductivity of HfS$_2$ is very low compared with that of MoS$_2$. Recent studies predicted that HfS$_2$ is a strong contender as a channel material for next-generation (NG) field-effect transistors (FETs) because of its reasonable bandgap ($\sim$1.2 eV) and electron mobility ($\sim$1833 cm$^2$/Vs), as compared to its TMD counterparts [11], [12].

TMDs act as the strong candidature, especially for tunnel FET applications. Although it suffers from low ON current and scaling channel length-related device issues, it can be addressed by using high quality and excellent device electrostatics of TMD film, and also with high-$\kappa$ dielectric along with the modified geometry of the device structure [13], [14].

There are several techniques for the synthesis of two-dimensional (2-D) materials mostly based on the mechanical exfoliation, chemical exfoliation, i.e., the top-down approach [1], [15], and chemical vapor deposition [16]. Despite the good quality of the 2-D material, it suffers from very low yield and flake size. However, the chemical synthesis route of the TMDs has not been well explored, especially for electronic device fabrication to date. The merit of this technique includes the potential for bulk production of the desired materials in electronic device applications [17]. Moreover, the chemical route allows the film formation of the material for device fabrication which reduces the cost of the production significantly.

Furthermore, the gate dielectric for 2-D semiconducting layer, especially the insulator/2-D semiconductor interface, plays a critical role to define the carrier mobility and the gate leakage current density of the FETs [18], [19]. The lattice mismatch between the semiconductor and the gate dielectric can increase the surface scattering and results mostly in mobility degradation. Therefore, the dielectric/semiconductor interface engineering can efficiently dampen the Coulombic scattering of charge carriers in the atomically thin 2-D layer through the engineering of lattice mismatch effect between the semiconducting material and high-$\kappa$ dielectric [20].

The top-gated geometry has the advantage that it provides local gate biasing at low voltage, high-speed switching, and high integration density [21]. In order to reduce contact...
resistance and parasitic capacitances, it is preferable to use top-gated devices. Moreover, to control the time-dependent degradation of the transistor, the top-gated geometry provides isolation from the moisture and contaminants from the environment. In the case of 2-D materials, the lithography on the atomically thin layer may cause severe damage to atomic structure and degrade the electrical properties of the FETs. Hence, to realize a viable device structure and performance, the integration of \( \mu \)-interdigitated electrodes (\( \mu \)-IDE) based geometry has been determined to serve as the source and drain at the underneath of the spin-coated chemically synthesized HfS\(_2\) multilayer. Recently, HfS\(_2\) as a conducting channel and Al\(_2\)O\(_3\) as a dielectric-based transistor are demonstrated where the drive voltage and charge carriers mobility are high and low, respectively [1].

Here, we report the \( \mu \)-IDE based multilayer of HfS\(_2\) FETs with top-gated dielectric HfO\(_2\) for the first time to the best of authors’ knowledge. The integration of \( \mu \)-IDEs along with high-\( k \) material as the dielectric layer in HfS\(_2\) FETs exhibit excellent transistor properties such as electron mobility \( \sim 56.7\ \text{cm}^2/\text{Vs} \), subthreshold swing (SS) \( = 70\ \text{mV/dec} \), current on/off ratio \( \sim 10^4 \), and transconductance of \( \sim 1.5\ \mu \text{s} \) establishing its competency for low-voltage NG FET applications.

II. EXPERIMENTAL

The Al/HfO\(_2\)/HfS\(_2\) device structure-based FETs have been fabricated on the SiO\(_2\)/Si substrate with the integration of Al \( \mu \)-IDEs as illustrated in Fig. 1(a). Initially, the SiO\(_2\)/Si substrate is cleaned by acetone boiling at 60 \(^\circ\)C, rinsed by isopropanol (IPA), and heated at 200 \(^\circ\)C. Then, Al thin film (~50 nm) is deposited by thermal evaporation at \( \sim 1 \times 10^{-6}\) mbar pressure followed by defining Al \( \mu \)-IDEs by standard Maskless Optical Lithography (Intelligent Micro Patterning) process. The SU-8 (2002; Micro-Chem) negative photoresist was spin coated on the Al/SiO\(_2\)/Si samples. The samples were then subjected to pre-exposure bake (PB) from room temperature (RT) to 95 \(^\circ\)C for 10 min, and after PB, the samples were cooled down to RT. After the PB process, the samples were exposed to the illumination of 365-nm UV using Maskless Optical Lithography to pattern \( \mu \)-IDE structure, and the samples were consequently subjected to post exposure bake (PEB) from RT to 105 \(^\circ\)C for 10 min. Thereafter, samples were developed using SU-8 developer (Micro-Chem), for 1 min followed by IPA rinse and N\(_2\) gas purging and performed the hard bake at 150 \(^\circ\)C for 20 min. To achieve \( \mu \)-IDE patterns, samples were etched through Al standard etchant [22]. The SU-8 covering the necessary Al was removed from samples by using N-methyl-2-pyrrolidone (NMP). The samples were incessantly stirred in NMP at 50 \(^\circ\)C for about 5 h and rinsed by IPA to remove the NMP. Here, to minimize the parasitic [23]–[26], seven finger architecture of \( \mu \)-IDE which serve as source and drain for the end device, has been used and the channel length of \( \mu \)-IDEs has been kept \( \sim 15\ \mu \text{m} \) to utilize the maximum flakes deposited by spin coating in the next step.

HfS\(_2\) is prepared by a low-cost chemical route (hot injection method) using hafnium chloride (HfCl\(_4\)) and carbon disulfide (CS\(_2\)) as precursors at 350 \(^\circ\)C [17]. In brief, HfS\(_2\) was prepared by adding the sulfur precursor at 350 \(^\circ\)C in the solution of hafnium chloride and oleylamine, and heated for \( \sim 14\) h. The stock solution was made using butanol and hexane mixture in 1:1 ratio. For spin coating, the solution is sonicated for \( \sim 5\) h to separate the flakes and centrifuged to remove the bulk portion. The supernatant is mixed with butanol in 1:50 ratio to obtain the desired solution for spin coating. Multilayers of HfS\(_2\) are spin-coated over Al\(_{\mu \text{-IDE}}\)/SiO\(_2\)/Si substrate and confirmed by Atomic Force Microscope (AFM).

Furthermore, HfO\(_2\) thin films are deposited by RF magnetron sputtering from the HfO\(_2\) target (purity 99.99\%) at \( \sim 150\) W, Argon (100 sccm), and \( \sim 6 \times 10^{-3}\) mbar process pressure. Before sputtering on an active substrate, pre-sputtering was performed for \( \sim 10\) min to eliminate any impurities present on the target surface. Finally, the top metal gate is deposited by thermal evaporation of Al (~100 nm) through a shadow mask and confined to the fingers of \( \mu \)-IDEs. The final realized device Al/HfO\(_2\)/HfS\(_2\)/Al\(_{\mu \text{-IDE}}\) structure is shown in Fig. 1(b). The cross-sectional view of the Al/HfO\(_2\)/HfS\(_2\)/Al\(_{\mu \text{-IDE}}\) device structure is shown in Fig. 1(c).

The thickness of multilayers (~five layers with each monolayer of thickness \( \sim 0.7\) nm) of HfS\(_2\) is \( \sim 3.4\) nm and surface morphology of both HfS\(_2\) and HfO\(_2\) are confirmed by AFM (Dimension Icon Bruker). The thickness of HfO\(_2\) thin film is measured by variable angle spectroscopic imaging ellipsometer (EP4-SE; Accurion). The chemical analysis of HfS\(_2\) has been confirmed by confocal Raman spectrophotometer (LabRAM HR Evolution; Horiba) with the excitation wavelength of 532 nm in the range of 300–500 cm\(^{-1}\). Raman mapping was done with gratings of 600 gr/mm and a very low laser power of \( \sim 0.17\) mW on the sample. The electrical properties of the multilayer HfS\(_2\), FETs with HfO\(_2\) as a gate dielectric were analyzed at RT using Keithley 4200-SCS.
The rms roughness of sputtered HfO₂ thin film is 0.17 mW.

Fig. 3. (a) Surface micrographs of spin-coated HfS₂ flakes. (b) Height profile of the HfS₂. Surface morphology of the sputtered HfO₂ thin films at room temperature. (c) 2-D micrograph. (d) 3-D micrographs.

Confocal Raman spectroscopic analysis has been performed with the excitation wavelength of 532 nm for the confirmation of HfS₂, as shown in Fig. 2. The Raman spectrum peak near 325 cm⁻¹ confirms the presence of A₂u mode for 1H phase of HfS₂ which corresponds to the out-of-plane vibration of S atoms in the HfS₂ structure. Similar observations are noticed in [27] and [28].

The surface morphology, thickness measurements of spin-coated multilayers, HfS₂ flakes as prepared by the chemical route and dielectric thin film, HfO₂ deposited by sputtering have been analyzed by tapping mode AFM as shown in Fig. 3. The rms surface roughness and the thickness of multilayers HfS₂ are ~1.16 and ~3.4 nm, respectively. On the other hand, the rms roughness of sputtered HfO₂ thin film is ~0.27 nm. The thickness of the HfO₂ is measured to be ~13.5 nm.

III. RESULTS AND DISCUSSION

Fig. 4(a) shows the output (Iₘₐₓ–Vₚₖₑ) characteristics of the Al/HfO₂/HfS₂/Al₁₋₈₅₋₉ IDE-based FETs. The moderately linear behavior of Iₘₐₓ versus Vₚₖₑ is observed at low voltage up to 1 V suggesting the partially ohmic contact between μ-IDFET and HfS₂. The significant enhancement in drain saturation current (5.8 μA at Vₚₖₑ = 2 V) as collated from [1] (0.8 μA at Vₚₖₑ = 40 V) may be attributed to the non intrusion of atmosphere with the channel region, resulting in higher stability. This evidently proves the stronger gate coupling with HfO₂ as the dielectric and results in strong drain current saturation (~5.8 μA at Vₚₖₑ = 2 V).

Fig. 4(b) illustrates the transfer (Iₘₐₓ–Vₚₖₑ) characteristics determined by measuring the drain–source current (Iₘₐₓ) as the function of top gate voltage (Vₚₖₑ) at the fixed drain voltage (Vₘₐₓ). It is evident from Fig. 4(a) and (b) that the drain currents in the output characteristics as well as in the transfer characteristics are approximately the same for Vₚₖₑ = 0 V and Vₘₐₓ = 1 V, both the characteristics have Iₘₐₓ = ~3.5 μA as marked with orange and green circles in Fig. 4(a) and (b), respectively. The Iₘₐₓ/Idₐₜ ratio, SS, and threshold voltage (Vₜₐₜ) are estimated to be ~10⁴, 70 mV/dec, and ~2.72 V, respectively. SS is calculated by the inverse subthreshold slope of the logarithmic drain current (Iₘₐₓ) to the applied gate to source voltage (Vₚₖₑ) as depicted by the black circle on the black curve of Fig. 4(b). The Iₘₐₓ/Idₐₜ ratio, here, is calculated from transfer characteristics for the curve where Vₘₐₓ is 1 V (IₘₐₓFF when Vₚₖₑ = 5 V, Iₘₐₓ when Vₚₖₑ = 2 V). Here, the threshold voltage (Vₜₐₜ) is computed from linear extrapolation (blue curve) of Iₘₐₓ–Vₚₖₑ curve in the linear region [29] as shown in Fig. 4(b) and marked with the red circle on the x-axis of the graph.

In the transistor, the field-effect mobility (μ) was calculated by the plot of Iₘₐₓ versus Vₚₖₑ at the fixed drain voltage of 1 V from the following equation [30]:

\[
\mu = \frac{\partial I_{d_x}}{\partial V_{g_x}} \frac{L}{W C_{ox} V_{d_x}}
\]
where $C_{ox}$ is the capacitance of the device Al/HfO$_2$/HfS$_2$/Al$_{IDE}$ in the accumulation region. Here, the capacitance ($C_{ox}$) of $\sim 34$ nF/cm$^2$ at 500 kHz was used to calculate the FET mobility. The channel width ($W$) is 70 $\mu$m and channel length ($L$) is 15 $\mu$m which leads to computed field-effect electron mobility of Al/HfO$_2$/HfS$_2$/Al$_{IDE}$ structure to be $\sim 56.7$ cm$^2$/V$\cdot$s.

The $C$–$V$ characteristics are obtained by sweeping the gate voltage from accumulation (+3 V) to inversion (−3 V) at 500 kHz (frequency) as illustrated in Fig. 5(a) and (b). HfS$_2$ being used here is intrinsically n-type. Thus, from +1 to +3 V being called as the accumulation region, where HfS$_2$ is the active channel at $V_{gs} > 0$ V and operates in accumulation region. Similarly, as revealed from the output characteristics, where $I_{ds}$ increases with $V_{gs}$ from 0 to 2 V as a result of majority charge carrier accumulation in the channel region. On the other hand, $V_{gs} < 0$ V causes the channel to deplete gradually, also designates from the decrease in $I_{ds}$ with variation of $V_{gs}$ from −1 to −3 V in the output characteristics, may be due to the depletion of majority charges in channel region or at the interface of HfO$_2$/HfS$_2$, which eventually instigates towards the inversion beyond −1 V due to the inversion of charges in the channel region [31]–[33].

The Al/HfO$_2$/HfS$_2$/Al$_{IDE}$ structure is attributed to the lower parasitic [23]–[26] leading to the enhancement of mobility. The capacitance–voltage ($C$–$V$) characteristics of Al/HfO$_2$/HfS$_2$/Al$_{IDE}$ (by shorting the drain and source and without shorting the source and drain) at different frequencies are shown in Fig. 5(c) and (d) which envisages the lower capacitance for the latter case. This significant variation in $C_{max}$ of Al/HfO$_2$/HfS$_2$/Al$_{IDE}$ structures might be attributed to the lateral leakage between S and D. After the shorting of source and drain, higher value of capacitance of Al/HfO$_2$/HfS$_2$/Al$_{IDE}$ structure is witnessed; on the other hand, lower value of capacitance is noticed when source and drain are not shorted, as a consequence of charge carrier leakage and Maxwell–Wagner dispersion between electrodes [23]. This Maxwell–Wagner dispersion results into the lateral scattering of the charge carriers at the dielectric/semiconductor interface when the bias is applied at the gate and drain is left open, and when the source and drain are shorted, the charges are confined in the channel region. Here, preferentially, n-type carrier transport behavior is observed for the fabricated device of $\sim 3.4$ nm, HfS$_2$(multilayer) channel. The total gate capacitance can be modeled as the combination of the capacitances due to oxide ($C_{ox}$), quantum confinement in the channel ($C_q$), and the trapped charges ($C_{IT}$) in the HfO$_2$/HfS$_2$ interface [34]–[36] as shown in Fig. 6(a) and (b). Here, as the quantum capacitance ($C_q$) of the Al/HfO$_2$/HfS$_2$/Al$_{IDE}$ FETs originated in the inversion layer of the nanoscale device, which does not completely screen the quasi-static electric field during applied gate voltage ($V_{gs}$), the partial penetration of external electric field through the multilayer HfS$_2$ semiconducting channel will generate excess charge carriers and attribute to the quantum capacitance ($C_q$). Since 2-D-based low dimension Al/HfO$_2$/HfS$_2$/Al$_{IDE}$, FETs on current is the average carrier velocity times the charge injected into the channel region [34]. In fact, the electrical and transport characteristics of FETs are a function of the electrostatic field-effect control of these channel mobile carriers upon applied bias ($V_{gs}$).

The voltage drop across the channel is less than the total bias applied at the gate terminal; hence, the quantum capacitance ($C_q$) is the function of the localized channel potential ($V_{lch}$) and can be expressed as [34]:

$$C_q = -\frac{q}{eV_{lch}}.$$

The interface trap density between HfO$_2$/HfS$_2$ interface is computed to be around $10^{10}$ (eV)$^{-1}$ cm$^{-2}$ as shown in Fig. 6(a) from the following standard subthreshold slope ($S_S$) expression [33]:

$$S_S = \left(1 + \frac{C_D + C_{IT}}{C_{ox}}\right)(ln10) \left(\frac{kT}{q}\right).$$
Fig. 7. $J_{g-V_g}$ (gate leakage current density to the applied gate bias) characteristics of Al/HfO$_2$/HfS$_2$/Al-μ-IDE FET fabricated at room temperature.

Fig. 8. $g_m-V_{gs}$ (transconductance versus gate bias) at $V_{ds} = 1$ V characteristics of Al/HfO$_2$/HfS$_2$/Al-μ-IDE, μ-IDE FET-fabricated structure.

where $S_S$ is the subthreshold slope, $C_D$ and $C_A$ are the capacitance of the semiconductor and the interfacial trap charges, respectively.

In general, lower leakage current density is desired for low static power dissipations in NG FETs, hence increasing the lifetime of the device operation. The gate leakage current is calculated to be $\sim 47$ nA/cm$^2$ at $-1$ V gate voltage from the leakage current–voltage ($J-V$) characteristics shown in Fig. 7.

The transconductance ($g_m$) plays a crucial role in the transistor gain, which is an important parameter, especially for analog circuit implementations. Therefore, transconductance ($g_m$) of Al/HfO$_2$/HfS$_2$/Al-μ-IDE FETs is computed by the following relation [29], [30]:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$$

where $I_{ds}$ is the drain current at particular $V_{ds}$, and $V_{gs}$ is the applied gate bias.

However, for circuit applications, the transconductance must be high which reduces the contact resistance and hence, improves the device performance [37]; the maximum calculated value of $g_m$ for Al/HfO$_2$/HfS$_2$/Al-μ-IDE is $\sim 1.5$ $\mu$S as shown in Fig. 8.

Finally, Table I shows the state-of-the-art available reports related to 2-D TMDs based FETs. It clearly perceives that the chemically synthesized HfS$_2$-based FETs shows comparable electrical parameters with the mechanically exfoliated other 2-D materials. It can be clearly seen from the calculated parameters that the fabricated FETs show good SS and higher mobility than the other HfS$_2$-based FETs. The extracted transistor parameters strengthen the candidature of the proposed FET structure for NG technology beyond silicon.

### IV. Conclusion

In summary, a new and interesting μ-IDE-based multilayer HfS$_2$ transistor with HfO$_2$ as a gate dielectric is investigated for low-power FETs applications. The electrical performance of Al/HfO$_2$/HfS$_2$/Al-μ-IDE, FETs exhibit high electron mobility of $\sim 56.7$ cm$^2$/Vs, the threshold voltage of $\sim -2.72$ V, SS of $\sim 70$ mV/dec, and transconductance of $\sim 1.5$ $\mu$S which reveal high compatibility of HfS$_2$, 2-D TMD with HfO$_2$ as a gate dielectric for NG FETs. The surface morphology investigation revealed a smooth surface of both the conducting 2-D channel material (HfS$_2$) as well as of high-κ dielectric (HfO$_2$). Thus, the low threshold voltage, steep SS, ultralow OFF-state leakage current, and low operating voltage of the demonstrated μ-IDE-based multilayers HfS$_2$ FETs with HfO$_2$ gate dielectric proves its potential for NG low-power device applications.

### Acknowledgment

The authors would like to thank the Centre for Design and Fabrication of Electronic Devices (C4DFED) and Advanced Materials Research Centre (AMRC) IIT Mandi, for the use of various state-of-the-art device fabrication and characterization facilities for this paper. The author S. Sharma would like to thank Dr. S. Srinivasan, IIT Mandi, for discussion about the quantum effect of devices.

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