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Reduced switching mode for SAR ADCs: analysis and design of SAR A-to-D algorithm with periodic standby mode circuit components

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Abstract: This study presents the analysis and design of reduced switching (RSw) activity mode successive approximation register (SAR) analogue-to-digital (A-to-D) algorithm. For given analogue-to-digital converter (ADC) specifications, RSw mode design is based on the observation that the signal variation in two successive samples becomes linear over a certain range of input frequencies. Hence, dispensable switching activity between the two samples can be eliminated by enabling periodic temporal reference to the converter. No prediction or logic circuitry is required to extract information from previous bits. However, there exists a trade-off between the input frequency and the sampling frequency. A design criterion is derived using numerical mathematics to skip evaluation of the optimum number of bits while maintaining the desired signal-to-noise and distortion ratio. The design criterion is validated through behavioural simulations using MATLAB/Simulink®. Furthermore, a fully differential 10-bit, 104 kS/s ADC is designed in a standard 180 nm CMOS technology to demonstrate circuit implementation of the RSw mode. In the RSw mode, power dissipation in the comparator and relevant digital circuitry decreases by 20%. The ADC achieves low-frequency effective number of bits of 9.7 bits and spurious free dynamic range of 68.3 dB. With 1.8 V supply voltage, average power dissipation in the core ADC is 2.54 μW; resulting in figure-of-merit of 29.3 fJ/conv-step.

1 Introduction

As a result of rapid evolution in CMOS technology, circuit techniques for mm-scale sensing systems are gaining popularity. Characteristics of the signal that need to be acquired by the sensor nodes depend on the application. In bio-sensing, personalised health care monitoring and data logging applications the input is slow varying and has limited dynamic range [1, 2]. Whereas, in applications such as audio, sensor embedded RFID, environmental sensing (temperature, pressure etc.), manufacturing and supply chain the signal bandwidth is in kHz range [3–5]. Moreover, the data acquisition has become very diverse because of the precise classification of the signals owing to advancement in technology. For example, the category of low bandwidth bio-signals itself has differences in voltage range and occupied frequency spectrum. An EEG signal falls in 0.1 to 100 Hz while an EMG signal resides in 500 Hz to 5 kHz of frequency band [6]. Typically, sensor networks comprising of distributed sensor nodes can perform sensing, processing and communicating tasks. Digital processing of the data makes the system more capable and enhances its ability to perform sophisticated processes. Therefore, an analogue-to-digital converter (ADC) becomes one of the essential circuit blocks to interface the physical world signal with the digital signal processing circuitry.

Among several ADC architectures, a successive approximation register (SAR) ADC is preferred for digitisation because of the following three reasons. First, its architecture is relatively simple. Secondly, it primarily consists of digital circuits which are beneficial in terms of technology down scaling. Thirdly, the ADC consumes minimal bias/static current since it rarely requires a high-performance op-amp, such as the one analysed in [7]. Low speed, high-resolution SAR ADCs are reported in the literature for very low bandwidth applications [8, 9]. On the contrary, moderate resolution ADCs having a sampling rate up to 1 MS/s are used in system-on-chip (SoC) measurement and wireless sensor networks [10–12]. Further the literature survey reveals efforts in the direction to use medium speed ADCs (few hundreds of kS/s) with circuit techniques for reducing power consumption in low bandwidth regime [13–20]. From another perspective, these designs intend to increase the ADC utilisation span over a broader frequency range without dissipating power in unnecessary switching. However, augmented circuit complexity of the design in the form of prediction logic, accuracy tracker, error checking and digital output correction limits flexibility and configurability of the ADC for multi-sensory input SoC applications.

A method to configure an SAR ADC in reduced switching (RSw) mode without employing circuit blocks that excessively increase the architectural complexity to eliminate superfluous switching is proposed in this paper. For a certain input frequency range, sampling makes signal variation in successive samples linear. This causes several significant bits corresponding to the samples redundant. RSw mode gets rid of redundant switching by using temporal reference point available to the converter. A design criterion is derived based on numerical mathematics to operate an ADC in the RSw mode. For given ADC specifications, the analysis obtains the frequency range of RSw mode and finds the optimum number of bit-cycles to skip during consecutive conversions. Unlike predictive designs, which extract information from previous bits [14, 18, 20, 21], no additional prediction logic or error checking and correction circuitries are required to implement the proposed analogue-to-digital (A-to-D) algorithm. Although analytical formulation presented in this paper is generic, a 10 bit, 104 kS/s ADC is designed to show circuit-level realisation of the RSw mode A-to-D algorithm. The comparator and digital control circuitry are modified to incorporate RSw mode in the design. These circuits are made inactive to save switching energy dissipation in the RSw mode. Hence, the proposed technique decreases the power consumption of the ADC circuit components with negligible circuit complexity and area overhead. Moreover, consistent performance over process, voltage and temperature (PVT) variations is ensured owing to the circuit simplicity of this method.

The remaining part of the paper is organised as follows: Section 2 presents the proposed concept and the criteria derived to optimally implement the RSw mode. The MATLAB/Simulink model and the behavioural simulation results are presented in Section 3. The SAR ADC architecture and its circuit components

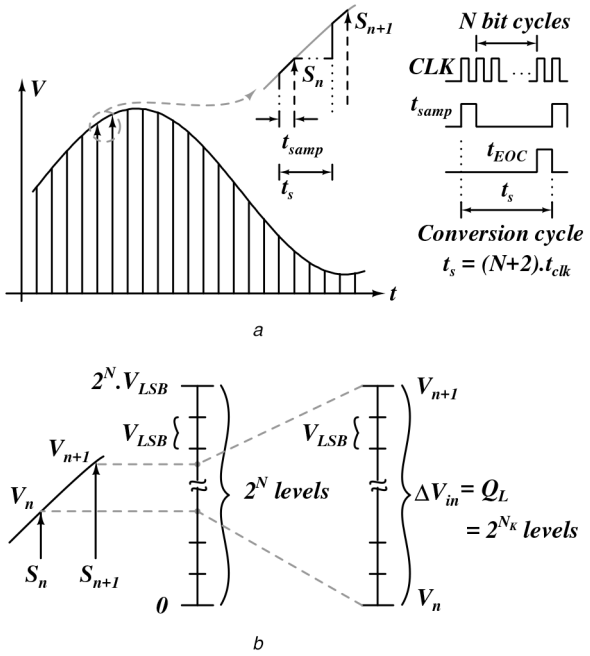

Fig. 1 *RSw mode concept illustration*

(a) A slow varying signal sampled at high frequency and its linear approximation, ***(b)*** Quantisation levels corresponding to small change in the input signal during consecutive samples

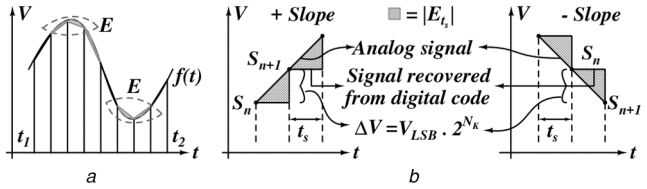

Fig. 2 *Application of numerical mathematics in the RSw mode ADC design*

(a) Approximation of the integral of a continuous-time function using composite trapezoids, ***(b)*** Representation of input signal and recovered signal assuming linear variation between two successive samples

in a standard 180 nm CMOS process are described in Section 4. Lastly, the simulation results confirming the benefits of the proposed method are presented in Section 5, followed by conclusions in Section 6.

2 RSw mode concept and the design criteria

2.1 Concept

If the input signal is bandlimited to a frequency, f_b where $f_b \ll f_s$ then the signal variation between two samples becomes linear because of the closely placed samples. In this case, redundant switching can be eliminated without any prediction and control logic circuitry if temporal reference is provided to the converter.

Fig. 1*a* exemplifies a situation where a slow varying signal is sampled at a high frequency. For reference voltage V_{REF}, the resolution of an N-bit ADC is $V_{REF}/2^N$. As depicted in Fig. 1*b*, for a small change in the input signal (ΔV_{in}) between consecutive samples S_n and S_{n+1}, the quantisation levels need to be resolved by the converter are determined as:

$$Q_L = \frac{\Delta V_{in}}{V_{LSB}} = \frac{\Delta V_{in} \cdot 2^N}{V_{REF}}. \quad (1)$$

These levels correspond to N_K least significant bits (LSBs) of successive quantisation such that

$$N_K \geq \frac{\log Q_L}{\log 2}. \quad (2)$$

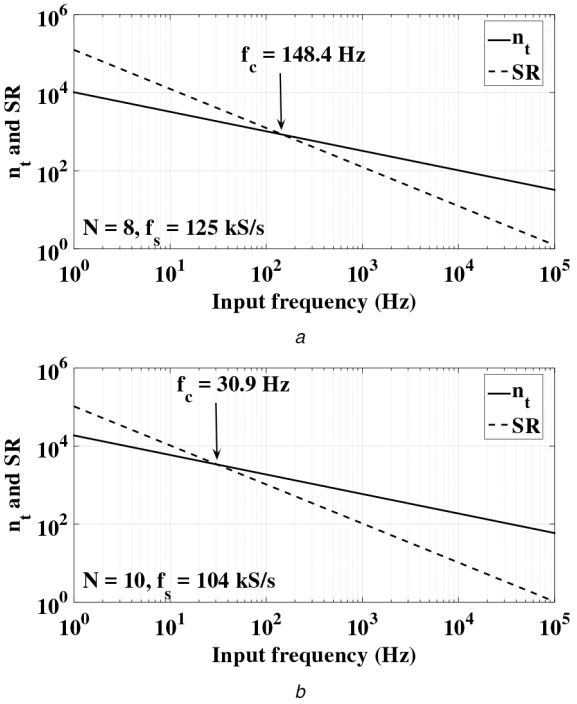

Fig. 3 *Critical point frequency estimation using composite trapezoidal rule. Case study for*

(a) $N = 8$ and $f_s = 125$ kS/s, ***(b)*** $N = 10$ and $f_s \simeq 104$ kS/s

Assuming that the digital code corresponding to S_nth sample is known, $N_P = N - N_K$ significant bits are redundant in the digital code of the sample S_{n+1}. Therefore, by calculating only N_K LSBs, N-bit accuracy can be achieved for every S_{n+1}th sample ($n = 1, 3, 5\ldots$). Here, it can be noted that alternate conversion-cycles constitute the periodic reference point from where the ADC skips N_P significant bits.

2.2 Design criteria

First, an upper bound on the input frequency that can be linearised to N-bit resolution while operating at sampling frequency f_s is calculated and then, the allowable values of N_P bits for the calculated upper bound are obtained. Numerical analysis (trapezoidal method) of approximating definite integral is used for this purpose.

Integral of a continuous-time function can be approximated as the summation of the areas of composite trapezoids of equal height [22]. If the original function has two derivatives on an interval [t_1, t_2], then the error (E) between the areas under the curve of a continuous function and its trapezoidal approximation (refer Fig. 2*a*) on that interval is given as:

$$\left|E\right| \leq \frac{(t_2 - t_1)^3}{12 \cdot n_t^2} \cdot \xi, \quad (3)$$

where n_t is the number of partitions and ξ is an upper bound for $|f''(t)|$ on $t_1 \leq t \leq t_2$. Considering a sinusoidal input, value of the upper bound for $|f''(t)|$ can be calculated as $\xi = A \cdot \omega_{in}^2$ where A is the amplitude and $\omega_{in} = 2\pi f_{in}$ is the angular frequency of the continuous-time input.

From the ADC viewpoint, error budget can be obtained from

$$|E| = V_{LSB} \cdot t_s, \quad (4)$$

where t_s represents the sampling period. From (3) and (4), the value of n_t which satisfies the error bound for a given input frequency can be evaluated as:

$$n_t \geq \sqrt{\frac{t_{\text{in}}^3 \cdot \xi}{12E}}. \quad (5)$$

Fig. 3 shows the sampling ratio (SR = $t_{\text{in}}/t_{\text{s}}$) and the corresponding n_t for various input frequencies. Clock frequency of 1.25 MHz is assumed and two cases are studied: $N = 8$, $f_{\text{s}} = 125\,\text{kS/s}$ and $N = 10$, $f_{\text{s}} \simeq 104\,\text{kS/s}$. In Fig. 3, the point at which the solid line crosses the dotted line is the critical point. For respective set of resolution and sampling frequency, the critical point represents a frequency range for which the input can be linearised without degrading the signal-to-noise ratio (SNR). Frequency at the critical point is denoted as f_{c}. For $f_{\text{in}} < f_{\text{c}}$, the sampling ratio is greater than the corresponding n_t and hence error in the area of continuous-time signal and its linear approximation over SR intervals is less than the maximum error bound obtained from (4).

Now, for an N-bit f_{s} S/s ADC, consider the case of $f_{\text{in}} \leq f_{\text{c}}$; making the input change linear during each conversion-cycle. If digital output of this converter is passed through an ideal N-bit digital-to-analogue converter (DAC) then the output of the DAC is a stair-case waveform with a period $t_{\text{s}} = 1/f_{\text{s}}$. As shown in Fig. 2*b*, for maximum change of ΔV in the input signal, error in the areas under the curve of continuous-time signal and the signal recovered from digital code is bounded by

$$\left|E_{t_{\text{s}}}\right| = 0.5 \cdot V_{\text{LSB}} \cdot 2^{N_K} \cdot t_{\text{s}}. \quad (6)$$

However, skipping evaluation of the significant bits for alternate samples may degrade the linearity (and SNR) of the ADC. Therefore, to achieve N-bit linearity while skipping N_P bits, (6) must be modified for the resolution and linearity of $(N + N_P)$-bit ADC. Hence, the new value of error bound, E_{t_{s},N_P}, is formulated as:

$$\left|E_{t_{\text{s}},N_P}\right| = 0.5 \cdot V_{\text{LSB}} \cdot 2^{N_K - N_P} \cdot t_{\text{s}}. \quad (7)$$

The critical frequency denotes the maximum input frequency which can be linearised to the required accuracy. At this frequency, $(t_2 - t_1) = t_{\text{in}} = 1/f_{\text{c}}$ and $n_t = \text{SR}$. Therefore, maximum change, ΔV, in the successive samples over SR intervals can be obtained from the given input function, which is sinusoidal in this case. Then error in the area under the curve of approximately linear input signal and its digital representation, $E_{\Delta V}$, can be calculated as:

$$|E_{\Delta V}| = 0.5 \cdot \Delta V \cdot t_{\text{s}}. \quad (8)$$

Equating (7) and (8) eventually leads to the difference $N_K - N_P$. Since $N_K + N_P = N$, optimum values of the N_K and N_P bits are obtained by solving two-variable simultaneous equations. For the case of $N = 10$ and $f_{\text{s}} \simeq 104\,\text{kS/s}$, N_K and N_P are found to be 6 and 4, respectively.

3 Behavioural modelling: verification of the design criteria

Computer simulations play a major role in circuit design to get the most optimised results. Mixed-mode simulators like Cadence AMS are very efficient and lead to better circuit design. However, due to the higher circuit complexity of the designs they might consume a lot of time even at early stages including concept validation. An alternative approach of behavioural modelling can drastically reduce simulation time. Behavioural simulations are extensively used for capacitive DAC modelling of an SAR ADC. We apply this method of analysis to RSw mode ADC. The proposed concept and the design criteria are modelled in MATLAB/Simulink and verified through behavioural simulations before physical level implementation. The model follows the SAR ADC working principle using a behavioural description of various circuit components without considering the device's physical properties. Fig. 4 shows a top-level block diagram of the model. Apart from the conventional process flow of an SAR ADC, a standby window

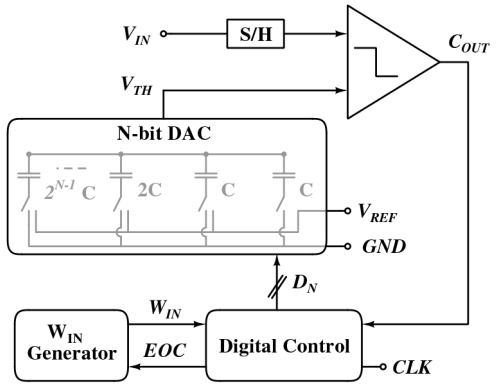

Fig. 4 *Top-level block diagram of the ADC model*

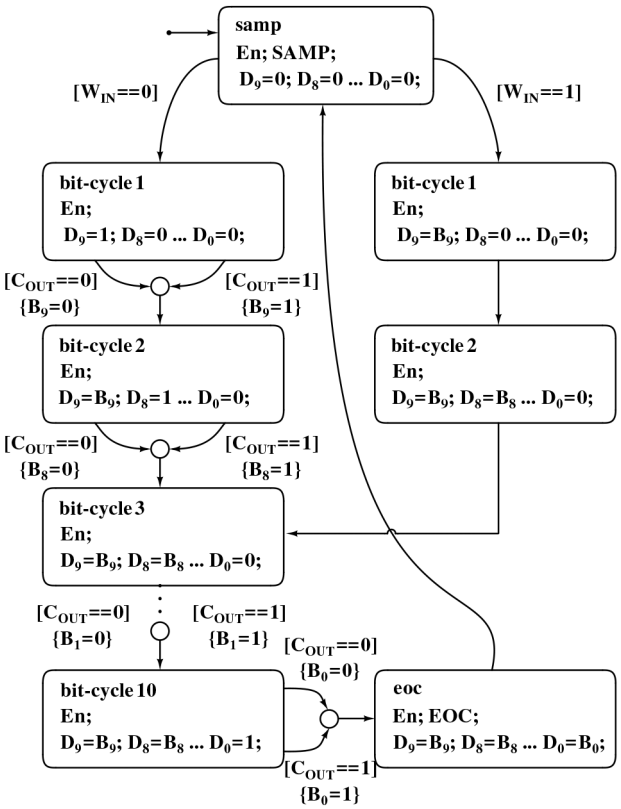

Fig. 5 *MATLAB Stateflow diagram of the digital control block for an example case of $N = 10$, $N_K = 8$ and $N_P = 2$*

generator block is introduced in the model. This block produces the timing reference required for significant bit skipping.

Complete digital control is implemented as a state machine where the state transition diagram or table represents each step of the conversion-cycle. The transition diagram, modelled in the Stateflow® environment is triggered by the ADC clock in Simulink [23, 24]. Fig. 5 shows the state transition diagram of the digital control block used to model the proposed concept for an example case of $N = 10$, $N_K = 8$ and $N_P = 2$. Before transiting from the sample state to the most significant bit (MSB) state, the status of W_{IN} the signal is checked. Bit skipping is enabled if W_{IN} is at logic 1. During the bit skipping, values stored in the local parameters during previous conversion-cycle (when $W_{\text{IN}} = 0$) are used as the binary outputs instead of considering the comparator decisions to evaluate bits. Note that this digital control can be easily modified to skip the desired number of significant bits by changing a number of the states in the respective branch.

An in-built library function from DSP System Toolbox is used to implement the S/H block. The SAMP event generated by the Stateflow chart triggers the S/H block. The comparator model is shown in Fig. 6 emulates circuit topology of a high-gain and high-speed static comparator. Difference in the sampled input and the

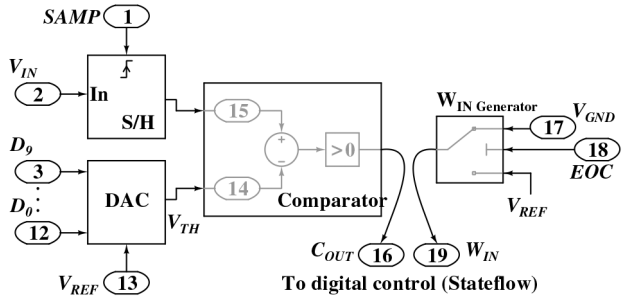

Fig. 6 *Behavioural model of the ADC building blocks in Simulink*

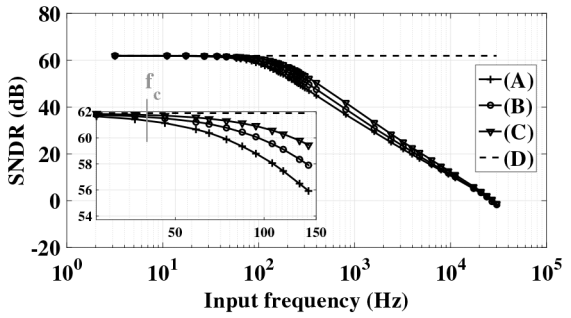

Fig. 7 *Behavioural simulation results showing SNDR of a 104 kS/s ADC in full conversion and RSw modes*
(A) $N_K = 5$ and $N_P = 5$, ***(B)*** $N_K = 6$ and $N_P = 4$, ***(C)*** $N_K = 7$ and $N_P = 3$, ***(D)*** Full conversion mode

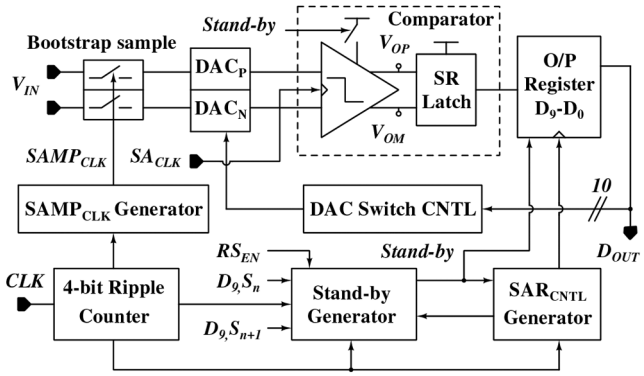

Fig. 8 *Proposed ADC architecture showing standby mode comparator and digital logic for the RSw mode operation. Here, D_9, S_n and D_9, S_{n+1} are the MSBs evaluated in the odd and even conversion-cycles, respectively*

threshold voltage is compared to zero for generating the binary output. For the 10-bit SAR ADC example under consideration, the threshold voltage can be represented as:

$$V_{\mathrm{TH}} = \frac{D_9 \cdot V_{\mathrm{REF}}}{2^1} + \frac{D_8 \cdot V_{\mathrm{REF}}}{2^2} \cdots + \frac{D_0 \cdot V_{\mathrm{REF}}}{2^{10}}, \tag{9}$$

where D_9 through D_0 denote comparator output in respective bit-cycles. Equation (9) is implemented as a MATLAB function to model behaviour of a binary-weighted C-DAC in an SAR ADC. The standby window generator block is one-bit counter and it counts the occurrence of the end-of-conversion (EOC). Count of one implies the assertion of W_{IN} the signal. Fig. 6 also shows the model of the window generation block, employing a simple switch. Since the EOC event changes sign in every conversion-cycle, the window generator produces alternate high and low outputs; providing the necessary periodic reference to the converter for bit skipping.

MATLAB/Simulink behavioural simulation results for signal-to-noise and distortion ratio (SNDR) of a 104 kS/s ADC in full conversion and RSw modes are presented in Fig. 7. When bit skipping is disabled in full conversion mode, the converter behaves as an ideal 10-bit ADC having constant SNDR over entire Nyquist

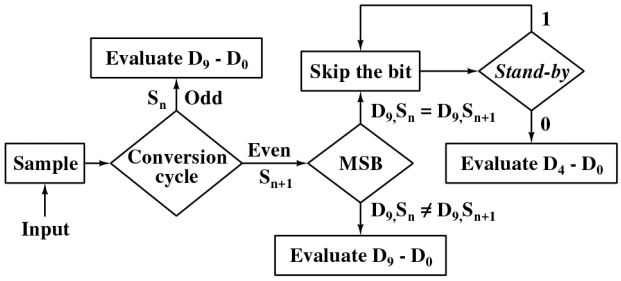

Fig. 9 *A-to-D conversion flowchart for $N_P = 4$ in the RSw mode*

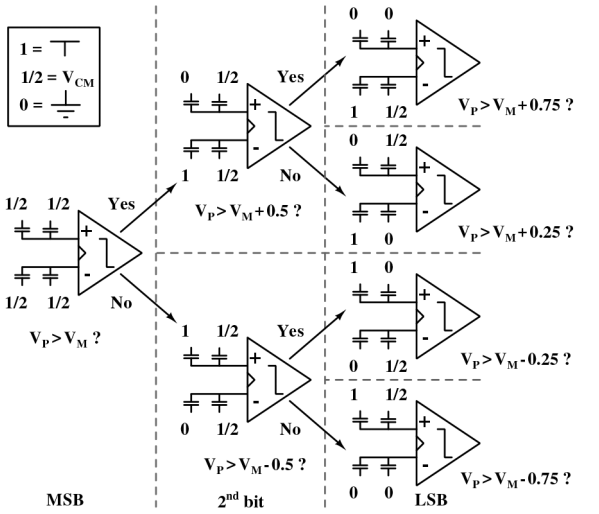

Fig. 10 *DAC switching procedure for a 3 bit example case*

frequency range. In the RSw mode, the SNDR starts to fall at certain input frequencies depending on the combination of N_K and N_P bits. For the case of $N_K = 6$ and $N_P = 4$, it can be seen that till 31 Hz input frequency the SNDR remains fairly equal to the SNDR of ideal 10-bit ADC and it starts to roll down thereafter. This value of input frequency is in close agreement with the value of critical frequency obtained from the analysis of Section 2 (refer Fig. 3*b*). Furthermore, it can be noted that other combinations of N_K and N_P bits either fail to get full benefits of the RSw mode or degrade the ADC SNDR at critical frequency. Hence the proposed concept and the derived design criteria are validated.

Following the analysis and the behavioural simulations, a user-friendly graphical user interface (GUI) is designed in MATLAB. The GUI allows users to input ADC specifications (full-scale voltage, resolution and sampling frequency) and calculates the RSw mode parameters (critical frequency, N_K and N_P).

4 ADC architecture and circuit components

The RSw mode concept can be utilised to save power consumption of the comparator and the digital control circuit in the SAR ADC. A fully differential transistor-level SAR ADC with specifications same as that of Fig. 3*b* is designed to demonstrate power reduction in aforesaid circuit components. In the RSw mode, the ADC skips evaluation of 4 significant bits, D_8 to D_5, in consecutive conversion-cycles. Fig. 8 shows the proposed architecture of SAR ADC. The ADC is largely an event-driven converter. In addition to the clock, output of the ripple counter controls the events that should occur in a conversion-cycle.

During the sampling phase, the input is sampled on to the DAC capacitors through bootstrap switches. A-to-D conversion flowchart of the RSw mode design is shown in Fig. 9. The conversion-cycles of samples S_n and S_{n+1} are treated as odd and even cycles where $n = 1, 3, 5\ldots$ The standby generator block is synchronised with the counter. The generator first determines whether the conversion-cycle is odd or even, compares the MSBs if the conversion-cycle is even and then asserts a *Standby* signal if the MSBs are same. If the conversion-cycles are odd, then the routine

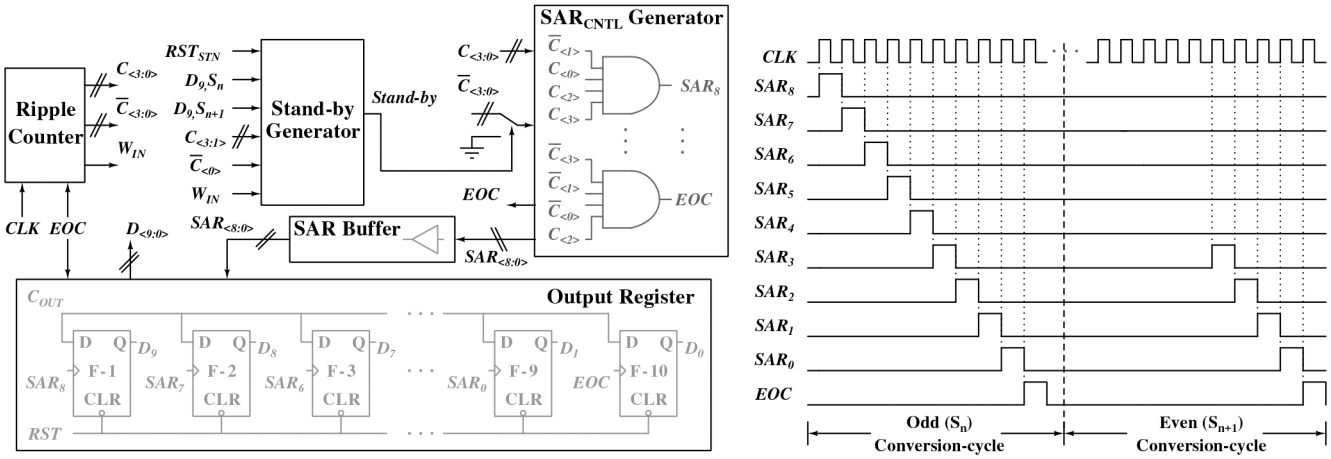

Fig. 11 *Block diagram of the ripple counter-based digital control circuit modified to incorporate the proposed concept and the timing diagram for the output of SAR_{CNTL} generator in odd and even conversion-cycles*

procedure is followed and all the bits are evaluated. MSBs are compared to detect positive/negative signal changes and confirm that the two successive samples have polarity. It is worth mentioning that, boundary crossing at the skipped significant bits (e.g. from 0011…1 to 0100…0) introduces only 1 LSB error which is tolerable according to the budget given in (4). The counter deactivates *Stand–by* signal once N_P bits are skipped in the even conversion-cycle. Remaining bits are then resolved and EOC is raised to indicate the availability of the converted digital code.

4.1 Capacitive DAC

Several DAC architectures and switching schemes have been reported in the literature to improve the energy efficiency of the converter [25–28]. V_{CM}-based switching, merged capacitor switching and capacitor-splitting DAC scheme are some of the examples of progressive switching methods which can reduce switching energy by 87.5, 93.4 and 96.9%, respectively. Although energy efficiency is the primary objective of these switching procedures, switching logic complexity, tolerance to V_{CM} variation, area reduction and matching requirements are the parameters which trade against each other in deciding the DAC topology.

The proposed concept is not specific to any DAC switching procedure. However, the DAC topology for circuit implementation decides figure-of-merit (FoM) since the DAC switching power contributes approximately one-third of overall power consumption. The DAC architecture, adapted from [26], is chosen because it saves 93.7% switching energy compared to the conventional DAC, it is less dependent on the accuracy V_{CM} and only 256 unit elements on a single side are needed to achieve 10-bit resolution. The DAC switching procedure for a three-bit example case is explained in Fig. 10. In this implementation, the MIM capacitor is used for the DAC capacitor bank. Note that, inherent mismatch in the DAC capacitor array limits the value of the unit capacitor (C_U) [29]. For this switching scheme, we derived an equation to obtain the minimum value of C_U set by the mismatch parameters and it is given in (10)

$$C_U = 18 \cdot (2^{N-1}) \cdot K_\sigma^2 \cdot K_C \tag{10}$$

K_σ and K_C are the technology-dependent matching coefficient and capacitor density, respectively. The process used for this design provides a capacitor density of 1 fF/μm^2 with a 4% error rate. From (10), the minimum allowable value of the unit capacitor required for $N = 10$ is found to be 14.8 fF. However, in the chosen technology, the minimum value of the MIM capacitor defined by the design rules is 17.8 fF. Hence, 20 fF of the unit capacitor is used for the DAC design. This selection of slightly higher unit capacitor also serves to decrease the effect of parasitic associated with the interconnecting metals.

4.2 Digital control circuit for RSw mode operation

Conventional architecture of digital control circuit consists of the shift register and SAR sub-blocks [30]. The shift register generates control signals for the SAR block. The SAR block receives comparator's decision as an input and determines sequential C-DAC switching depending on the received input. Once all the bits are resolved, both the sub-blocks are reset for the next conversion-cycle. Considering an N-bit SAR ADC employing a trial-and-error procedure based on the binary search algorithm, $(N+2)$ clock cycles are required to complete one conversion-cycle. Hence, for a 10-bit ADC with the conventional digital control circuit, 12 flip-flop shift register and 10 flip-flop SAR are required. It can be noted that the flip-flops in the SAR block operate at sampling frequency whereas the flip-flops in the shift register switch at $(N+2) \times f_s$ frequency. Therefore, with an increase in resolution and sampling frequency, the power dissipation of the digital control circuit increases considerably.

Counter-based digital control circuit is used in this design to reduce power consumption and circuit complexity. Fig. 11 shows a detailed implementation of the counter-based control circuit, modified to incorporate the proposed concept. A 4-bit ripple counter replaces the shift registers of the conventional synchronous digital circuit. The counter is designed to count $(10+2)$ pulses on every positive edge of the clock. Augmented 2 counts are for the sampling and EOC cycles. Compared to 12 flip-flops of conventional design only 1 flip-flop (which receives the clock signal) operates at $12 \times f_s$ frequency. The operating frequency of remaining flip-flops sequentially reduces to half of the previous value. This approach also provides flexibility to easily change the control circuit for the desired resolution. For example, the same 4-bit ripple counter can be used for a 12-bit ADC by just modifying the reset logic of the counter.

Outputs of the ripple counter generate trigger signals for the output register block. Since on a particular count, only one AND gate is active, as shown in Fig. 11, the pattern of sequential pulses is obtained at the output of SAR_{CNTL} the generator. These pulses are then passed through the SAR buffer block and are used for triggering the flip-flops in the output register to store the comparator's decision in the bit-cycles. The buffer provides two inverter delays in the signal path to mitigate setup time violation at the flip-flop input.

Standby generator: Fig. 12 shows the gate-level implementation of the standby generator circuit. Two D flip-flops are used; one for storing the MSB generated in the odd conversion-cycle, and another for generating the *Standby* signal. Extra circuitry is not required for generating the control signals which trigger these two flip-flops. The signal W_{IN} comes from the ripple counter while the signal SAR_7 is generated by the SAR_{CNTL} generator. Similar to $SAR_{\langle 8:0\rangle}$, the signal W_{CNTL} is also obtained using the output of the ripple counter. Initially, the *Standby* signal is reset to logic 0. MSB generated in the odd conversion-cycle ($W_{IN} = 0$) is

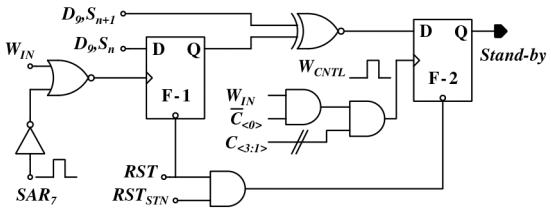

Fig. 12 *Gate-level implementation of the standby generator circuit for the proposed 10 bit ADC architecture*

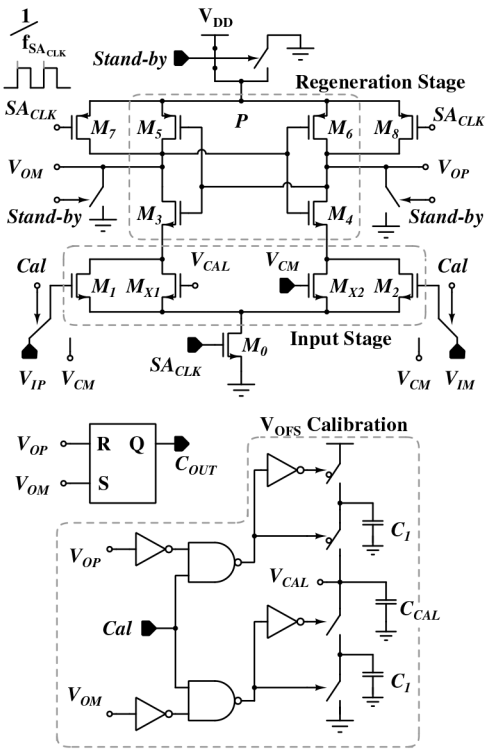

Fig. 13 *Dynamic latch comparator of the ADC. In default case, V_{DD} is connected to the circuit. When standby is asserted, V_{DD} is disconnected from the circuit and nodes P, V_{OP} and V_{OM} are connected to ground. The bubbled switch conducts when the gate voltage is at logic 0*

stored in F-1. XNOR gate compares MSB evaluated in the even conversion-cycle ($W_{IN} = 1$) with the stored value of F-1. If the comparison is true, XNOR outputs logic 1. Triggered during even conversion-cycle, F-2 becomes transparent and sets *Standby* signal to logic 1. Flip-flops have active-low reset and RST_{STN} reset F-2 to bring *Standby* output back to logic 0 when 4 significant bits are skipped.

Since the significant bits are not evaluated in the even conversion-cycle, $SAR_{\langle 8:4\rangle}$ pulses are not required to trigger the flip-flops of the output register. Hence, during the period when *Standby* signal is at logic 1, the complementary outputs of the ripple counter ($\bar{C}_{\langle 3:0\rangle}$) are disconnected from the SAR_{CNTL} generator and the corresponding input terminals of the SAR_{CNTL} generator are connected to GND. This reduces power dissipation in SAR_{CNTL} generator and buffer blocks by avoiding unwanted switching of AND and NOT gates. Output of the SAR_{CNTL} generator during odd and even conversion-cycles is depicted in Fig. 11. While the standby mode is ON, the $DAC_{P,N}$ switch control signals are generated using the digital codes stored in the output register during odd conversion-cycle.

For a D flip-flop to have only static power dissipation through leakage current, switching activity at both D and CLK inputs must be zero (provided that SET and CLR inputs are disabled). Although it may seem that transition from 0 to 0 and 1 to 1 does not dissipate power, CMOS implementation of the flip-flop does consume power due to charging and discharging of internal nodes [31]. As explained in the next subsection, the comparator output in the standby mode is held at a constant level to bring down switching activity at the D input to zero. Since switching at the CLK input is also nulled with the proposed digital circuit, a small leakage current defines power consumption of the output register in the standby mode.

4.3 Dynamic latch comparator for RSw mode operation

Fig. 13 shows the circuit implementation of the dynamic latch comparator used in the ADC. The comparator comprises an input stage, a regenerative stage stacked over the input stage and an SR latch. On the assertion of *Standby* signal, V_{DD} of the input and regeneration stage of the comparator is turned OFF to disable the quantiser. The output nodes V_{OP} and V_{OM} are grounded to prevent leakage current flow into the PMOS substrate. The arrangement seems to create an invalid input state for the SR latch. Hence, to avoid malfunction in transiting from the invalid state to the valid state, the *Standby* mode is revoked when the CLK is at logic 0 state.

Comparator offset voltage is one of the performance-limiting parameters. In present-day down-scaled technology nodes, offset voltage caused by the transistors mismatch can severely degrade ADC performance. Static offset reduces available input rage whereas dynamic offset affects the ADC transfer characteristics. Depending on the sign of the offset, the ADC output may saturate before the input attains full scale value or the ADC continues to generate all zeros even after the smallest input voltage change. Therefore, unless an external offset calibration is feasible, the comparator requires an extra on-chip circuitry to cancel the offset voltage. This circuit adds up to the comparator's power consumption. As shown in Fig. 13, the self-calibrating offset cancellation loop is used in this design to consider a practical scenario of mismatch in sub-nanometer process technologies. Before the A-to-D conversion process begins, the comparator is calibrated by applying logic 1 at *Cal* signal. During the calibration phase, the switched capacitor circuit in the calibration loop adjusts V_{CAL} to offset voltage (V_{OFS}). In the conversion phase ($Cal = 0$), calibration current due to V_{CAL} continues to flow through the transistor M_{X1}; compensating for the offset voltage. A thorough analysis of the self-calibrating comparator can be found in [32].

Power dissipation analysis: Power dissipation in the input and regeneration stage of the comparator can be expressed as:

$$P_{comp} = P_{dyn} + P_{leak} + P_r, \tag{11}$$

where $P_{dyn} = f \cdot C_L \cdot V_{DD}^2 \cdot \gamma$ represents the switching power, $P_{leak} = V_{DD} \cdot I_{leak}$ denotes the leakage power and P_r is the regenerative power consumed due to regenerative charge. C_L is the load capacitance, γ is the probability of the output switching from logic 0 to logic 1 and I_{leak} is the leakage current. Assuming the input is evenly distributed between 0 and V_{REF}, recalling (11) and (12) from [33], regenerative power can be written as: $P_r = f_s \cdot V_{DD} \cdot Q_C$, where Q_C signifies regenerative charge of a complete conversion-cycle. In an N-bit conventional ADC, dynamic comparator is switched in every bit-cycle and hence $\gamma = 1$. Therefore, power consumption in the dynamic comparator used for conventional ADC is:

$$P_{conv} = N f_{SA_{CLK}} C_L V_{DD}^2 + V_{DD} I_{leak} + f_s V_{DD} Q_C. \tag{12}$$

In the RSw mode, depending on the status of the conversion-cycle (odd/even) and the *Standby* signal, two successive conversion-cycles will dissipate different amounts of power. When the standby window is active, both the switching power and the leakage power are zero, since the nodes P, V_{OP} and V_{OM} are connected to ground. Therefore, average power dissipation in the comparator of the RSw mode ADC is formulated as:

$$P \simeq \frac{(1+\zeta)(P_{dyn} + P_{leak}) + P_r + P_{r,K}}{2}, \tag{13}$$

where $P_{r,K} = f_s \cdot V_{DD} \cdot Q_{C,K}$ is the regenerative power in the even conversion-cycle and ζ is $(N_K)/N$. The regenerative charge in the even conversion-cycle, $Q_{C,K}$, can be written as:

$$Q_{C,K} = C_L V_{eff} N_K \left[2\ln\left(\frac{V_{DD}}{A_K V_{REF}}\right) + (N_K + 1)\ln 2 + 2 \right].$$

The reduction in power (P_{save}) of the comparator achieved using proposed architecture is obtained by subtracting (13) from (12) and is given as:

$$\begin{aligned} P_{save} &= 0.5(1-\zeta)(P_{dyn} + P_{leak}) + 0.5P_r - P_{r,K} \\ &\simeq 0.5(1-\zeta)(P_{dyn} + P_{leak}). \end{aligned} \quad (14)$$

Notably, similar analysis (without regenerative component) holds for the digital circuit blocks which have been put into stagnant mode when the standby signal is active.

5 Results and discussion

The linearity of the ADC is evaluated using a histogram test. Fig. 14 shows the differential non-linearity (DNL) and integral non-linearity (INL) errors plotted with respect to the output codes. Peak DNL and INL errors are found to be −0.12/ + 0.51 LSB and −0.67/ + 0.54 LSB, respectively. Spectral analysis is carried out using tone testing. SNDR of the ADC for various input frequencies is shown in Fig. 15. Low-frequency SNDR is 60.2 dB; providing effective number of bits (ENOB) of 9.7 bits. In full conversion mode, SNDR is constant over the entire Nyquist range. At high input frequency, signal change during two successive samples becomes non-linear. Hence, as anticipated from our analysis, RSw mode SNDR falls with the increase in input frequency. Effective resolution bandwidth (ERBW) of the ADC in RSw mode of operation is 112 Hz. Dependence of the converter's SNDR on the input frequency can also be seen from Fig. 16 where SNDR of the ADC for low frequency and near ERBW input is plotted for different signal magnitudes. The ADC achieves a dynamic range of 61.6 dB. However, the peak SNDRs are 2.4 dB apart from each other.

Fig. 17 shows the ADC output spectrum for full scale and near-critical frequency sinusoidal input. Spurious free dynamic range (SFDR) of the ADC is 68.3 dB. Because of differential implementation, SFDR is dominated by the third harmonic. The ADC output spectrums in full conversion and RSw modes are indistinguishable from each other; providing evidence to support the proposed concept of RSw Mode for an SAR ADC. 100-run Monte Carlo simulations are performed on the design to gain fair idea of the effect of statistical mismatch on the ADC performance. Results of the analysis are shown in Fig. 18. The mean value (μ) of maximum DNL and INL is 0.58 and 0.77 LSB with standard deviation (σ) of 0.37 and 0.32 LSB, respectively. The effect of mismatch is more prominent on SFDR than SNDR with σ(SNDR) of 2 dB compared to σ(SFDR) of 4.6 dB from their corresponding mean values.

With 1.8 V supply voltage, total power dissipation in the core ADC is 2.54 µW. The standby generator circuit consumes only 36 nW of power. FoM of the ADC is 29.3 fJ/conv-step. Table 1 compares the simulated and the analytical values of achieved power reduction in building blocks of the ADC which are switched stagnant when the *Standby* signal is asserted. The analytical results are in good agreement with the simulation results. Power dissipation in the comparator and the pertinent digital circuitry decreases by 20.5% in RSw mode.

Table 2 presents the ADC results at various PVT corners. The standby generator circuit consists of only digital components. Implementation of RSw mode algorithm using periodic standby generator circuit is insensitive to PVT variations. Hence, the proposed ADC design is as immune to process variations as the conventional or well established SAR ADC designs, laid out with an utter focus on the analogue parts.

Fig. 19 shows the layout of the ADC in a standard 180 nm CMOS technology. The design occupies 0.537×0.383 mm^2 of area. Area of the standby generator circuit is 44×36.5 µm^2, barely 0.78% of the total area. For better matching, common centroid type layout is designed for the DAC capacitors. It can be observed that MIM capacitors (DAC and on-chip calibration) consume approximately one-third of the total area. A netlist was generated from the layout. The design was simulated rigorously considering device mismatch and PVT variations. Table 3 compares the ADC performance with the relevant literature which uses a 180 nm process. Using a simple bit skipping approach based on the proposed concept, the ADC achieves remarkably better FoM than [9, 15–17]. One of the reasons for this is because the proposed architecture, to a large extent, remains similar to the conventional SAR ADC but, consumes lesser power in the desired bandwidth.

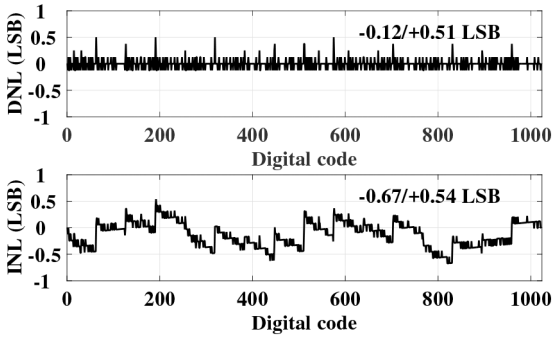

Fig. 14 *Differential and integral non-linearities (DNL and INL) of the ADC*

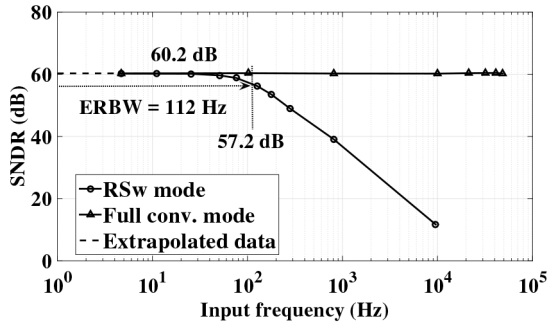

Fig. 15 *SNDR of the ADC versus input signal frequency*

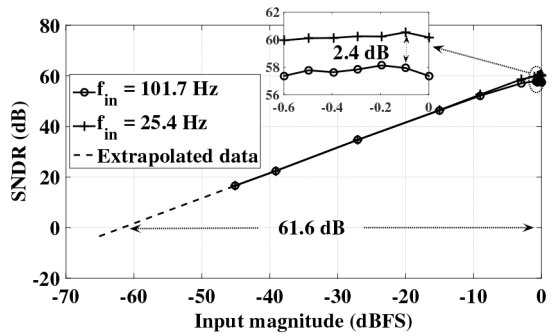

Fig. 16 *SNDR of the ADC for different magnitudes of the input sinusoid*

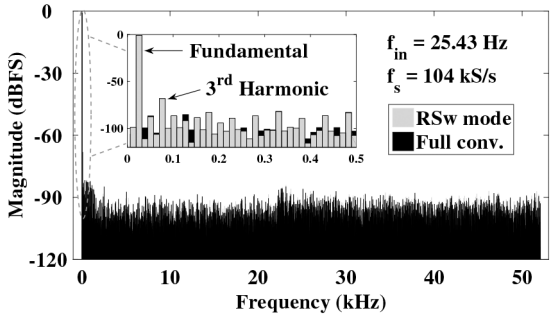

Fig. 17 *8192 points DFT of the ADC output at 104 kS/s*

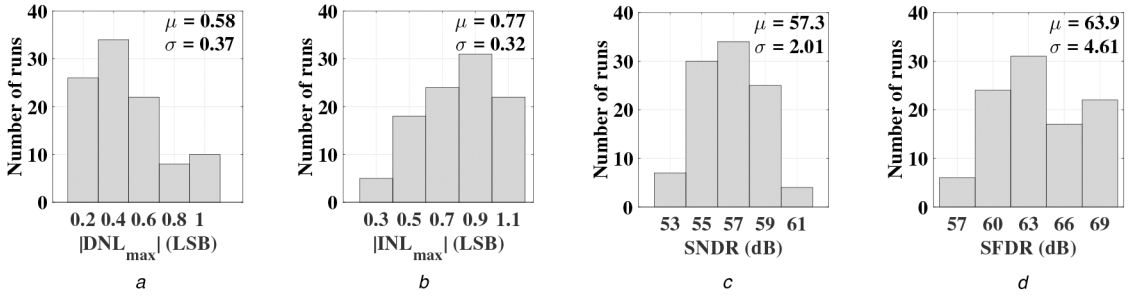

Fig. 18 *Monte Carlo analysis for various performance matrices of the ADC in RSw mode operation*
(a) DNL, ***(b)*** INL, ***(c)*** SNDR, ***(d)*** SFDR

Table 1 Power consumption in the ADC circuit components

	Without standby, nW	With standby, nW	P_{save}, nW	P_{save} (14), nW
comparator	467	385	82	93
SAR_{CNTL} Gen.	127	100	27	25
SAR buffer	109	81	28	22
output register	176	133	43	35

Table 2 ADC performance at PVT corners

PVT corner	SNDR, dB	SFDR, dB	ENOB, bits	Power, μW	FoM, fJ/step
TT, 1.8 V, 27°C	60.2	68.3	9.7	2.54	29.3
SS, 1.62 V, −20°C	59.6	73.1	9.6	1.83	22.6
FF, 1.98 V, 80°C	59.2	66.4	9.5	4.46	59.1
SF, 1.8 V, 27°C	60.5	69.1	9.8	2.57	27.7
FS, 1.8 V, 27°C	59.9	68	9.6	2.55	31.5

Table 3 Performance summary and comparison with relevant SAR ADCs

Ref.	Process, nm	V_{DD}, V	Res., bits	f_s, kS/s	DNL, LSB	INL, LSB	Power, μW	f_{in}, Hz	SNDR, dB	SFDR, dB	ENOB, bits	FoM, fJ/step
[13][b] 2011	180	0.6	10	100	−0.7/0.4	−0.7/0.8	1.3	50 k	57.5	67	9.3	21
[14][b] 2012	180	1	10	500	−0.9/0.9	−0.8/0.5	14.2	250 k	57.3	76	9.2	47
[15][b] 2013	180	1.1	8	10	−0.18/0.34	−0.20/0.27	0.127	5 k	46.3	61.9	7.4	63.4
[16][b] 2013	180	1.8	10	62.5	−0.08/0.07	−0.09/0.32	2.95	10	59.4	—	9.6	62.2
[17][b] 2014	180	0.9	9	100	085	1.52	1.33	1 k	50.1	65.1	8.0	51.3
[9][a] 2016	180	1.8	14	10	—	—	10.3	511	84.2	107	13.7	77
[20][a] 2018	180	0.6	10	500	0.424	0.424	2.47	ERBW	59.2	—	9.54	12.7
This work[a]	180	1.8	10	104	−0.12/0.51	−0.67/0.54	2.54	25[c]	60.2	68.3	9.7	29.3
								100[d]	57.8	67.8	9.3	38.7

[a]Simulation results.
[b]Measurement results.
[c]Near f_c.
[d]Near ERBW of RSw Mode.

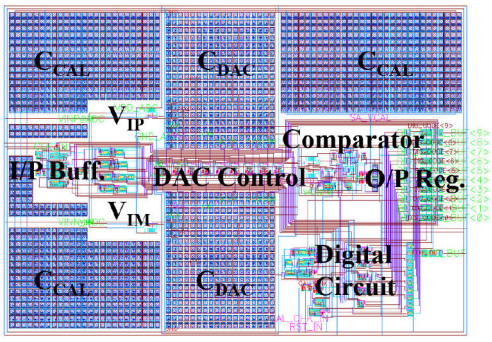

Fig. 19 *Layout of the ADC in a standard 180 nm CMOS process*

From (12), it can be seen that the dynamic power consumption scales with V_{DD}^2. Hence the achieved FoM with 1.8 V of V_{DD} is acceptable when compared to FoM of [13, 20] at 0.6 V V_{DD}. Moreover, the proposed concept is generic and it is not specific to the DAC architecture used in this design. Therefore, it can be utilised for SAR A-to-D algorithm with contemporary low energy DAC switching procedures such as [34, 35], to further improve the FoM.

6 Conclusions

For given ADC specifications, this paper shows that there exists a range of frequencies over which, successive input samples have linear relation. Subsequently, an algorithm to utilise the SAR ADC in RSw activity mode within this frequency range is presented. The RSw mode ADC does not rely on prediction or control logic to avoid redundant switching. Here, unnecessary switching activity is eliminated by providing a temporal reference to the ADC. In the RSw mode of operation, inconsequential circuitry is made inactive by asserting periodic standby signal. Based on the numerical

mathematics, a design criterion which relates the given input function, sampling frequency and the standby window size to obtain required performance is also determined. Although the proposed concept is generic, a 10-bit 104 kS/s SAR ADC is considered as an example to demonstrate circuit design of RSw mode A-to-D algorithm. With the standby window of 4 significant bits, a 20% reduction in the power of the RSw mode comparator and digital control circuitry in the ADC is achieved. The static and dynamic performances of the ADC stay constant at all the PVT corners. Once configured in the RSw mode, the standby generator circuit does not demand external control inputs. Therefore, it is included as an integral part of the SAR ADC for resourceful operation. This design approach enhances the benefits of the SAR ADC by offering reconfigurability and versatility in multi-sensory input SoC interface for IoT applications. Usability of the RSw mode can be extended by providing a magnitude reference in conjunction with the temporal reference to further reduce the unnecessary switching power.

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