NrGO Floating Gate/SiO_XN_Y Tunneling Layer Stack for Nonvolatile Flash Memory Applications

Mahesh Soni,[1,2] Ajay Soni,[3] and Satinder K. Sharma*[1]

***Abstract*—This paper presents an ultra–thin silicon oxynitride (SiO_XN_Y, 4 nm) tunneling layer, nitrogen functionalized reduced graphene oxide (NrGO, 3–5 layer) floating gate (FG) and poly (methyl methacrylate) (PMMA, 60 nm) blocking layers based Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au, non–volatile flash memory (NVFM) structures. The ultra–thin SiO_XN_Y helps in improving the interface with Si, resulting in lower gate leakage current density and considerable enhanced retention characteristics. The nitrogen engineered GO followed by reduction to NrGO under UV illumination attributes to the modification of the physiochemical properties, hence beneficial for non-volatile memory applications. The uniform, stress free and low temperature processing advocates the potential of PMMA as blocking layer for improved memory characteristics. The electrical characterizations on the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au gate stack demonstrates a memory window (δW) of ~ 1.25 V @ ± 3 V and ~ 2.6 V @ ± 5 V, low gate leakage current density (J) ~10 nA/cm^2 @ – 1 V, retention ~ 3 × 10^{11} sec (> 10 years with extrapolation) and endurance of more than 100 cycles.**

***Index Terms*— Non-volatile Flash Memory (NVFM), Ultra-Thin Silicon oxynitride, Nitrogen Functionalization, Memory Window, Gate leakage current density, Higher Retention and Endurance**

I. Introduction

For conventional non–volatile flash memory (NVFM) structures, the continuous scaling of tunneling, floating and blocking layers have raised reliability based concerns, small memory window (δW) and low data retention (minimal gate leakage current density ~ < 50 nA /cm^2), for instance [1-7]. To cope with the requirements for large δW, nano wire floating gate (NWFG) based NVFMs with low leakage current characteristics have been demonstrated [8, 9]. Although, the fabricated NW based NVFMs make use of complex geometries, requires multiple processing steps, which makes further device miniaturization difficult [10]. In this context, the low dimensional, solution processable reduced graphene oxide (rGO), FG–NVFMs have gained attention [1, 5, 7]. Previously reported rGO FG–NVFMs demonstrated moderate; memory characteristics (δW ~ 4 V) at high operating voltages (>15 V) [1, 5, 7]. To further improve the performance of the scaled NVFMs operation at low voltages (≤ 5 V), the following plays an important role, (a) interface of the tunneling layer with the Si, [11-14] (b) FG should have sufficient charge trapping sites, high density of states (DOS) (c) interface between the FG and blocking layer [1, 2, 7, 11-15].

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In order to improve the tunneling layer and Si interface, nitrogen incorporation in SiO_2 (silicon dioxide) or oxynitridation of Si has gained interests [11-14, 16-20]. The recent work [11], demonstrates high performance of the gate stack using ultrathin oxynitride as an interfacial layer. The additional impact of nitrogen incorporation in oxides are, (i) improving the dielectric constant, possible to scale further [11, 12], (ii) enhanced immunity to electrical stress, lower gate leakage current [11, 13, 16-20]. In addition to this, during the past decade, one of the leading semiconductor industries (such as IBM) are also looking for oxynitrides (specifically silicon oxynitride (SiO_XN_Y)) as an interface layer [23, 24].

Therefore, in the present investigations, to obtain the uniform interface between tunneling layer and underlying Si, the oxynitridation of Si (silicon oxynitride, SiO_XN_Y) was performed and used as a tunneling layer. To improve the δW in NVFMs operating at low voltages, functionalization (incorporation of additional charge trapping sites) of FG may be advantageous. As discussed in our previous report [9], doping GO with nitrogen (N) followed by reduction to NrGO proved useful and is reported to tune the physiochemical properties [25-27]. The similar atomic sizes between the carbon atoms in GO and nitrogen benefits strong bond formation and provide additional charge trapping sites [25-31].

Further, to maintain interface of the FG with the blocking layer, poly (methyl methacrylate) (PMMA) was spin coated over the NrGO/SiO_XN_Y/p–Si/Au, gate stack and used as blocking layer [9]. The spin coating technique was preferred in the present study as the commonly employed physical deposition techniques over FG NrGO, generate stress on the underlying NrGO leading to generation of additional defects in the NrGO which may degrade the performance of the fabricated NVFMs [9, 32]. This work presents a systematic investigation of the charge storage, gate leakage current density and retention analysis on the fabricated Al/PMMA/NrGO/SiO_2/Si/Au, NVFM structures. The cyclic Capacitance–Voltage (C–V), gate leakage current density– Voltage (J–V), Capacitance – Time (C–T) and endurance measurements were performed using Keithley 4200 SCS parameter analyzer.

II. Experimental

Figure 1 (a) – (h) shows the schematic for the fabricated NrGO FG based Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au, NVFM structures. For the fabrication of NrGO based NVFM structure, 2-inch p–Si wafers (1–10 Ωcm) with <100> orientation were cleaned using standard RCA cleaning (Figure 1 (a)). For high

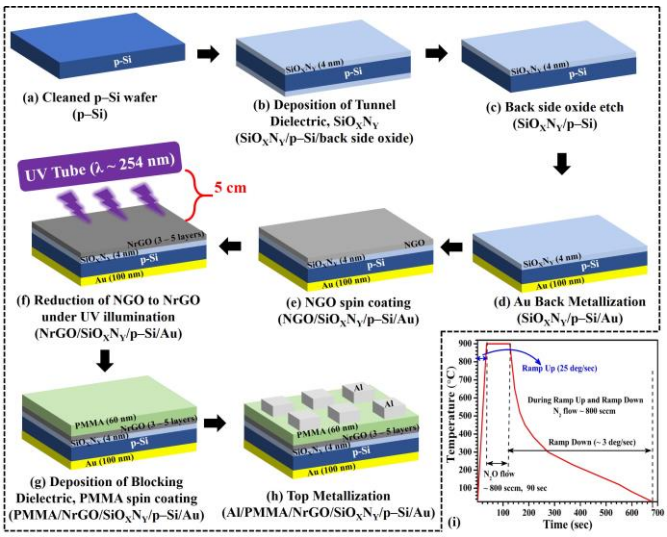

Figure 1 (a) – (h) Schematic view for the NrGO layer based Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au, NVFM structure (i) Time line for the deposition of ultrathin (4 nm) SiO_XN_Y on cleaned Si wafer

quality, ultra-thin SiO_XN_Y tunnel oxide deposition, RCA cleaned Si wafers were loaded to Rapid Thermal Oxidation (AS–One, ANNEALSYS, France Make) at 25 ˚C under N_2 flow (~ 800 sccm) and the temperature was then raised to 900 ˚C at a ramp rate of ~ 25 ˚C/sec. Followed by this, the wafers were subjected to nitrous oxide flow ~ 800 sccm at 900 ˚C for 90 sec. The temperature was then ramped down to 25 ˚C at rate of ~ 3 ˚C/sec under N_2 flow ~ 800 sccm. Timeline and various processing steps for the deposition of ultrathin SiO_XN_Y is shown in Figure 1 (i). Thereafter, the SiO_XN_Y/p–Si/back-side oxide samples (Figure 1 (b)) were subjected to back side buffer oxide etch and immediately loaded into the e–beam evaporator for Au (~ 100 nm) back metallization (shown in Figure 1 (c) and (d)). Afterwards, the synthesized NGO [9, 33-35] was deposited over SiO_XN_Y/p–Si/Au using spin coating at a speed of 500 rpm (acceleration 100 rpm/s) for 15 s immediately followed by 2000 rpm (acceleration 500 rpm/s), for 30 s, finally the sample (NGO/SiO_XN_Y/p–Si/Au) was dried on a hotplate at 70 ˚C for 5 minutes (Figure 1 (e)). For reduction of NGO, the NGO/SiO_XN_Y/p–Si/Au gate stack was kept in a UV chamber for illumination (with a sample to UV tube distance of 5 cm, as shown in Figure 1(f)). The further details regarding the reduction process, material characterizations at intermediate steps [9, 34, 36], number of layers (thickness) of NrGO are presented in our previous report [9, 27]. Later on, over NGO/SiO_XN_Y/p–Si/Au gate stack, PMMA was spin coated at 3000 rpm (acceleration 1000 rpm/s) for 30 s and dried on a hot plate at 80 ˚C for 10 minutes, to serve as a blocking layer (shown in Figure 1 (g)). Finally, top metal, Al electrodes were thermally evaporated over PMMA/NGO/SiO_XN_Y/p–Si/Au using shadow mask to result into Al/PMMA/NGO/SiO_XN_Y/p–Si/Au, NVFM structures, shown in Figure 1 (h).

From each of the aforesaid device processing steps, set of reference samples from the same batch was held in reserve for further physical, chemical, optimization of various parameters and to fabricate the control samples. The thickness of the ultra-thin SiO_XN_Y and PMMA were found to be ~ 4 ± 0.2 nm (using J. A. Woollman ellipsometer) and ~ 60 ± 2 nm (Nanomap-LS stylus profilometer), respectively. The fabricated Al/PMMA/NGO/SiO_XN_Y/p–Si/Au, NVFM structures along with the control samples (Al/PMMA/SiO_XN_Y/p–Si/Au & Al/SiO_XN_Y/p–Si/Au) were also characterized at room temperature.

III. Results And Discussions

The cyclic C–V measurements for the control samples Al/PMMA/SiO_XN_Y/p–Si/Au and Al/SiO_XN_Y/p–Si/Au as shown in inset of Figure 2 (a). It is clear from the C–V measurements on the control samples, that, there is no noticeable difference during the forward (from inversion to accumulation) and reverse (accumulation to inversion) C–V sweeps, attributing towards no charge trapping/de-trapping, confirms for the uniform interface between layers. Further, the cyclic C–V measurements for Al/PMMA(~60 nm)/NrGO/SiO_XN_Y(~4 nm)/p–Si/Au structures at a frequency of 1MHz under different low sweep voltages ± 3 V (marked with "A) and ± 5V (marked with "B") (shown in Figure 2 (a)) were carried out to elevate the memory characteristics, memory window (δW) [9]. As clearly seen from the Figure 2 (a), the cyclic C–V measurements for Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au, NVFM structures demonstrate two interesting characteristics, first, a

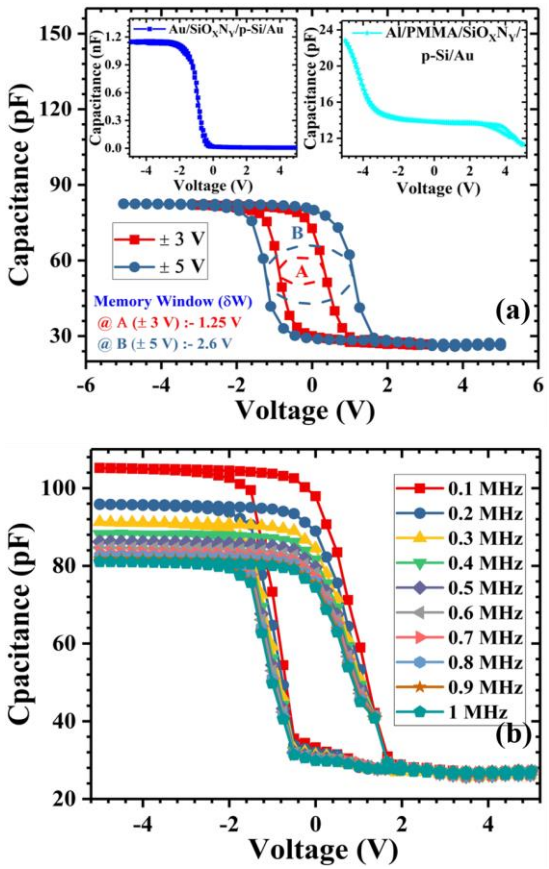

Fig. 2 Cyclic C–V measurements for the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au NVFM structures (a) at 1 MHz under different sweep voltages; (b) at sweep voltage of ± 5 V as a function of frequency ranging from 0.1–1 MHz. Inset in (a) shows the Cyclic C–V characteristics for the control samples (Al/SiO_XN_Y/p–Si/Au and Al/PMMA/SiO_XN_Y/p–Si/Au) showing negligible memory window.

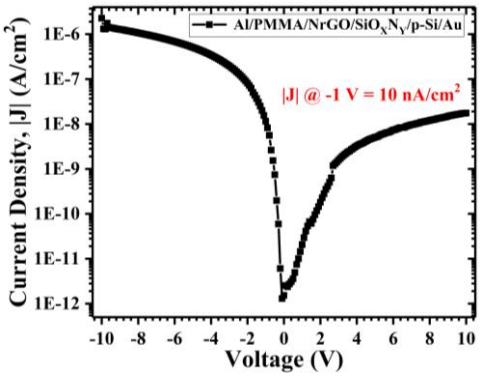

Fig.3|J|–V characteristics for the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au NVFM structure. Inset shows the |J|–V for ± 10 V

clockwise hysteresis and second, a noticeable right shifted flat band voltage (V_{fb}) under reverse sweep. Thus, suggests charge trapping/memory effect in Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au NVFM structure. As observed from Figure 2 (a), δW for the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au NVFM structure is 1.25 V and 2.6 V at sweep voltage of ± 3 V and ± 5 V, respectively. The obtained clockwise hysteresis in the cyclic C–V curves indicates hole trapping in the NrGO layer, in line with the reports in literature [9, 37]. The obtained δW (~ 1.25 V for ± 3 V, 2.6 V for ± 5 V) for the NrGO based NVFM in the present case is significantly higher than reported δW for GO (δW ~ 2.3 V @ –5/8 V) [21], rGO (δW ~ 3 V @ ± 14 V) [1], NrGO (δW ~ 2 V @ + 3 V to –5V) [9], CNT (δW ~ 400 mV for ± 3 V) [22] based NVFM structures, also summarized in the Table I.

To confirm further, that the observed δW in Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au is due to the trapping and de–trapping of charges at the trapping sites in the NrGO layer and not due to dielectric polarization, random defects, cyclic C–V measurements with varying frequency was also carried out [9]. Figure 2 (b) shows the cyclic C–V measurements on NrGO based NVFM gate stack with varying frequency (0.1 – 1 MHz) and clearly rules out the possibility of trapping/de–trapping of charges other than the FG NrGO. Although, it can be seen from Figure 2 (b), that with varying frequency, the cyclic C–V curves are have slightly right shifted V_{fb} and minimal increase in

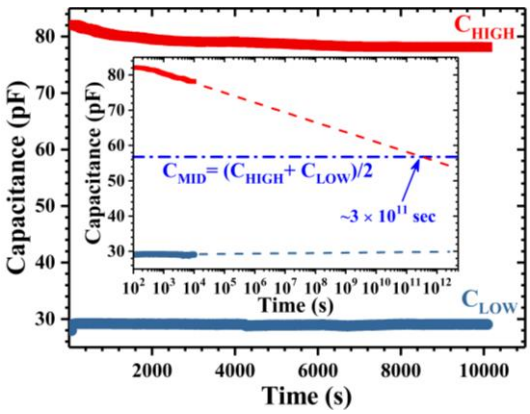

Fig. 4 Retention (C–T) characteristics for the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au NVFM structure. Inset shows the extrapolated C–T curves.

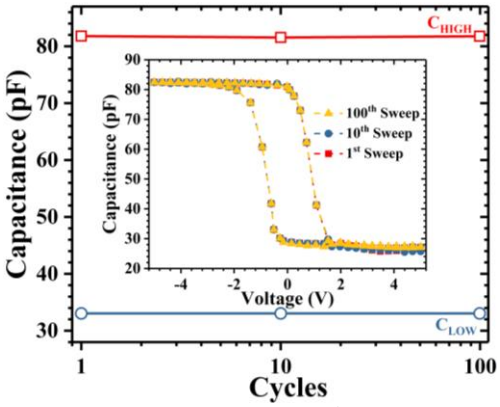

Fig. 5 Endurance (Cyclic C–V over number of cycles) measurements for 100 cycles on the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au NVFM structure. The inset shows the cyclic C–V measurements for 1st, 10th and 100th cyclic sweeps

accumulation capacitance at low frequencies. The above discussed observation with varying frequency may be due to different response time for the charges trapped/de–trapped at the NrGO layer [9]. The cyclic C–V measurements for the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au NVFM structure in Figure 2 shows rapid switching under low voltage operation, hence advantageous for memory applications.

The estimate of number of charge carries stored per unit area (N_{NrGO}) in the FG can be calculated using (1) [1, 2, 9, 15].

$$N_{NrGO} = \frac{\delta W \times \varepsilon_0 \times \varepsilon_{PMMA}}{q \times t_{PMMA}} \quad (1)$$

where, $\varepsilon_0, \varepsilon_{PMMA}, q, and\ t_{PMMA}$ are the permittivity of air, dielectric constant of PMMA, electronic charge and thickness of PMMA, respectively. Using equation (1), N_{NrGO} was found to be ~10^{12} cm^{-2} for an applied bias of 5 V and ~5 × 10^{11} cm^{-2} for 3 V of applied bias. The calculated density of state values, N_{NrGO} in the present investigations is in close proximity with the DOS for multilayer graphene ~10^{13} cm^{-2} eV^{-1} reported in literature [1, 2, 9, 15]. The difference between the calculated values of N_{NrGO} in the present case and DOS of multilayer graphene reported in literature may be attributed (i) suppression of DOS in NrGO as a result of functionalization [9, 15, 28, 38] (ii) lower dielectric constant of PMMA (ε_{PMMA} ~ 4) as compared with the high-k dielectrics used in literature (HfO_2, ε_{HfO_2} > 19, Al_2O_3 $\varepsilon_{Al_2O_3}$ ~ 9) [9, 15]. As discussed previously,

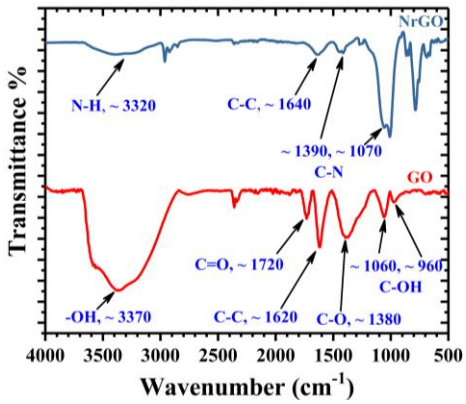

Fig. 6 FTIR absorption spectrum for GO and NrGO

TABLE I PERFORMANCE COMPARISON FOR VARIOUS NVFM STRUCTURES

NVFM Structures	Sweep Voltages (in V)	Memory Window (in V)	Retention (in s)	Gate Leakage Current Density (nA/cm^2) @ -1 V	Ref
TaN/Al_2O_3/rGO/SiO_2/p-Si	± 14	~ 3	10^8	-	[1]
	± 16	~ 5.8			
	± 18	~ 8			
	± 20	~ 9.4			
Au/Al/Ti/Al_2O_3/graphene/SiO_2/p-Si	± 7	~ 2	10^8	-	[2]
Au/Al/Ti/Al_2O_3/graphene/SiO_2/p-Si	± 7	~ 6			
TaN/Al_2O_3/few layer rGO/SiO_2/p-Si	± 8	~ 1.5	-	-	[7]
	± 10	~ 2.6			
	± 14	~ 4.2			
	± 18	~ 6.8			
Al/PMMA/NrGO/SiO_2/p-Si/Au	+ 3 to – 5	~ 2	10^5	20	[9]
	± 7	~ 3.3			
TaN/Al_2O_3/GO/SiO_2/p-Si	– 5 to 8	~ 2.2	-	-	[21]
	– 5 to 14	~ 7.5			
TaN/Al_2O_3/rGO/SiO_2/p-Si	± 4	~ 1.4			
Pt/HfAlO/CNT/HfAlO/p-Si	± 3	~ 0.4	10^4	-	[22]
Al/PMMA/NrGO/SiO_XN_Y/p-Si/Au	**± 3**	**~ 1.25**	**3× 10^{11}**	**10**	**This Work**
	± 5	**~ 2.6**			

in the present investigations, the aim was to propose a simple and low-cost approach demonstrating improved memory performances under low bias operations, maintain the interface of the FG with the underlying tunneling and top blocking layer. The measured |J| for the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au, NVFM structures at dc voltage of 10 V is ~18 nA/cm^2 shown in Figure 3. The significantly higher δW (~ 2.6 V) and lower |J| (10 nA/cm^2 @ – 1 V) is an indication of the enhanced reliability and feasibility for the use of Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au structure for NVFM applications [2].

For the real-world memory applications, its necessary to investigate the retention (C–T) and endurance characteristics of Al/PMMA/NGO/SiO_XN_Y/p–Si/Au NVFM structures, as shown in Figure 4 and Figure 5, respectively. For the retention evaluation, a write pulse of ± 5 V for 0.1 s is applied followed by read voltage close to V_{fb} (– 0.5 V). Here, the write pulse of – 5 V corresponds to high state capacitance (C_{HIGH}), the write pulse of + 5 V corresponds to low state capacitance (C_{LOW}). While, the mid capacitance (C_{MID}) = ((C_{HIGH} +C_{LOW})/2). As clearly noticed from the C–T characteristics that, initially for ~ 1000 s an exponential decay (rise) were observed for C_{HIGH} (C_{LOW}), and thereafter, till ~ 10^4 s the C_{HIGH} and C_{LOW} remains distinguishable (Figure 4). On extrapolating beyond 10^4 sec, it is observed that C_{HIGH} coincide with C_{MID} at ~ 3 × 10^{11} sec (inset of Figure 4) [15]. Hence, the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au, NVFM structure showed retention characteristics for ~ 3 × 10^{11} sec (approximately > 10 years). The observed retention in the present case is found to be significantly higher than the previously reported NVFMs utilizing GO, rGO, NrGO, CNT [1, 2, 7, 9, 21, 22].

Figure 5 shows the endurance (cyclic C–V, performed manually) measurements for the FG–NVFMs after 1st, 10th and 100th sweeps. For endurance measurements, the cyclic C–V sweeps were repeated for upto 100 cycles at a bias ± 5 V. While the C_{HIGH} and C_{LOW} states measured at – 0.5 V (V_{fb}). It is clear from the Figure 5, that as compared with the 1st C–V sweep, the devices behave robustly, showed stable and repeatable C–V characteristics even after 100th sweep cycles. Thus, the electrical characteristics on fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au structures demonstrate potential for its use in next generation NVFM operating at low operating voltages. The FTIR analysis for the GO and NrGO are presented in Figure 6. The FTIR spectra shows a sp^3 hybridized carbon (C–C) peak in GO at ~ 1620 cm^{-1} while sp^2 hybridized carbon peak in NrGO at ~ 1640 cm^{-1} shown in Figure 6. Additionally, for GO, the FTIR shows the presence of functional groups, hydroxyl (–OH), carbonyl (C=O), epoxy (C–O–C) and carboxyl (O=C–OH) at 3370, 1720, 1380, 1060 & 960 cm^{-1}, respectively [9, 33]. While, for NrGO, the presence of carbon–nitrogen (C–N) and nitrogen–hydrogen (N–H) absorption peaks at 1390 & 1070, 3320 cm^{-1}, respectively and negligible absorption peaks of other functional groups confirms the N doping and reduction in GO.

IV. CONCLUSIONS

In summary, here we demonstrated, cost–effective and easily controlled Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au structure for next generation NVFM applications. The use of NrGO is owing to the outstanding electronic properties and low dimensionality. The ultra-thin SiO_XN_Y helps in providing enhanced interface with Si, while, the uniform, stress free and low temperature processing advocates the use of PMMA. The electrical characterizations for the fabricated Al/PMMA/NrGO/SiO_XN_Y/p–Si/Au devices show large memory window, long term data retention under low applied voltage, minimal gate leakage current densities and stable endurance. It indicates that the demonstrated FG–NVFM structure can be employed for low–cost NVFM applications at low voltages. The advantages of the present approach is compatibility with the existing semiconductor processing while the low temperature solution processing opens a new direction

for organic electronics.

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