A Discrete-Time MOS Parametric Amplifier-Based Chopped Signal Demodulator

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***Abstract*— This article presents a discrete-time parametric amplifier (DTPA) as the signal demodulator for chopper amplifier. Unlike the conventional chopper, the DTPA demodulator features noise-efficient gain augmentation while demodulating the chopped signal. The demodulator also enables low-frequency noise cancellation during the inherent track-and-hold (T/H) process of the charge parametrization. The positive feedback loop and the dc servo loop are implemented for applications requiring larger input impedance and dc input offset cancellation using a bandpass transfer function. Design considerations for the DTPA-based demodulator circuit and the merits and demerits of the chopper–DTPA amplifier are discussed as well. The proposed design has been fabricated in a standard 180-nm CMOS technology node. The complete design occupies 0.127 mm^2 of the die area and consumes 2.4-μW power from a 1.5 V of V_{DD}. The measurement results show that the DTPA demodulator provides 8-dB gain enhancement while improving on the prior art of T/H-based demodulator and the amplifier achieves input referred noise voltage of 2 μV_{rms} in 143-Hz bandwidth.**

***Index Terms*— Chopping, discrete-time parametric amplifier (DTPA), low power, sensor interface, track-and-hold (T/H) demodulator.**

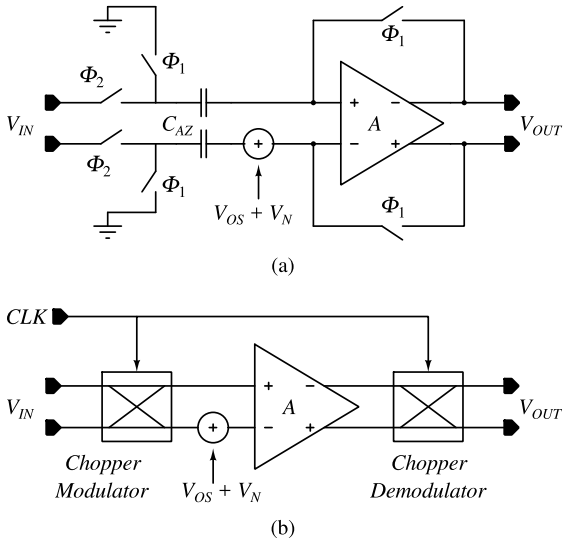

Fig. 1. Simplified block diagrams of the basic (a) auto-zeroed amplifier and (b) chopper amplifier.

I. Introduction

With the advancement of technology, concepts of mm-scale multi-sensory devices and Internet-of-Things (IoT) are gaining popularity [1], [2]. Front-end amplification is an important component of signal conditioning circuitry of environmental measurement, MEMS sensor, and biomedical data acquisition systems [3]–[5]. Typically, the signal that needs to be acquired in these systems is quite small, and it is superimposed on a comparatively larger dc common-mode signal. Moreover, the $1/f$ noise of MOS devices is dominant in this regime of operation. Therefore, low-noise and low-offset are vital requirements for the front-end amplifier to accurately quantify the signal of interest. Besides noise, low power dissipation with minimal area consumption is also a critical parameter for the amplifier. Usually, the design of front-end amplifier presents a tradeoff between the power consumption and the noise level since its current requirement is noise limited and seldom scales down with low data rate.

The dynamic offset cancellation techniques including auto-zero or chopper stabilization are often used to reduce low frequency noise [6]. As shown in Fig. 1(a), auto-zeroing is largely a switched-capacitor sampled-data technique. In the auto-zeroed amplifier, offset and noise are first sampled on a capacitor and later subtracted from the input signal during amplification. On contrary to the auto-zeroing, chopping is a continuous time method. As depicted in Fig. 1(b), the chopping technique circumvents the low frequency flicker noise by modulating the input to a higher frequency where only white noise exists. Design tradeoffs of these methods are well established in the literature [6], [7]. The input chopping is commonly preferred over the auto-zeroing method because, the later suffers from noise aliasing and requires larger area and power to fulfill the sample-and-hold noise constraint at the input. However, up modulated low-frequency noise appears as spurs/ripples at the output of the chopper amplifier. Therefore, chopping at both, the input and the output, requires additional filtering or ripple reduction techniques [8], [9] to treat the output ripples.

Variants of the amplifier which employ both, auto-zeroing and chopping techniques in a single front-end are also reported in [10]–[12] to alleviate the impediments of design tradeoffs.

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These designs utilize advantages of both the techniques to obtain low noise floor with ideally no output ripples. However, this method works on sampled data and the input signal is not processed during the sampling period. To achieve continuous-time operation, a ping-pong arrangement is required which uses two identical input stages to simultaneously auto-zero and amplify the input. The ping pong approach tends to considerably increase the circuit complexity and power consumption of the amplifier. Rather, a class of capacitively coupled chopper stabilized amplifiers have evolved as an attractive choice for various sensor interface systems due to their power efficiency, gain accuracy and ability to block dc offset at the amplifier input [13]–[15].

In multisensory multichannel IoT applications, resource sharing between interface circuit components is necessary for design optimization [16]. The circuit techniques that perform multiple tasks concurrently are particularly crucial for area-constrained portable applications. They can offer a degree of versatility to improve power and area efficiency of the system. However, it is observed that, the chopper switches in the amplifier only transpose the signal frequency and provide no contribution to the front-end amplification. This indeed motivates to explore the circuit which is as passive as the chopper, but enables noticeable gain enhancement during frequency translation. Further literature survey in the corresponding direction reveals use of a track-and-hold (T/H)-based demodulator by Bilotti and Monreal [17]. However, the voltage gain augmentation from the T/H demodulator is limited to 6 dB.

A demodulation technique using a discrete-time parametric amplifier (DTPA) is presented in this article. The proposed technique potentially provides >6 dB gain enhancement in the demodulator with contemporaneous down conversion of a chopped signal. The DTPA is inherently noise-efficient and consumes no static or bias current for frequency translation. Hence, combining the advantages of input chopping with interlaced T/H-and-boost type demodulation increases the gain, and reduces the output ripples without rigorous post filtering. Moreover, the DTPA demodulator aids in retaining the input impedance of the capacitively coupled chopper amplifier due to its capability of gain augmentation.

Operation of the chopper–DTPA amplifier is detailed in Section II. The design considerations for DTPA-based demodulation such as gain, linearity and noise are described in Section III. Implementation of the prototype chip and measurement results are presented in Section IV. Merits and demerits of the DTPA demodulator are discussed in Section V followed by conclusions in Section VI.

II. Chopper—DTPA Amplifier

Fig. 2 shows the top level architecture of the proposed chopper—DTPA amplifier. The amplifier consists of a capacitively coupled operational transconductance amplifier (OTA) with input chopping in the forward path, a large time constant OTA–C filter in the dc servo loop (DSL) and a capacitive positive feedback loop (PFL). A chopper demodulator of the conventional topology is replaced with the DTPAs and the controlling switches. At the demodulator stage, the DTPAs recover

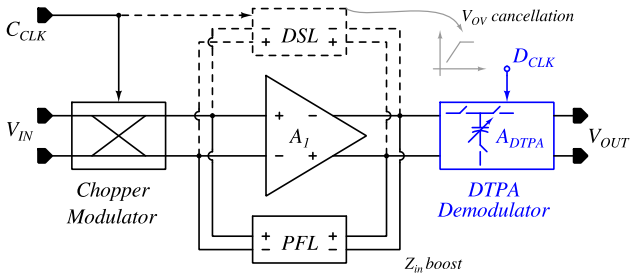


Fig. 2. Architectural block diagram of the proposed chopper stabilized amplifier with DTPA-based signal demodulator.

and amplify the input signal concurrently. The input buffers in this design bandlimit the noise spectrum to minimize aliasing and set the input common mode voltage required for inversion layer formation in the DTPA. As the DTPA is capable of driving only small ON-chip capacitive loads, the output buffers shield the DTPA gate voltage and provide its un-attenuated replica at the output. The input chopping tends to reduce the input impedance of the amplifier. Therefore, the PFL is used to boost the input impedance of the amplifier. Although this work concentrates on the demodulation technique, an optional DSL is implemented for applications where the amplifier is expected to receive a dc offset.

The circuit diagram of the forward path of the chopper—DTPA amplifier is shown in Fig. 3. The chopper works on a C_{CLK} whereas the demodulator operates on a D_{CLK}, which is derived from the C_{CLK}. The first order closed loop gain of the OTA is given as

$$A_{v,CL} = \frac{A_{v,OL} \cdot C_{\mathrm{in}}}{C_{\mathrm{in}} + A_{v,OL} \cdot C_f} \tag{1}$$

where $A_{v,OL}$, C_{in}, and C_f are open loop gain, input capacitance, and feedback capacitance of the OTA, respectively. Assuming $A_{v,OL} \cdot C_f \gg C_{\mathrm{in}}$ and capacitive loading of the OTA is negligible, the closed loop gain can be approximated to the ratio C_{in}/C_f.

As shown in Fig. 4(a), the proposed scheme incorporates T/H-and-boost functions in the signal demodulator. Down-conversion of only the positive output is exemplified for brevity. During $D_{C1} = 1$, the chopped input signal is tracked on the MOSCAP of DTPA_1 with the source–drain junction connected to 0 V. In the track phase, as depicted in Fig. 4(b), the input dependent gate charge of the MOSCAP due to formation of inversion layer (Q_I) can be represented using oxide capacitance (C_{ox})

$$\begin{aligned} Q_G \approx |Q_I| &= V_{\mathrm{IN}} \cdot C_{\mathrm{ox}} \\ &= (V_{\mathrm{CM}} + v_{\mathrm{in}}) \cdot C_{\mathrm{ox}}. \end{aligned} \tag{2}$$

When D_{C1} goes to 0, DTPA_1 is switched to the boost phase. In the boost phase, the source–drain junction is connected to V_{DD} and the gate remains floating until D_{C2} connects it to the output terminal. The switches with bubble notation are implemented using pMOS devices. During this period, V_{DD} attracts all the inversion charges from the channel. The gate charge is balanced by the charges in the body and the

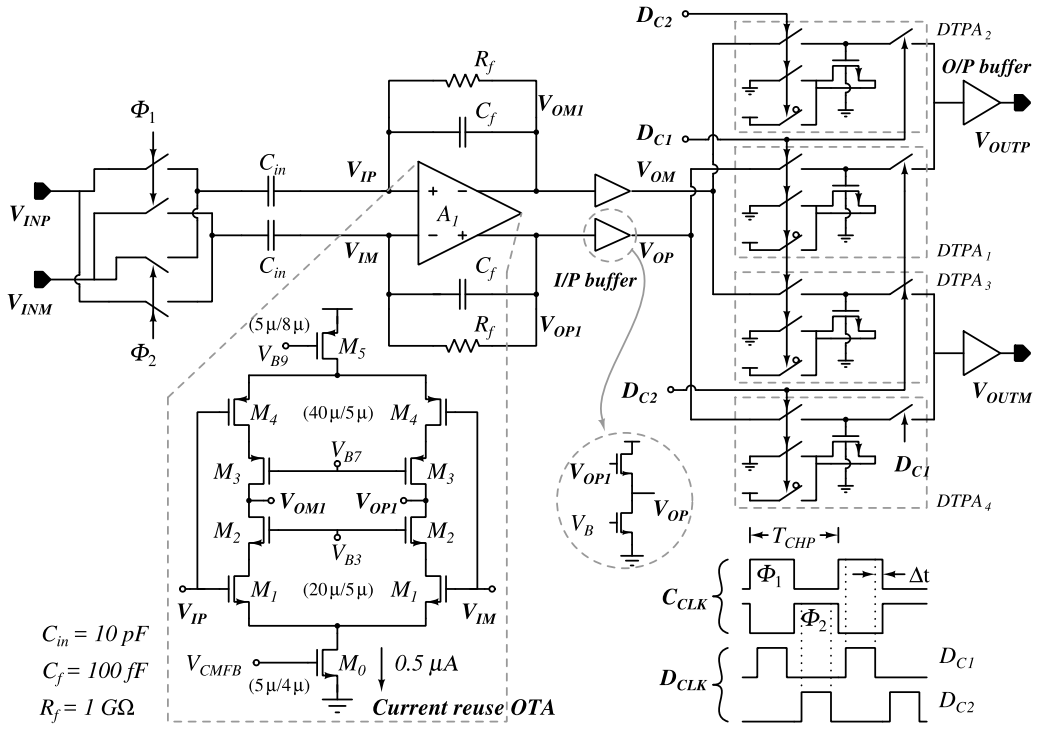


Fig. 3. Circuit implementation of the chopper—DTPA amplifier, the demodulator switching scheme and the clock timing diagram (bias circuitry generating V_{B3}, V_{B7}, and V_{B9}, and the CMFB for maintaining output common mode of the OTA are not shown here for simplicity).

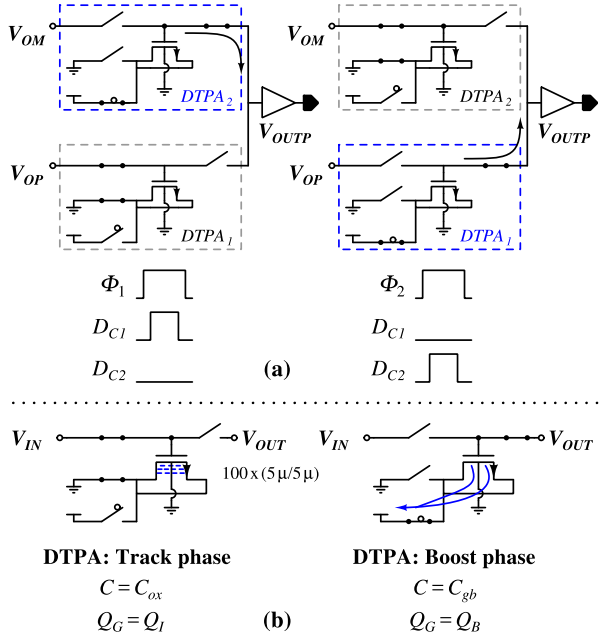


Fig. 4. (a) Working of the interlaced DTPAs in ϕ_1 and ϕ_2 clock periods and (b) principle of an nMOS DTPA: track and boost phases. In this design, the resulting capacitance of the MOSCAP in the track and boost phases are 12.2 and 3.6 pF, respectively.

effective gate-body capacitance (C_{gb}) becomes less than the gate-channel capacitance [18]. Therefore

$$Q_G = |Q_B| = V_{\text{OUT}} \cdot C_{\text{gb}} \tag{3}$$

where $C_{\text{gb}} < C_{\text{ox}}$. At this stage, since the gate charge is constant (gate is floating), the gate-body voltage rises to counteract decrease in the capacitance as per the charge conservation principle. From (2) and (3), the analytical expression of the boost factor which corresponds to the gain of a DTPA during the demodulation can be obtained as

$$\begin{aligned} V_{\text{IN}} \cdot C_{\text{ox}} &= V_{\text{OUT}} \cdot C_{\text{gb}} \\ A_{\text{DTPA}} &= \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{C_{\text{ox}}}{C_{\text{gb}}}. \end{aligned} \tag{4}$$

If C_{gp} is a parasitic capacitance associated with the gate of MOSCAP, then C_{gp} shares the gate charge during the boost phase and hence, the DTPA gain reduces to

$$A_{\text{DTPA}} = \frac{C_{\text{ox}} + C_{gp}}{C_{\text{gb}} + C_{gp}}. \tag{5}$$

As exemplified in Fig. 4(a), when $D_{C2} = 1$ in the phase ϕ_2 of C_{CLK}, the boosted signal gets connected to the output of the amplifier. Complementary D_{CLK} signals are used for DTPA_1 and DTPA_2 and hence, they take turns to generate the output signal. During each half cycle of C_{CLK}, one of the DTPAs works in the track phase whereas, the other operating in the boost phase provides the output. Because the output of the capacitively coupled amplifier changes sign after each $T_{\text{CHP}}/2$, the interlaced DTPAs demodulate the boosted input signal at the original frequency.

A. Capacitively Coupled Amplifier

Although this demodulation technique is not explicitly specific to the topology of the forward path OTA, the OTA design must satisfy low power and small area consumption requirements of multi-channel systems with optimal noise

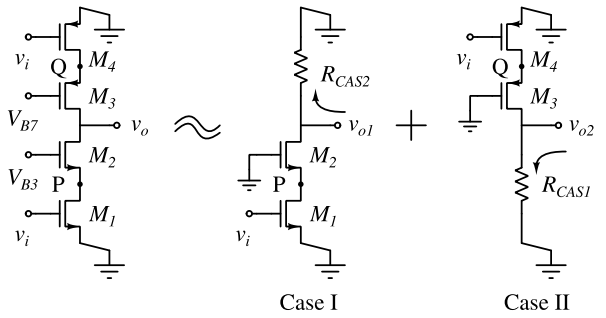


Fig. 5. Equivalent ac half circuit of the current reuse telescopic OTA. Cascode loads are assumed frequency independent for analyzing the frequency response using superposition.

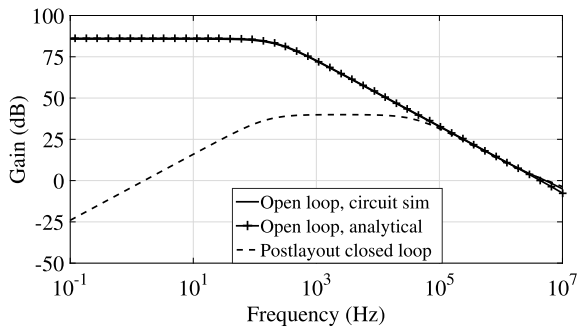


Fig. 6. Analytical and simulated open loop gain of the OTA A_1, and simulated closed loop response of the capacitively coupled OTA with $C_{\text{in}} = 10$ pF and $C_f = 100$ fF.

performance. The conventional two-stage, cascode and folded cascode architectures achieve low noise operation at the expense of high power, and are inefficient for area-constrained low power applications [19]. A current reuse telescopic cascode topology [20], as depicted in Fig. 3, is chosen for the main OTA.

The equivalent ac half circuit and the method used to derive frequency domain transfer function of the OTA are shown in Fig. 5. Frequency response of cascode load exhibits a high frequency pole-zero doublet whose location is independent of the load capacitance [21]. Therefore, cascode loads are replaced with their equivalent resistive components for analyzing the OTA using superposition. The simplified transfer function of the OTA obtained from ac small signal analysis of the two cases is given as

$$\begin{aligned}\frac{v_o}{v_i} &= \overbrace{-\frac{g_{m1}R_O}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}}^{\text{Case I}} \overbrace{-\frac{g_{m4}R_O}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p3}}\right)}}^{\text{Case II}} \\ &= -\frac{R_O\omega_{p1}\left[\omega_{p2}\omega_{p3}(g_{m1}+g_{m4})+s\left(g_{m1}\omega_{p2}+g_{m4}\omega_{p3}\right)\right]}{\left(s+\omega_{p1}\right)\left(s+\omega_{p2}\right)\left(s+\omega_{p3}\right)}\end{aligned} \tag{6}$$

where g_m and r_o are the transconductance and the output resistance of the respective transistors, and $R_O = R_{CAS1}||R_{CAS2}$ is the overall output resistance of the OTA such that $R_{CAS1} \approx g_{m2}r_{o2}r_{o1}$ and $R_{CAS2} \approx g_{m3}r_{o3}r_{o4}$. The locations of poles and zero are

$$\begin{aligned}\omega_{p1} &= \frac{1}{R_O \cdot C_L} \\ \omega_{p2} &= \frac{(g_{m2}r_{o1}+1)}{r_{o1}\cdot C_P} \approx \frac{g_{m2}}{C_P} \\ \omega_{p3} &= \frac{(g_{m3}r_{o4}+1)}{r_{o4}\cdot C_Q} \approx \frac{g_{m3}}{C_Q} \\ \omega_{z1} &= \frac{g_{m2}g_{m3}(g_{m1}+g_{m4})}{g_{m1}g_{m2}C_Q + g_{m3}g_{m4}C_P}\end{aligned}$$

where C_P and C_Q are the capacitances associated with the nodes P and Q, respectively while C_L is the load capacitance of the OTA. The transfer function given by Eq. (6) is numerically computed in MATLAB [22] and validated with circuit simulation. Fig. 6 confirms close agreement of the results in the frequency band of interest.

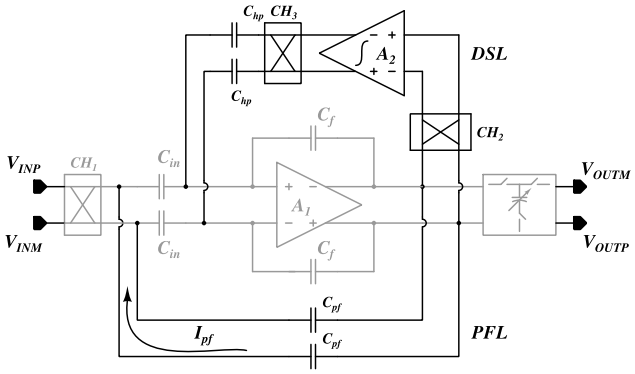


Fig. 7. Implementation of the positive feedback loop and the DSL. An external 1-μF capacitor is used in the integrator.

Simultaneous use of both, nMOS and pMOS as the input transistors increases transconductance of the OTA; thereby improving the bandwidth and noise performance. Assuming the intrinsic gain ($g_m \cdot r_o$) of transistors is much greater than 1, the simplified input referred thermal and $1/f$ noise voltages of the OTA can be obtained as

$$v_{n,th}^2 = \frac{16KT}{3(g_{m1}+g_{m4})} \cdot \Delta f \tag{7}$$

$$v_{n,1/f}^2 = \frac{2}{C_{\text{ox}}\Delta f (g_{m1}+g_{m4})^2}\left(\frac{K_n g_{m1}^2}{(WL)_1} + \frac{K_p g_{m4}^2}{(WL)_4}\right) \tag{8}$$

where K is the Boltzmann's constant, T is the absolute temperature, and K_n and K_p are the flicker noise constants of nMOS and pMOS, respectively. From (7) and (8), it can be inferred that designing $g_{m1} = g_{m4}$ can effectively reduce the input referred noise of the OTA by a factor of 0.707 without requiring additional current.

The simulated transconductance of the OTA is about 13 μS. The open loop dc gain of the designed amplifier is 88 dB which corresponds to 0.4% gain inaccuracy in the closed loop configuration. In this implementation, 40 dB $A_{v,CL}$ is designed with 10 pF and 100 fF metal-insulator-metal (MIM) type input and feedback capacitors while an off-chip feedback resistor sets the dc operating point for the capacitively coupled OTA. Fig. 6 exemplifies the simulated closed loop response of the OTA.

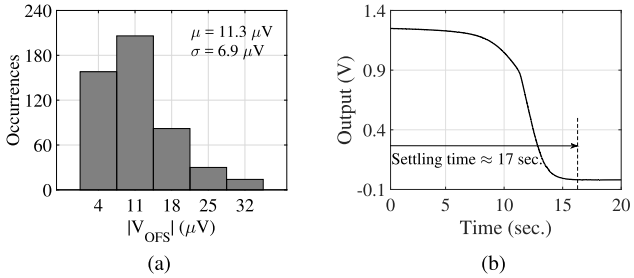


Fig. 8. (a) 500 run Monte Carlo simulation result for offset voltage and (b) settling time of the DSL.

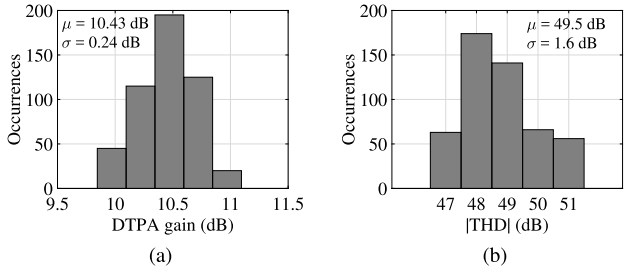


Fig. 9. 500 run Monte Carlo simulation results for (a) DTPA gain and (b) total harmonic distortion of the chopper–DTPA amplifier for 2 mV_{PP} signal.

B. Impedance Boosting and Optional DSL

A PFL and a DSL, as shown in Fig. 7, are employed around the amplifier for demonstrating their compatibility with the DTPA-based demodulation. The required input impedance of the amplifier may vary depending on the impedance of source/electrode. Typically, the input impedance $Z_{\text{in}} > 10$ MΩ is necessary to avoid input signal attenuation [23]. The modulator CH_1 in conjunction with the capacitance C_{in} reduces the amplifier's input impedance to a switched-capacitor resistor of value $1/2 \cdot f_{\text{CHP}} \cdot C_{\text{in}}$, which in this case is comparable to 10 MΩ at $f_{\text{CHP}} = 4$ kHz. The input impedance can be increased by reducing C_{in} and f_{CHP}. Nonetheless, it can reduce closed-loop gain of the ac coupled amplifier and increase noise [24]. Therefore, the amplifier requires input impedance boosting. Positive capacitive feedback is one of the techniques [14], [25], [26] to improve input impedance. In the PFL of this design, $C_{pf} = C_f$ is used to boost the input impedance of the amplifier, as reported in [14]. The simulated maximum input impedance of the amplifier is 96 MΩ.

dc offset at the amplifier's input gets up-modulated to chopping frequency and hence passed through the input capacitors. A servo loop is usually employed to cancel the dc input offset voltage which can otherwise saturate the amplifier output [14]. The DSL produces a high pass transfer function whose cut-off frequency is given by $f_{hp} = C_{hp} \cdot f_{u,\text{int}} / C_f$ where $f_{u,\text{int}}$ denotes the unity gain bandwidth (UGBW) of the G_m-C integrator. The UGBW of the integrator obtained from simulation is 58 mHz. Consequently, C_{hp} of 600 fF is opted in this design to get the high pass cut-off at approximately 350 mHz. The distribution of the input referred offset voltage is shown in Fig. 8(a). The mean and standard deviation are 11.3 μV and 6.9 μV, respectively. The settling behavior of the amplifier for 50 mV dc offset at the input is also simulated. As shown in Fig. 8(b), the saturated differential output voltage recovers in about 17 s; eliminating the effect of the external offset voltage.

III. DTPA Demodulator: Design Considerations

A. Gain and Linearity

In the chopper–DTPA design, nonlinear MOS Q-V characteristic is used as a parameter to achieve the voltage gain during the demodulation. Therefore, considering that the DTPA demodulator is more nonlinear as compared to conventional chopper and T/H based demodulators, Monte Carlo simulations are performed to analyze the effect of statistical mismatch on the gain spread of the DTPA and the linearity of the chopper–DTPA amplifier. The parasitic gate overlap capacitance loads the DTPA with smaller length [18]. This parasitic remains constant regardless of the gate length, and its loading effect reduces as the length increases. Therefore, 5-μm length is used for the DTPA. The DTPA area is chosen to minimize the gain mismatch in the two interlaced signal paths and avoid linearity degradation. The width is divided into smaller units and a large number of substrate contacts are placed around the capacitor to lower the resistance in the boost phase. The simulation results are shown in Fig. 9. Since change in the output voltage of a DTPA is less than the change of the area by the ratio of the gate parasitic capacitance to the total gate capacitance in the boost phase, statistical mismatch affects the gain distribution marginally. As can be seen from Fig. 9(a), standard deviation of the DTPA gain is only 0.24 dB from its mean value of 10.43 dB. Magnitude of the total harmonic distortion (THD) of the chopper–DTPA amplifier for 2-mV_{PP} input signal is shown in Fig. 9(b). As expected, the amplifier achieves moderate |THD| of about 50 dB with 1.6 dB of standard deviation. In addition to this, the results of statistical mismatch analysis carried out for all process corners are shown in Fig. 10. Mean values of the DTPA gain and the amplifier |THD| are in good agreement with the target values of 10 and 50 dB whereas, their respective standard deviation judiciously remain below 0.3 and 1.8 dB across all the corners.

Further to mismatch, another important aspect of the DTPA demodulator is that the gain augmentation is a function of the charge in the inversion layer. This charge depends on the gate potential and as a result, the gain becomes susceptible to the dc potential at the MOSCAP gate. Analysis of [27] suggests that the dc output in the boost phase shifts nonlinearly from its value in the track phase. Therefore, the simulated DTPA small signal gain for various input common mode voltages is studied in Fig. 11. At lower V_{CM}, the potential is not enough to create a strong inversion layer ($V_G < V_T$). Whereas at voltages above 510 mV, output of the DTPA saturates; leaving no headroom for small signal amplification. Based on these results, V_{CM} of the DTPA demodulator across process variations is maintained about 430 ± 25 mV using input buffers.

B. Demodulation Noise

In a DTPA, charge is parameterized to obtain signal amplification without degrading the signal-to-noise ratio [18]. However, the T/H mechanism in the DTPA-based demodulation process introduces switching noise. Using the analysis

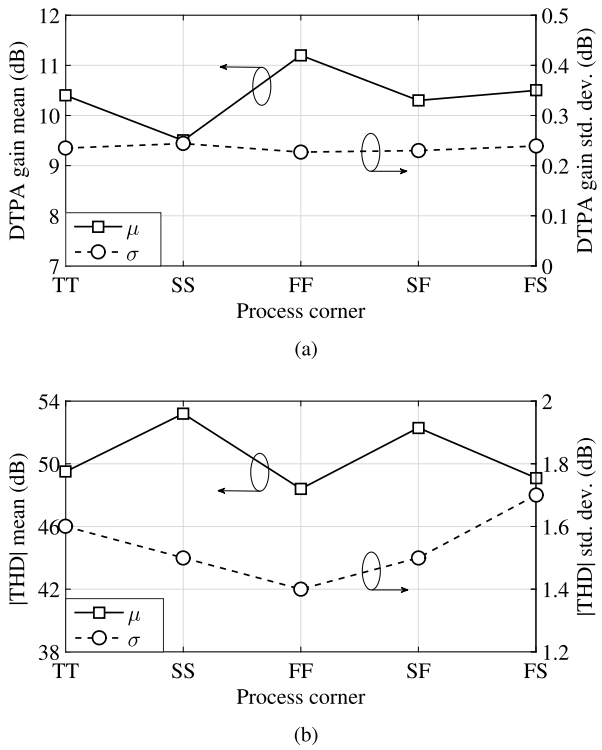


Fig. 10. Results of statistical mismatch analysis for (a) gain of the DTPA and (b) THD of the amplifier at various process corners.

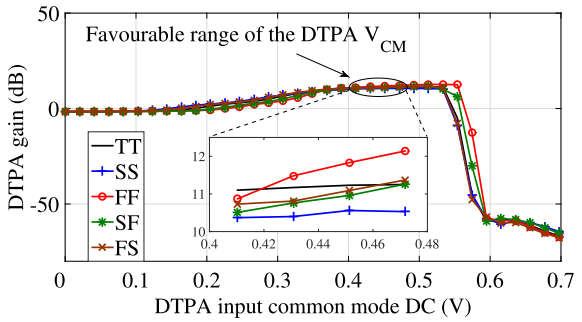


Fig. 11. Simulated DTPA gain with respect to V_{CM}; indicating favorable input common mode voltage range across various process corners.

of [17], the noise power spectral density (PSD) transfer function of a track-and-hold circuit for a frequency range of interest ($0 < f < f_{CHP}/2$) and noise spectrum bandwidth B can be written as

$$\left[\frac{\eta_o}{\eta_i}\right]_{f<\frac{f_{CHP}}{2}} = d^2\left[1+2\sum_{n=1}^{h}\text{sinc}^2(n\cdot d)\right] + (1-d)^2(1+2h)\text{sinc}^2\left[(1-d)\frac{f}{f_{CHP}}\right] \quad (9)$$

where η_i and η_o are input and output noise PSDs, d is duty cycle of the DTPA clock, h is the nearest integer to B/f_{CHP} and $f_{CHP} = 1/T_{CHP}$ is chopping frequency. Equation (9) suggests that noise aliasing occurs increasing the in-band noise density. Typically, $B > f_{CHP}$ is required in the design and noise

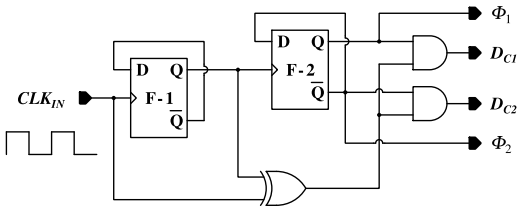


Fig. 12. Implementation of the clock generator circuit to obtain duty cycles of C_{CLK} (ϕ_1, ϕ_2) and D_{CLK} (D_{C1}, D_{C2}) as 50% and 25%, respectively.

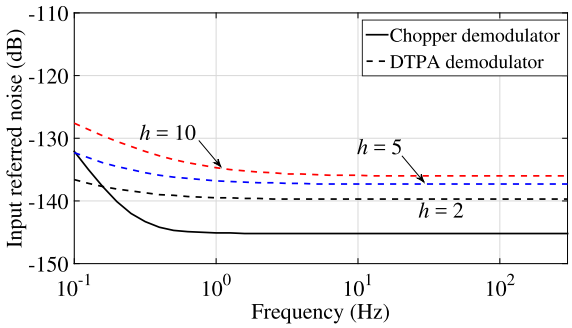


Fig. 13. Input referred noise spectral density of the chopper–DTPA and conventional chopper amplifiers.

is under sampled by the DTPA; causing fold over of high frequency noise into the signal band.

From the demodulation perspective, the two DTPAs (down-converting either V_{OP} or V_{OM}) receive equal but opposite polarity noise voltages. These voltages are added together at the demodulator output. For $f \ll f_{CHP}$, the DTPA outputs are correlated and hence the low frequency offset and noise voltages cancel each other. For the remaining spectrum, most of the noise components are because of aliasing and are uncorrelated. Therefore, their noise PSDs are summed at the demodulator output.

From (9) it can be noted that the noise in the worst case ($f = 0$) is maximum for $d = 0$. As shown in Fig. 12, the duty cycle of D_{CLK} is set to 25% for this design to sufficiently eliminate the switching transients. Fig. 13 shows the input referred noise of the amplifier with and without the DTPA demodulator. Expectedly, the contribution of aliasing to the thermal noise density of the chopper–DTPA amplifier increases with increment in h. This white-noise degradation can be reduced by optimally restricting the noise spectrum at the input of the DTPA demodulator. Accordingly, the -3 dB bandwidth of the source follower (input buffer) across the process variations is chosen in the range $4 \cdot f_{CHP} \sim 7 \cdot f_{CHP}$ to limit the T/H noise and faithfully recover the input signal.

C. PVT Worst Case

The amplifier design is analyzed at 135 process-voltage-temperature (PVT) corners using periodic ac (pac) and periodic noise (pnoise) simulations. Slow nMOS—slow pMOS (SS) corner operating at 1.35 V and -20 °C shows the worst performance. At this corner g_m reduces noticeably because of decrease in the bias current. The DTPA gain decreases while the input referred noise increases. The closed

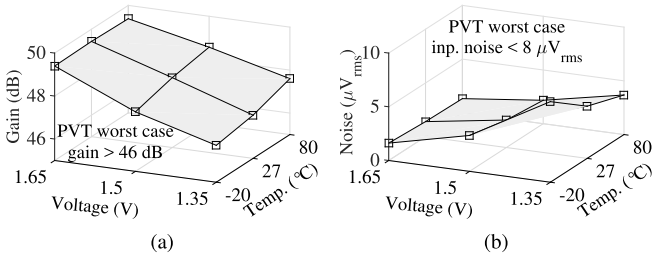


Fig. 14. (a) Gain and (b) input referred noise of the amplifier at SS corner for −20 °C to 80 °C temperature with V_{DD} varying from 1.35 to 1.65 V.

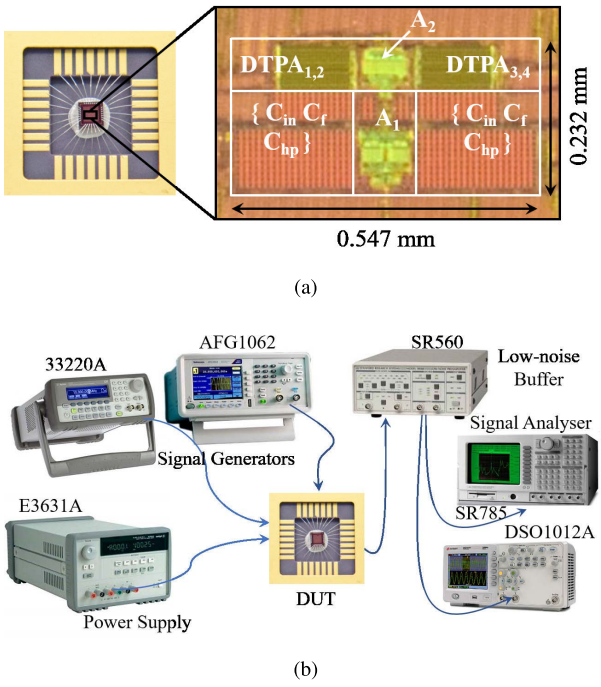


Fig. 15. (a) Microphotograph of the chopper–DTPA amplifier chip and (b) test setup for characterization. (Instrument pictures courtesy: company web pages and the authorized e-commerce web sites).

loop gain and the input referred noise voltage of the amplifier at SS corner for −20 °C to 80 °C and ±10% variation in V_{DD} from its nominal value (1.5 V in this design) are plotted in Fig. 14. It can be observed that the obtained noise and gain are within the target design margin of 10 μV_{rms} and 46 dB, respectively.

IV. The Measurement Results and Discussion

A test chip of the proposed design is fabricated in a standard 180-nm CMOS technology node. The complete design occupies 0.127 mm^2 of the chip. A micro-photograph of the chopper–DTPA amplifier along with the experimental test setup used for characterization of the chip is shown in Fig. 15. The design under test (DUT) is powered from 1.5 V of supply voltage using Agilent 3631A power supply. The chopper clock (ϕ_1, ϕ_2) and the DTPA clock (D_{C1}, D_{C2}) of 4 kHz frequency are derived from a single master clock (CLK_{IN}),

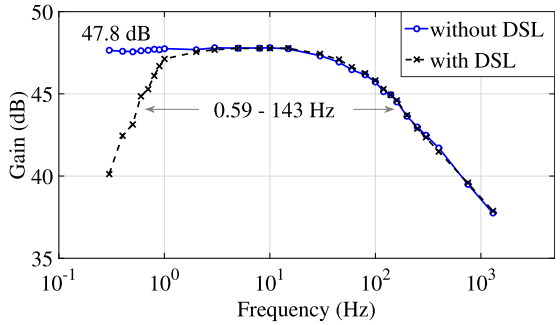


Fig. 16. Transfer characteristics of the amplifier with and without the DSL.

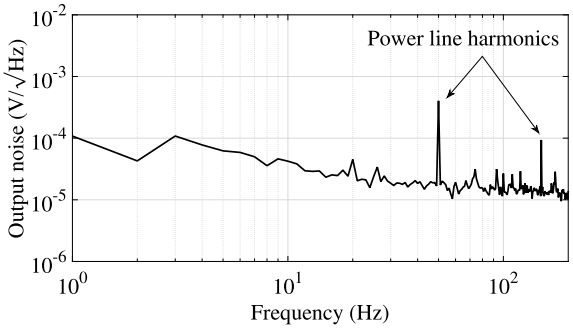
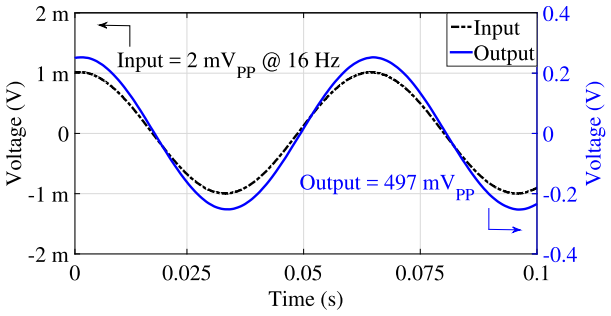


Fig. 17. Measured output noise power spectral density of the amplifier.

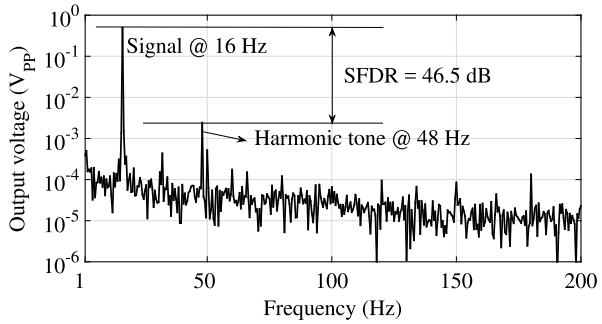
fed externally to the chip. The inputs are generated from Agilent 33220A and Tektronix AFG1062 signal generators. Stanford Research Systems (SRS) made low-noise voltage preamplifier SR560 buffers the output of the designed amplifier to enable correct measurement of low frequency data. The output waveforms are captured and analyzed using Agilent DSO1012A and SRS dynamic signal analyzer SR785 in time and frequency domains, respectively.

Transfer function is measured by applying a sinusoidal signal of different frequencies at the amplifier input. The transfer characteristics of the amplifier with and without the optional DSL are shown in Fig. 16. The amplifier achieves a maximum gain of 47.8 dB with 143-Hz bandwidth. This gain is 7.8 dB higher than the gain given by (1). It might be case that the presence of parasitic resistance in the signal path limits further gain enhancement by providing a dissipative route to the charge on the MOSCAPs. CMRR and PSRR of the amplifier at mid-band frequency are 70 and 63 dB, respectively. The −3-dB high pass cutoff frequency is obtained at 590 mHz when the DSL is enabled. The design consumes 1.2-μA current when the DSL is disabled and 1.6-μA current when it is connected in the circuit.

The noise performance of the designed amplifier is measured by shorting its input terminals to ground. Fig. 17 shows the low frequency noise spectral density measured at the output of the amplifier. 50-Hz power line harmonics are found contributing to the noise spectra and <40 $\mu V/\sqrt{Hz}$ thermal noise density is measured. The integrated equivalent input referred noise voltage in the amplifier bandwidth is calculated as 2 μV_{rms}; giving noise efficiency factor (NEF) [28]



(a)



(b)

Fig. 18. (a) Transient response and (b) output spectrum of the chopper-DTPA amplifier for 2 mV$_{PP}$, 16-Hz input signal.

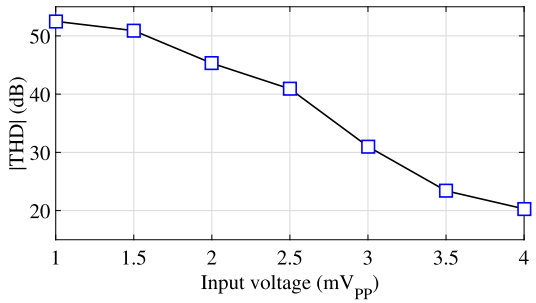


Fig. 19. THD of the amplifier with respect to varying input signal magnitude.

of 8.1. The obtained residual offset voltage of the amplifier is 28.4 μV. The T/H process simplifies removal of the amplifier's offset while the augmented gain from the DTPA demodulator reduces the effect of noise when referred to the input.

Time domain response of the amplifier to a 2 mV$_{PP}$, 16-Hz sinusoidal input signal plotted in Fig 18(a), and the corresponding output spectrum with 0.5% THD is shown in Fig. 18(b). Negligible delay in the output and low input noise density evidently confirm that the analysis presented in Section III-B optimizes the DTPA demodulator noise figure for less power dissipation in the source follower. The THD of the amplifier for different magnitudes of the input is shown in Fig. 19. The DTPA demodulator receives 100 times amplified chopped signals and therefore the MOSCAPs experience large signal swings at its gate. Hence, the THD of the amplifier degrades significantly due to nonlinearity introduced by the MOSCAPs, as the input goes beyond 2.25 mV$_{PP}$. The linearity is comparatively better for lower input signals.

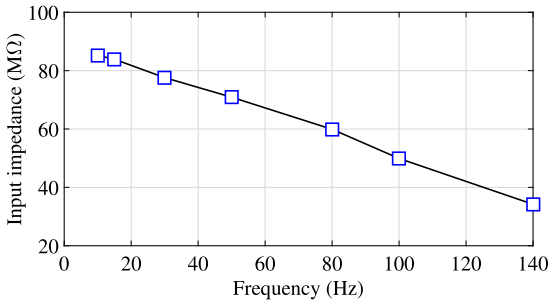


Fig. 20. Input impedance of the amplifier versus input signal frequency.

The input impedance is measured by forming a voltage divider between an OFF-chip resistor and the designed amplifier, and tapping out the voltage at the amplifier input. The measured low frequency input impedance of the amplifier with the PFL is 83 MΩ. Fig. 20 shows the input impedance plotted with respect to the input signal frequency. As anticipated, the value of Z_{in} decreases with the increase in frequency. However, since this article primarily focuses on the DTPA-based demodulation, no specific efforts other than the PFL were made to further improve the input impedance.

Table I compares the overall circuit performance with prior work employing various combinations of noise reduction techniques including chopper, auto-zero, correlated double sampling, etc. The proposed amplifier achieves significantly better NEF compared to [10], [11], [15]. Albeit the NEF of this design is reasonably higher than [12], the NEF of [12] excludes impedance boosting and DSLs which can have considerable effect on the current consumption and the noise performance.

Furthermore, performance of the designed amplifier with respect to capacitively coupled chopper amplifier having input chopper connected after and before the input capacitors [13], [14], input chopping with an open loop amplifier [24], chopping with frequency division multiplexing [30] and ac coupled bandpass amplifier [31] is summarized in Table II. The designs which focus on boosting the input impedance of the amplifier [26], [29] are also included in Table II. As can be seen from the table, this chopper–DTPA design achieves lower NEF compared to [13], [14], [31]; indicating that the design is optimized considering noise-power tradeoff. Muller *et al.* [24] shows lowest NEF among all but, the open loop gain stage causes channel-to-channel gain mismatch of 15% and degrades linearity down to 0.4% for an input signal as small as 1 mV$_{PP}$. The input impedance of the designed amplifier is on par compared to [14] and [24] because of lower input capacitance required by this design. Although Samiei and Hashemi [26], Chang *et al.* [29] have reported higher input impedance, they consume relatively more current.

In addition to aforementioned performance, multiple chips of the chopper amplifier with DTPA demodulator are measured to evaluate the design. The measurement results are shown in Fig. 21. The gain is approximately 8 dB higher than the closed loop gain of the capacitively coupled OTA with 0.7% variation. The input referred noise voltage varies from

TABLE I

PERFORMANCE COMPARISON WITH AMPLIFIERS EMPLOYING VARIOUS NOISE REDUCTION TECHNIQUES

Topology	Chopper-autozero		Chopper-CDS	Current mode	Chopper-DTPA
Reference	[10] VLSI Symp'05	[11] JSSC'10	[12] JSSC'10	[15] TCASII'18	This work
Tech (μm)	0.18	0.5	0.18-0.5	0.18	0.18
Supply voltage (V)	1	3-5.5	1.8-5	0.8	1.5
Supply current (μA)	500	1700	12.8	5*	1.6
f_{CHP}, f_{AZ} (kHz)	1000, 0.001	28, 14	500, –	2	4
-3 dB BW (Hz)	2 M	–	–	130	143
C_{in} (pF)/C_f (pF)	**80/2**	–	–	**1000/-**	**10/0.1**
Gain (dB)	**32**	**60**	**60**	**56**	**48**
Noise (nV/$\sqrt{}$Hz)	50	27	37	160	162
|THD| (dB)	52	–	–	–	45
NEF	**43***	**43.5***	**5.5**	**13.7**	**8.1**
PEF‡	1849	–	–	150.1	98.4
Area (mm^2)	0.88	2.5†	1.14†	0.03	0.127

* Estimated from the reported data † With pad ring ‡ PEF = NEF$^2\cdot$ V_{DD}

TABLE II

PERFORMANCE OF THE CHOPPER–DTPA AMPLIFIER WITH RESPECT TO REPORTED LOW FREQUENCY AMPLIFIERS

Reference	[13] JSSC'10	[14] JSSC'11	[24] JSSC'15	[29] TCASI'17	[26] SSCL'19	[30] JSSC'19	[31] TCASI'19	This work
Tech (μm)	0.18	0.065	0.065	0.13	0.18	0.13	0.13	0.18
Supply voltage (V)	1	1	0.5	1.225	1.2	1	2	1.5
Supply current (μA)	3.5	1.8	4.6	33.14	2.1	7.5	3.15§	1.6
Power (μW)	3.5	1.8	2.3	40.6	2.5	7.5	6.3	2.4$^\natural$
C_{in} (pF)/C_f (pF)	**1000/10**	**12/0.12**	–	–	–	**2/–**	–	**10/0.1**
Gain (dB)	**40**	**40**	**30**	**66-93**	**41-59**	**30**	**43-55**	**48**
Noise (μV_{rms}) in BW (Hz)	1.3 100	0.6 100	1.3 500	3.7 45.5	2 200	1.4 150	3.45 320	2 143
NEF	**9.3***	**14**†	**4.6**	**106***	**9.9**	**8.7**	**13.2**	**8.1**
PEF	86.5	196	10.6	13764	117.6	75.7	348.5	98.4
Linearity (%) @ V_{in} (mV_{PP})	– –	– –	0.4 1	0.4 0.6	1.7 1	55.5$^\flat$ 4	68$^\flat$ 6	0.5 2
Z_{in} (MΩ) @ f_{in} (Hz)	– –	**30** –	**28** **100**	**570** **50**	**500** **100**	– –	– –	**49** **100**
Area (mm^2)	0.3	0.1	0.025	0.183	0.08	0.039‡	0.6§	0.127

* Estimated from the reported data † With servo loop ON ‡ FDM demodulation is needed
$^\flat$ |THD| (dB) § IA + PGA + LPF + ADC $^\natural$ External output driver is used

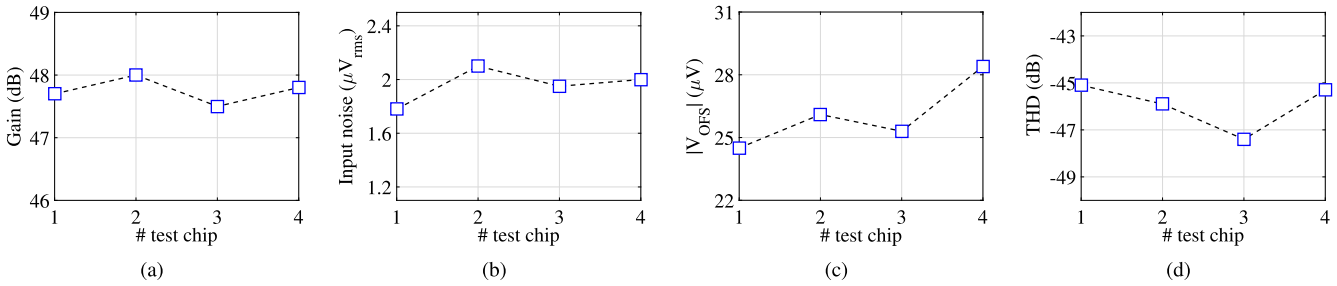


Fig. 21. (a) Gain, (b) input referred noise voltage, (c) input offset voltage, and (d) THD of four chopper-DTPA amplifier chips.

1.8 to 2.1 μV_{rms}, which confirms that the noise performance of the design is favorably within the budget of low-frequency sensing applications. The average magnitude of residual offset voltage is 26 μV. The THD for 2 mV_{PP} input is measured less than -45 dB (<0.5%) in all the chips, and it is acceptable considering the use of intrinsically nonlinear MOSCAP in the demodulator. To the best of authors' knowledge, this work is the first attempt to verify the use of MOSCAP based parametric amplification stage as the chopped signal demodulator. Merits and demerits of a typical DTPA-based demodulation of chopped signal are discussed in this section as a direction for its applicability.

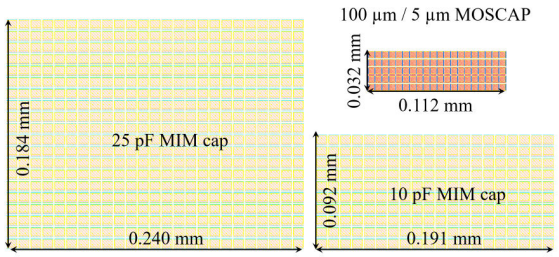


Fig. 22. Layout area of the DTPA MOSCAP in this design, 10 and 25 pF MIM capacitors.

V. Merits and Demerits of DTPA Demodulator

A. Merits

The experimental results confirm that the DTPA demodulator enables both, amplification and downconversion of a chopped signal, simultaneously. The parametric amplification in the demodulator is a noise-free process [18]. Compared to the T/H demodulator, this is of significance because the DTPA demodulator overpowers the T/H demodulator gain while contributing the same switching noise. Similar gain augmentation can be obtained with a conventional chopper demodulator followed by a closed-loop gain stage, but the DTPA demodulator has advantage of no static current consumption, compared to dc operating point and bias current requirements of the closed-loop gain stage. A comparison of 48-dB gain capacitively coupled chopped amplifier using the DTPA and the chopper demodulation is performed to investigate the effectiveness of DTPA demodulation in addition to the power-efficient gain enhancement. The comparison evidently reveals following benefits of the DTPA demodulator.

1) The chopper–DTPA design enhances the gain of capacitively coupled amplifier without decreasing the input impedance. The conventional chopper architecture on the other hand is bounded by tradeoff between closed loop gain, input impedance, and passive area. It can be observed from Table II that the chopper–DTPA amplifier attains 48 dB gain using just 10 pF C_{in} compared to 40-dB gain of [13] and [14] with C_{in} of 12 pF and 1 nF, respectively. From another viewpoint, this improves input impedance of the amplifier since a lower input capacitance achieves the required gain. As can be seen from Table III, the chopper–DTPA amplifier has an inherent advantage of higher input impedance.
2) *Area Efficient*: For the same 100 fF of feedback capacitor, the conventional topology requires 25 pF of input capacitor to provide 48-dB gain. Fig. 22 shows layout areas of the DTPA MOSCAP in this design, 10 pF and 25 pF MIM capacitors. Since, two MOSCAPs are needed for each of the two polarity outputs, as shown in Table III, the chopper–DTPA amplifier reduces the passive area by a factor of 1.8.
3) Spur free downconversion of the chopped signal: Incomplete cancellation of the output ripples remains an issue for the chopper demodulator. Extra ripple rejection loop [14] or spike filtering [8], [25] is required to obtain clean output signal. This leads to increased circuit complexity, area, and power consumption. Reportedly, the ripple rejection loop consumes at least 10% more power and adds 10% noise; degrading noise-power efficiency by 20% [32]. The DTPA demodulator simplifies the removal of residual output ripples owing to the T/H mechanism involved in the parametric amplification. Because offset and noise of the forward path OTA are not upmodulated, spurs are not generated at the DTPA demodulator output.

TABLE III
Performance Evaluation of 48 Decibel Gain Capacitively Coupled Chopped Amplifier Using the DTPA and the Chopper Demodulation With $C_f = 100$ Femto Farad

Parameter	Chopper demod.	DTPA demod.
C_{in} (pF)	25	10
C_{in} area (mm^2)	0.044	0.017
DTPA area (mm^2)	–	0.007
$Z_{in}^{\dagger}$ (MΩ)	5	12.5
|THD|‡ (dB) for 1 mV_{PP} input	55.5	54.7
|THD|‡ (dB) for 2 mV_{PP} input	53.2	49.5
Dedicated ripple rejection	Required	Not required

† $Z_{in} = \frac{1}{2 \cdot f_{CHP} \cdot C_{in}}$ ‡ Simulated mean value

B. Demerits

It is worthwhile to mention that the buffers used in this proof-of-concept implementation set the DTPA input common mode and shield the demodulator output from off-chip loading during characterization, as done in [18]. Although the buffers increase power, it is arguable to contemplate them as a limitation of the DTPA-based demodulation technique due to the following reasons. First, a complementary or double complementary MOS topology [33] can make the demodulator a weaker function of the input V_{CM}; alleviating the involvement of input buffer. And second, the practical scenarios of data acquisition typically comprise of an analog signal processing chain (amplification to analog-to-digital conversion) and the demodulator output need not to always see the external world.

The factual downsides of the DTPA demodulator are identified below for impartiality after having described its merits.

1) THD of the conventional chopper topology is driven by the forward path OTA whereas, for the DTPA demodulator the THD not only depends on the OTA but is also limited by nonlinear MOSCAP. From Table III, the THD of the amplifier with the DTPA and chopper demodulators are comparable for 1-mV_{PP} input. As the input magnitude increases, the nonlinearity due to MOSCAP starts to degrade the THD. In a certain outlook, there exists a tradeoff between the output linearity and the overall gain which eventually reduces the allowable input signal magnitude for this design.
2) The gain enhancement from the DTPA demodulator relies on the MOSCAP and its value in the different voltage-controlled operating regions, which are essentially PVT dependent. Therefore, variation in the gain of the DTPA is more as compared to that of the ratio-dependent closed-loop gain stage.

VI. Conclusion

A multivalent demodulation technique that utilizes merits of low-noise power-efficient DTPA for a chopper stabilized amplifier is introduced in this article. Interlaced DTPAs working on duty-cycled complementary clock pulses provide advantage of amplification during downconversion of the chopped signal. The chopper–DTPA amplifier embodies a positive feedback loop and a DSL to demonstrate high input impedance and dc offset cancellation compatibility, respectively. The amplifier design is validated using measurements of four prototype chips, fabricated in a standard 180-nm CMOS technology. The capacitively coupled amplifier wherein the ratio of input and feedback capacitors is set to obtain 40-dB gain, the amplifier actually enables 48-dB amplification, of which the extra 8 dB corresponds to the DTPA demodulator. Furthermore, the achieved 2-μV_{rms} input referred noise signifies low noise performance of the amplifier in low-frequency regime. However, due to increased nonlinearity of MOSCAP, the demodulator suffers from linearity degradation for a large output voltage swing. Therefore, in the case of capacitively coupled chopper amplifier, the DTPA demodulation is of potential use when the amplifier is expected to receive an input with low dynamic range and removal of chopping ripples is of concern along with the input impedance of the amplifier.

Acknowledgment

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