Digitally Assisted Secondary Switch-and-Compare Technique for a SAR ADC

Ashish Joshi, *Member, IEEE*, Hitesh Shrimali, *Senior Member, IEEE*, and Satinder Kumar Sharma, *Senior Member, IEEE*

***Abstract*—This brief presents a secondary switch-and-compare technique to improve the energy efficiency of a SAR ADC with minimal area and power overheads. The method exploits the self-calibrated comparator in the SAR ADC to generate a supplementary LSB. Instead of a C-DAC, this switching scheme produces voltage change required to evaluate the supplementary LSB at the calibration node of the comparator. The (N+1)th bit logic proficiently controls the secondary switching and assists the comparator in resolving the augmented LSB. A proof-of-concept (9+1)-bit 20 kS/s SAR ADC is designed in a standard 180 nm CMOS technology to demonstrate the proposed technique. The post-layout simulation results achieve energy efficiency of 51.2 fJ/conv.-step at 562 nW of average power consumption from V_{DD} of 1.8 V.**

***Index Terms*—Successive approximation, analog-to-digital converter, comparator offset, self-calibration, supplementary LSB, low power and multivalent circuit.**

I. Introduction

AMONG various analog-to-digital converter (ADC) architectures, a successive approximation register (SAR) ADC is popular choice for low to moderate speed data acquisition applications [1]–[4]. The conventional SAR ADC consists of a comparator, a capacitive digital-to-analog converter (C-DAC) and a SAR control logic circuit connected in a loop [5]. The DAC provides the reference voltages to the comparator for implementing the binary search (BS) while the SAR logic sets the direction of the search based on the comparator output in every clock-cycle [6]–[9]. The comparator essentially produces the binary data in successive comparisons and it is a crucial circuit component that largely decides performance of the ADC. However, the role of the comparator in the moderate resolution (8-12 bits) and several tens of kS/s SAR ADCs [1]–[3], [10]–[13] is limited to the quantisation of the sampled input with respect to the DAC-switched reference voltage.

A digitally assisted secondary switch-and-compare technique which exploits the comparator for augmented least significant bit (LSB) generation is introduced in this brief. The switching technique extends the functionality of the comparator to quantise the sampled input with respect to the DAC-independent reference voltage at its secondary input terminal. The design of (N+1)th-bit logic circuit is presented to efficiently reuse the calibration capacitor for the augmented bit evaluation. This multivalent utilisation of the comparator's secondary input stage and calibration capacitor achieves resolution increment without increasing the DAC size; thereby improving the area and energy efficiency of the converter.

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II. Illustration of the Proposed Concept

In an N-bit SAR ADC, the DAC voltage at the end-of-conversion (EOC) converges to the sampled input voltage within the ADC resolution ($V_{LSB,\ N}$) [5]. Thereafter, if a proportionate change of $V_{LSB,\ N}/2$ is established at the comparator's secondary input stage, then the comparator intrinsically generates an augmented LSB (the (N+1)th bit) in the next comparison.

Fig. 1 illustrates the concept for a single ended example case of N = 3 wherein, Fig. 1(a) shows the comparator with primary and secondary input stages used in the proposed method. Assuming that the most significant bit (MSB) and the (MSB-1)th bit are obtained as logic 1 after comparing the input sample with $\frac{V_{REF}}{2}$ and $\frac{3 \cdot V_{REF}}{4}$ respectively, Fig. 1(b) shows that the DAC voltage at the negative primary input is set to $\frac{7 \cdot V_{REF}}{8}$ prior to the third comparison. The secondary inputs are connected to a common-mode voltage, $V_{CM} = V_{REF}/2$ for first three comparisons. Considering the output of third comparison is also logic 1, the digital code after the DAC-switched successive approximation is 111. As shown in Fig. 1(c), this code implies that the input sample lies in the range $\frac{7 \cdot V_{REF}}{8}$ to V_{REF} where, $V_{REF} - \frac{7 \cdot V_{REF}}{8} = \frac{V_{REF}}{8} = V_{LSB,3}$ is the resolution of 3-bit ADC. Now as depicted in Fig. 1(c), voltage at the positive secondary input terminal is shifted to $V_{CM} - \frac{V_{REF}}{16}$, whereas voltages at the primary inputs remain unchanged. The comparator thus evaluates if the input lies in the upper or lower half of the third bit during the next clock-pulse; achieving 4-bit representation of the sampled signal.

As will be evident from the following sections, the secondary input stage is a versatile circuit component that cancels the comparator offset voltage and enables secondary switching to provide the augmented bit.

III. A-to-D Algorithm With Secondary Switching Embedded in the Comparator Offset Calibration

Block diagram of a fully differential (9+1)-bit proof-of-concept SAR ADC based on the secondary switching method and its corresponding conversion flowchart are depicted in

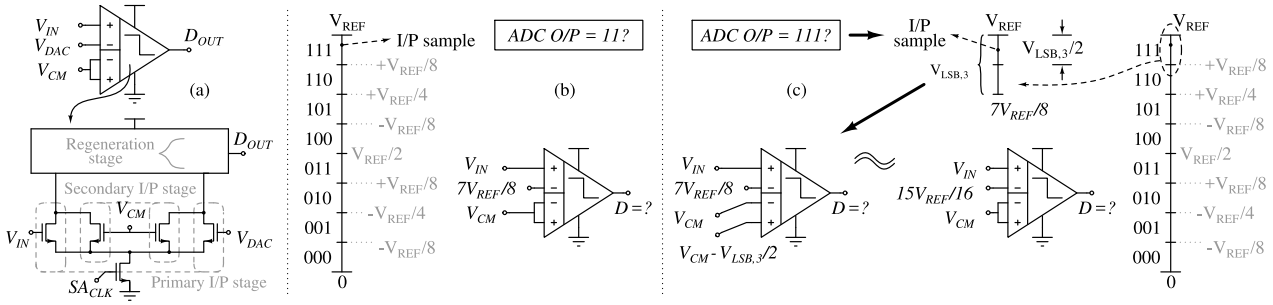


Fig. 1. (a) The comparator with primary and secondary input stages, (b) assuming the first two bits are obtained as logic 1, the comparator setting for calculating the LSB, (c) the secondary switch-and-compare technique: voltage at the secondary input is proportionally shifted to evaluate the augmented LSB.

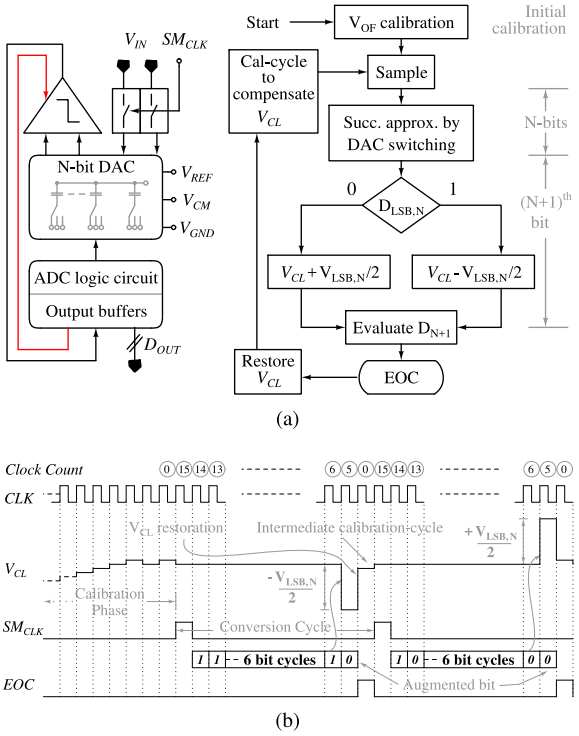


Fig. 2. (a) Top-level architecture and conversion flowchart of the ADC with the proposed switching technique, (b) the corresponding timing diagram.

Fig. 2(a). Initially, the comparator offset is calibrated as described in Section III-A. In the conversion phase, 12 clock cycles are required to output 10-bit data in each conversion-step. Counter-based digital control is opted due to its power efficiency in moderate speed SAR ADC designs [11]. The signal SM_{CLK} initiates the input sampling on the DAC capacitor bank. Bit-cycling is performed for the next 9 clock pulses to generate 9-bit digital code using the DAC switching.

The secondary switching method (Section III-B) inherently tunes the calibration voltage (V_{CL}) to obtain the augmented 10th bit. Once the augmented bit is generated, V_{CL} is restored and intermediate calibration-cycle is performed during the rising and falling edges of the *EOC* respectively. The timing diagram is exemplified in Fig. 2(b).

A. On-Chip Offset Calibration

In a SAR ADC design, the comparator offset is often considered as benign quantity since it is expected to equally affect each conversion-step. However, recent studies indicate that the comparator offset not only translates to an equivalent offset in the ADC transfer curve, but also leads to non-linearity in charge-shared SAR ADCs [4], [14] and therefore, requires calibration.

Fig. 3 shows circuit implementation of the comparator with on-chip switched-capacitor based self-calibration loop. The positive secondary input (gate of transistor M_3) is connected to a calibration capacitor C_{CL}, which is pre-charged to V_{CM}. The main architectural difference to calibration of [14] is placing a constant common-mode reference at the negative secondary input terminal to incorporate the proposed secondary switch-and-compare technique. During the calibration phase ($Cal = 1$), both the primary inputs are disconnected from the DAC and are shorted to V_{CM}. Charge is shared between the capacitors C_1 and C_{CL} based on the comparator output in each clock cycle. Assuming V_{CL0} is the voltage across C_{CL} in the k^{th} clock cycle, voltage across C_{CL} at the end of $(k+1)^{th}$ clock cycle is given by Eq. 1 if $V_{OP} = 0$ or Eq. 2 if $V_{OP} = 1$.

$$V_{CL} = V_{CL0} + \frac{C_1 \cdot (V_{DD} - V_{CL0})}{C_1 + C_{CL}} \tag{1}$$

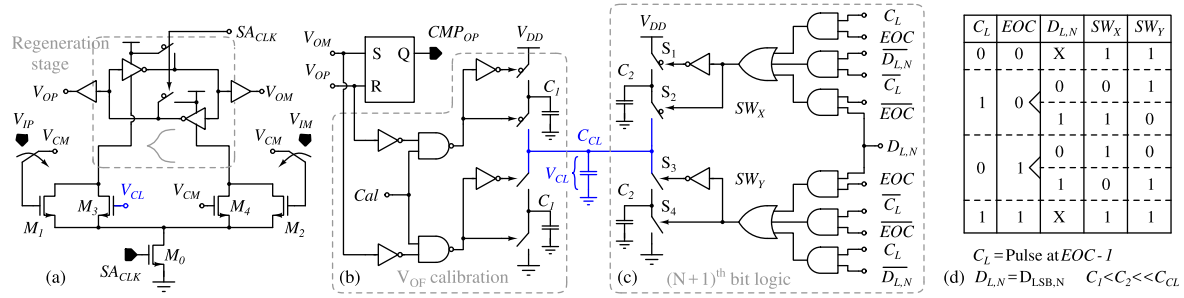
$$V_{CL} = V_{CL0} - \frac{C_1 \cdot V_{CL0}}{C_1 + C_{CL}} \tag{2}$$

This charge sharing continues until the self-calibration loop adjusts V_{CL} to compensate for offset voltage (V_{OF}), and the comparator starts producing alternate logic 1 and logic 0 outputs for sufficient clock cycles.

In the conversion phase ($Cal = 0$), the compensation current due to V_{CL} continues to flow through transistor M_3 of the comparator; resulting in cancellation of the offset voltage. The ratio $\frac{C_1}{C_1+C_{CL}}$ decides the residual offset voltage and noise on the calibration node. The smaller is the ratio, lower are the residual offset and noise. For a given clock frequency, leakage current dictates the minimum value of C_{CL} required to sustain V_{CL} for the entire conversion-cycle, while the maximum value is bounded by area and power consumption constraints.

B. Secondary Switching Procedure

Fig. 3 shows implementation of the secondary switching method for the augmented LSB generation. The same calibration capacitor used for offset cancellation is reused to produce $V_{LSB,N}/2$ voltage shift at the secondary input terminal. The digital circuitry in Fig. 3(c) also controls the switched capacitor network to undo the V_{CL} shift once the (N+1)th bit is generated. The completion of the DAC successive approximation (denoted by the signal C_L) triggers the secondary voltage



C_L	EOC	$D_{L,N}$	SW_X	SW_Y
0	0	X	1	1
1	0	0	0	1
		1	1	0
0	1	0	1	0
		1	0	1
1	1	X	1	1

Fig. 3. The comparator: (a) input and regeneration stages, (b) on-chip offset calibration circuit, (c) implementation of the secondary switching method to reuse the calibration capacitor (C_{CL}), and (d) corresponding switch control logic. Note that bubbled switches conduct when the controlling voltage is logic 0.

transition, whereas *EOC* triggers the opposite polarity voltage change for restoring V_{CL}. This logic is included as an integral part of the design since it does not require any off-chip signals.

It can be observed that there can be two cases for switching of C_{CL} to evaluate the (N+1)th bit.

1) $D_{LSB,\,N\,=\,0}$: In this case, switch S_2 is closed to proportionally charge C_{CL}. Positions of all the switches and the node voltages are shown in Fig. 4. The value of voltage shift, V_1, can be obtained as

$$V_1 = \frac{C_2 \cdot (V_{DD} - V_{CL})}{C_2 + C_{CL}}. \tag{3}$$

With this voltage change at secondary positive terminal, a comparison is made to obtain the (N+1)th bit. Then, switch S_2 is opened and switch S_3 is closed to restore V_{CL} by discharging C_{CL}. The corresponding voltage shift, V_2, can be calculated as

$$V_2 = \frac{-C_2 \cdot V_{CL1}}{C_2 + C_{CL}} = \frac{-C_2 \cdot (V_{CL} + V_1)}{C_2 + C_{CL}}. \tag{4}$$

2) $D_{LSB,\,N\,=\,1}$: In this case, the capacitor C_{CL} is first discharged for generating the (N+1)th bit and then charged during *EOC*, after the computation is made. The switching procedure is depicted in Fig. 4 and the respective voltage shifts are

$$V_1 = \frac{-C_2 \cdot V_{CL}}{C_2 + C_{CL}} \tag{5}$$

$$V_2 = \frac{C_2 \cdot (V_{DD} - V_{CL} - V_1)}{C_2 + C_{CL}} \tag{6}$$

Referring Eq. (3) to Eq. (6), it can be inferred that the voltage shifts depend on the value of V_{CL}. Unlike the DAC generated ratio-dependent reference voltage, the voltage transition at the positive secondary input represents only an approximate imitation of the reference voltage change required for evaluating the next bit. Hence, this switching procedure is termed as the secondary switch-and-compare technique and the comparison result is called the supplementary/augmented bit.

IV. Analysis of the Secondary Switching

A. Energy Consumption

The energy consumed in the (N+1)th bit generation circuit can be simplified as: $E_{(N+1)} = E_{cs} + E_{dig}$ where, E_{cs} is the total capacitor-switching energy and $E_{dig} \approx \sum C_{LD} \cdot V_{DD}^2 \cdot \gamma$, is the energy of digital circuit with C_{LD} and γ being the load capacitance of a logic gate and the probability of the gate

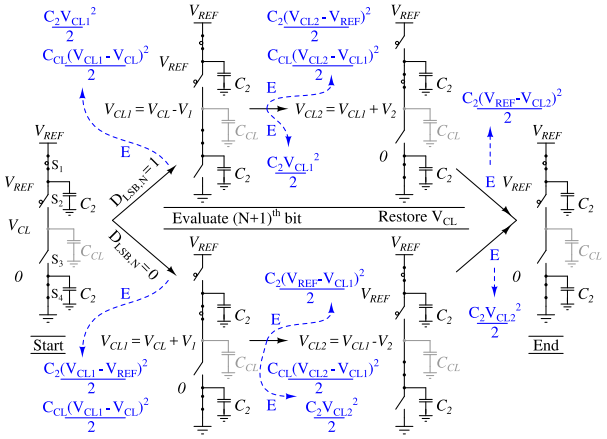


Fig. 4. Secondary switching procedure for augmented bit computation.

switching from logic 0 to logic 1. With initial condition that the source capacitor is charged to V_{DD} and the sink capacitor is discharged to ground, the capacitor-switching energy of the augmented bit generation (V_{CL} shift, V_{CL} restoration and completion of the secondary switching cycle) is step-wise shown in Fig. 4. Accordingly, the total capacitor-switching energies for the two cases explained in Section III-B are

$$E_{cs,1} = C_2[(V_{DD} - V_{CL1})^2 + V_{CL2}^2] + C_{CL}\left(\frac{V_{LSB,N}}{2}\right)^2 \tag{7}$$

$$E_{cs,2} = C_2[(V_{DD} - V_{CL2})^2 + V_{CL1}^2] + C_{CL}\left(\frac{V_{LSB,N}}{2}\right)^2 \tag{8}$$

Generally, $C_2 \ll C_{DAC}$ and according to the switching scheme, the logic gates switch only thrice in a conversion-cycle. Therefore, the total power consumed during the augmented bit generation is typically less compared to the overall comparator power.

With C as the unit capacitor, behavioral analysis is performed to quantify the energy efficiency of this method. 10-bit ADC cases are compared with a (9+1)-bit ADC where 9 bits are obtained from DAC switching and the extra 1-bit is evaluated using the secondary switching. $V_{CL} = V_{CM}$ is used, and $C_{CL} = 256\ C$ and $C_2 = C/2$ are chosen for the (9+1)-bit ADC with modified tri-level DAC switching method. As shown in Table I, the average switching energy in (9+1)-bit ADC is 50 % less compared to that of its 10-bit ADC counterpart [8]. Although capacitive areas of both the ADCs are approximately same, the (9+1)-bit ADC is area-efficient due to multi-functional use of C_{CL}.

TABLE I
SWITCHING ENERGY AND AREA EVALUATION FOR 10-BIT ADC

Ref.	E_{DAC} (CV^2_{REF})	Total diff. DAC size	C_{CL}	$E_{sec.}$ (CV^2_{REF})	Logic complexity
[6]	255.5	1024 C	–	–	Low
[7]	170.2	1024 C	–	–	Low
[8]	84.9	512 C	–	–	Low
(9+1)-bit†	42.4	256 C	256 C‡	0.25	Low

† This work with modified tri-level DAC switching ‡ $C_2 = C/2$

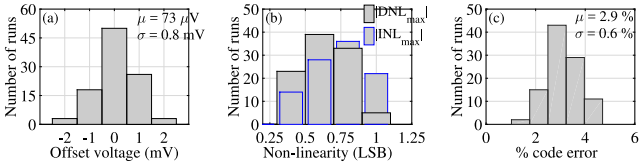


Fig. 5. Results of 100-run Monte Carlo analysis in a standard 180 nm CMOS technology: (a) calibrated offset voltage of the comparator, (b) DNL and INL, and (c) % code error for 2 LSB threshold value of the (9+1)-bit ADC.

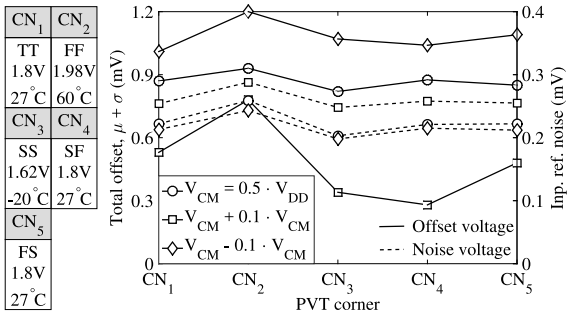


Fig. 6. Total offset voltage and input referred noise of the comparator at critical PVT corners with ± 10 % variation in V_{CM}.

B. Effect of Charging and Discharging Capacitor Mismatch

Practical design aspect of $V_{LSB,N}/2 \ll V_{CL}$ allows to neglect V_1 in Eq. 4 and Eq. 6, and also approximate the denominators of Eq. 3 to Eq. 6 as $C_2 + C_{CL} \approx C_{CL}$ for analysing the effect of mismatch on the voltage transitions. Moreover, by virtue of careful design, $V_{CL} \approx V_{CM}$ can be assumed for simplicity. Considering that the charging capacitor has maximum positive mismatch, ΔC_2, and the discharging capacitor has maximum negative mismatch, $-\Delta C_2$, the upward and downward voltage shifts can be written as $\frac{(C_2+\Delta C_2)\cdot V_{CM}}{C_{CL}}$ and $\frac{-(C_2-\Delta C_2)\cdot V_{CM}}{C_{CL}}$ respectively. Since the augmented bit calculation requires both upward and downward transitions, the error voltage, V_r, on the positive secondary input after one augmented bit generation cycle is

$$V_r = \frac{2 \cdot \Delta C_2 \cdot V_{CM}}{C_{CL}}. \tag{9}$$

As a mechanism to restrict the error voltage accumulation at the calibration node, a calibration-cycle is activated between two conversion-cycles. This intermediate calibration keeps V_{CL} relatively unchanged and effectively limits the comparator offset to the residual offset voltage.

C. The Augmented Bit Accuracy and ADC Linearity

Since the LSB generated from the DAC-switched output decides the direction of the secondary switching, the linearity and accuracy of the 10^{th} bit implicitly depends on the DAC. The employed tri-level DAC switching scheme, its energy efficiency, and minor dependence of the DAC on the accuracy of V_{CM} are detailed in [8]. However, selection criterion for the unit capacitor value is not discussed previously. This remaining information is presented here to optimise the DAC size while considering the capacitor mismatch.

Typically, the unit capacitor can be expressed with a nominal value of C and standard deviation of σ_C. For an N-bit fully differential SAR ADC with the chosen DAC switching scheme, worst-case DNL occurs when 2^{N-1} unit capacitors are switched in consecutive steps. Consequently, the standard deviation of the maximum DNL can be obtained as

$$\sigma_{DNL-max} = \frac{\sqrt{2^{N-1}} \cdot \sigma_C}{C}\ LSB. \tag{10}$$

MIM capacitor is commonly used to implement the C-DAC since it has low process variations, low temperature coefficient and good matching properties [15]. With reference to [1], mismatch of MIM capacitor having standard deviation of $\sigma(\Delta C/C)$ is modelled as

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_\sigma \sqrt{K_C}}{\sqrt{C}} \tag{11}$$

where, K_σ and K_C are the technology dependent matching coefficient and capacitor density parameter respectively. During the design, it is necessary to keep $3\sigma_{DNL-max} < 0.5 \cdot LSB$ for a high yield. Hence, a reasonable lower bound on the mismatch-limited unit capacitor can be calculated as

$$C = 18 \cdot (2^{N-1}) \cdot K_\sigma^2 \cdot K_C. \tag{12}$$

K_σ = 4 % and K_C = 1 fF/μm^2 in the chosen technology lead to the unit capacitor of approximately 15 fF. However, as per the design rules, the minimum value of the MIM capacitor is 17.8 fF. Therefore, C = 20 fF is used for the DAC. This selection of slightly higher C also serves to reduce the effect of parasitics associated with the routing metals. $C_2 = C/2$ is implemented as a series combination of two-unit capacitors while C_{CL} = 256 C closely satisfies the budgeted requirement of $< V_{LSB,N}/4$ change in V_{CL} for the simulated value of leakage current in < 100 pA range. As shown in Fig. 5(a), the standard deviation (σ) in the offset voltage of the comparator after 600 calibration-cycles in the initial V_{OF} calibration phase is 0.8 mV from its mean value (μ) of 73 μV. The input referred noise voltage obtained from Spectre pss/pnoise analysis in time-domain mode is 223 μV_{rms}. Furthermore, the results of PVT analysis performed with ± 10 % variation in V_{CM} are shown in Fig. 6. It can be seen that the total offset ($\mu + \sigma$) and noise voltages remain adequately low at critical PVT corners. The non-linearity errors subjected to the statistical mismatch are shown in Fig. 5(b). $\sigma(|DNL_{max}|)$ and $\sigma(|INL_{max}|)$ are 0.17 LSB and 0.22 LSB respectively. The distribution in Fig. 5(c) shows 2.9 % code error with 2 LSB threshold. As no conversion errors are observed above 4 LSBs, bit error rate of 5.62 e^{-6} is achieved with 90 % of confidence level for the bits > 4 LSBs.

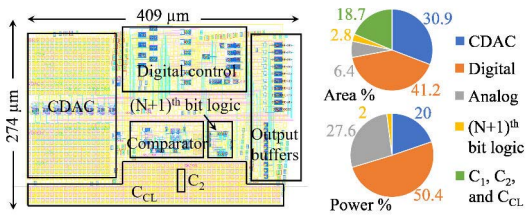


Fig. 7. The SAR ADC layout and component-wise area and power breakups.

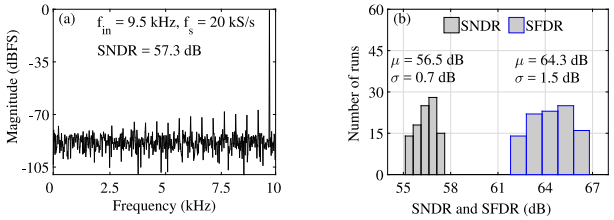


Fig. 8. (a)2^{10} points DFT of the ADC output, and (b) distribution of the ADC SNDR and SFDR from Monte Carlo simulation.

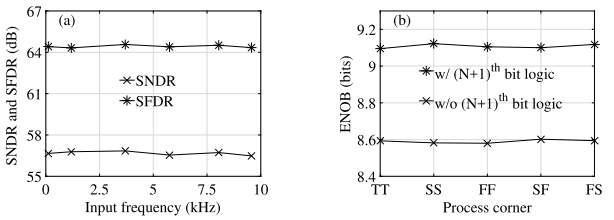


Fig. 9. (a) Mean value SNDR and SFDR versus input frequency, and (b) mean value ENOB across the process corners.

V. Post-Layout Simulation Results

Fig. 7 shows the ADC layout in a standard 180 nm CMOS technology. For post-layout dynamic performance with transient noise, Fig. 8(a) exemplifies the ADC output spectrum for near Nyquist full scale sinusoidal input. The SNDR obtained is 57.3 dB. Mismatch-dependent nature of V_{CL} limits the SNDR improvement in Monte Carlo simulation. As shown in Fig. 8(b), the mean value SNDR achieved is 56.5 dB ($\sim$ 9.1-bit ENOB). The SNDR and SFDR versus input frequency plot in Fig. 9(a) indicates that the secondary switching scheme embedded with the comparator offset calibration is independent of input signal frequency. Fig. 9(b) confirms that the proposed design is robust against the process variations.

Average power dissipation in the core ADC is 562 nW. The (N+1)th bit logic circuit consumes only 11 nW of the total power. The extra clock cycle to implement secondary switching is therefore justified for several moderate speed applications due to the low-power logic and high area efficiency of this method. The Walden figure of merit calculated using the mean value ENOB is 51.2 fJ/conv.-step. The FoM can be further improved by lowering V_{DD} of the SAR logic, as done in [1], and using contemporary DAC switching schemes, such as [9]. Table II substantiates the energy efficiency and usefulness of the proposed secondary switch-and-compare method.

VI. Conclusion

A digitally assisted secondary switching scheme for obtaining a supplementary (N+1)th bit from an N-bit SAR ADC has been reported. In this multivalent technique, N bits are resolved by successively switching the DAC capacitors, and the augmented bit is computed by switching the calibration capacitor through a logic circuit which has intelligent control over the calibration voltage change. Reuse of the calibration capacitor and low-power simple-to-implement (N+1)th bit logic are the features of this method which contribute to the improvement in energy and area efficiency of the converter.

TABLE II
Performance Summary of the ADC

Reference	Tech (μm)	V_{DD} (V)	f_s (kS/s)	ENOB (bits)	Power (μW)	FoM (fJ/conv.)
[1]	0.13	1	1	9.1	0.072	129.4
[2]*	0.18	1	1	9.1	0.043	73
[3]	0.18	1.8	1	9.05	0.09	171
[11]	0.18	1.1	10	7.4	0.127	63.4
This work†	0.18	1.8	20	9.1‡	0.562	51.2

* Sim. result † Post-layout sim. result ‡ Mean value

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