Manoj K Yadav¹, Arnab Mondal¹, Satinder K Sharma¹, and Ankush Bag^{1a)}

¹School of Computing & Electrical Engineering, Indian Institute of Technology Mandi, Mandi, H.P. India

a) Electronic mail: bag.ankush@gmail.com

Sapphire and gallium oxide have been used as substrates for most of the reported results on β -Ga₂O₃ devices. However, silicon (Si) is an abundant material on the Earth leading to easier and low-cost availability of this substrate along with higher thermal conductivity which makes Si a promising and potential substrate candidate for rapid commercialization. Therefore, in order to strengthen the feasibility of Ga₂O₃ on Si integration technology, we have deposited β -Ga₂O₃ on (100) and (111) oriented p-Si substrates using pulsed laser deposition (PLD) technique. A single-phase (β) and polycrystalline nature of the β -Ga₂O₃ film is observed for both samples using XRD. A low RMS roughness of 3.62 nm has been measured for Ga₂O₃/Si(100), as compared to 5.43 nm of Ga₂O₃/Si(111) using AFM. Moreover, $Ga_2O_3/Si(100)$ shows a smoother and uniform surface of the Ga_2O_3 film, whereas $Ga_2O_3/Si(111)$ seems to have a rougher surface with pits like defects. It might be due to the hexagonal projection of Si (111) that is not suitable for obtaining a good tilted-cuboid or monoclinic Ga₂O₃ crystal unlike the rectangle projection of Si (100). The electrical parameters of the fabricated Schottky barrier diodes (SBDs) were extracted using current-voltage (I-V) and capacitance-voltage (C-V) characteristics. The polycrystalline Ga₂O₃ film on Si(100) leads to fewer defects emerging from the Ga₂O₃/Si heterointerface due to the close symmetry of Ga₂O₃ and Si(100) crystal with rectangle projections unlike Ga₂O₃ on Si(111). These less number of defects eventually lead to better diode performance of Ga₂O₃/Si(100) where we have observed typical thermionic dominating carrier transport, whereas defect-assisted thermionic field emission has been the primary carrier transport mechanism in $Ga_2O_3/Si(111)$. Hence, Si (100) substrate is demonstrated to be a better and potential platform for Ga₂O₃ devices than Si (111).



I. INTRODUCTION

Recently, gallium oxide (Ga₂O₃) has attracted wide attention for the next generation of high efficiency and high power devices by virtue of its attractive material properties ^{1,2}. Ga₂O₃ material has five different polymorphs, namely α , β , γ , δ , and ε , among which β is the most thermodynamically stable and well-studied phase³. It has an extremely wide-bandgap in the range of (4.4 - 4.9 eV) ²⁻⁵, and a large theoretical breakdown electric field of about 8MV/cm ^{4,5} compared to the traditional silicon (Si) and later developed silicon carbide (SiC) ⁶, and gallium nitride (GaN) ^{7,8} semiconductor materials. The large bandgap of Ga₂O₃ allows it to operate at high temperatures and high breakdown field permits it to operate at high voltages. Because of these superior properties of Ga₂O₃, Baliga's Figure of Merit (FOM) is very large (3444) compared to other wide-bandgap semiconductors, claiming its transcendency as power device semiconductors. It carries the obvious potential to surpass SiC and GaN, not only in view of power device performances but also in terms of cost-effectiveness. These advantages of Ga₂O₃ demonstrate its ability to be a potential material for high power electronics as well as high-temperature environment electronics⁹.

Although significantly rapid progress is going on in β -Ga₂O₃ research currently, an ample amount of effort is still required to improve the performance of power devices and commercialize it. In this context, Farzana *et al.*¹⁰ have reported the influence of metal choice on Ga₂O₃ Schottky barrier diodes (SBDs) properties. They have investigated the current transport nature for the different SBDs and selection of the metal on Ga₂O₃ for best Schottky contact. Yao *et al.*¹¹ had also investigated the electrical behaviour of the Ga₂O₃ SBDs fabricated using different metals. Sasaki *et al.*¹² have fabricated the vertical Ga₂O₃ SBDs using a single-crystal β -Ga₂O₃ substrate. The ideality factor was very close to unity, and the barrier height of 1.46 eV was obtained for the vertical SBDs. The temperature dependence electrical characteristics of the vertical Ni/Au/Ga₂O₃ and Pt/Au/Ga₂O₃ SBDs based on β -Ga₂O₃ single crystal substrate, and they have also shown the temperature-dependent electrical characteristics. Although most of the researchers are using Ga₂O₃¹⁵ as a substrate to fabricate the Ga₂O₃ SBDs, also there are many other

4



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materials, such as Al₂O₃¹⁶, GaN ¹⁷, GaAs ¹⁸, and CoGa ¹⁹ have been used as a substrate material for Ga₂O₃ film growth. However, these substrates make the technology too expensive for rapid commercialization. Therefore, we have tried to explore the potential of the most inexpensive substrate, i.e., silicon for Ga₂O₃ devices. Another strong reason for finding Si as a likely substrate replacing bulk Ga₂O₃ is the higher thermal conductivity of Si (1.5 W/cm.K) than Ga₂O₃ (0.1 – 0.3 W/cm.K).

There are few reports on the growth of Ga₂O₃ on a silicon substrate ^{20–24} for high power applications, which could play an essential role in the integration of these power devices with the matured Si integrated circuit technology. *Zhang et al.*²² have been fabricated the p-Si/n-Ga₂O₃:N_b heterojunctions using sputtering. They have shown the effect of annealing and N_b on the electrical properties of heterojunction. *Altuntas et al.*²³ have been deposited the Ga₂O₃ on Si (111) substrate using plasmaenhanced atomic layer deposition technique (PEALD). The values of ideality factor, barrier height, and series resistance were obtained to be 1.93, 0.95 eV, and 3.1 k Ω respectively for Al/Ga₂O₃/Si diode. Therefore, the integration of Ga₂O₃ with a well-established and cost-effective Si substrate is a good approach for next-generation power devices. All these reports are showing the electrical performance of the Ga₂O₃ devices on Si substrates. However, the choice of the appropriate orientation of Si substrate for Ga₂O₃ SBDs in regard of high-power devices have not been studied yet.

Therefore, in order to strengthen the feasibility of Ga₂O₃ on Si integration technology, we report presently on the deposition of ~ 110 nm β -Ga₂O₃ film on two differently oriented p-Si substrates using pulsed laser deposition (PLD) technique. Gold (Au) metal is sputtered to form the Schottky contacts. The main electrical parameters have been extracted from the forward current-voltage (I-V) and capacitance-voltage (C-V) characteristics for both the SBDs.

II. DEVICE STRUCTURE AND FABRICATION

Gallium oxide pellet as a target for PLD (pulse laser deposition) was made from the gallium oxide powder purchased from the Sigma Aldrich Company. The gallium oxide powder purity was 99.999%. The obtained pellet was kept inside the furnace at 1200 °C for 24 hours. After the preparation of the

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 Ga_2O_3 pellet, it was loaded into the deposition chamber of the PLD system and kept under the vacuum of ~5×10⁻⁸ mbar. Prior to the film deposition, p-Si (100) and p-Si (111) wafers have been cleaned with standard RCA cleaning procedure, after that HF (hydrofluoric) acid treatment has been done to remove the remaining oxide layer from the wafers.

First, the Ga₂O₃ film was deposited on p-Si (100) substrate using PLD, and the sample was named as G1. For the sample G1, the substrate temperature was kept at 635°C during deposition, and the processing pressure of the chamber was 0.003 mbar. The frequency of the laser, pulse energy density, and deposition time duration were fixed at 5 Hz, 200 mJ/cm², and 35 minutes respectively. After the deposition of the first sample, p-Si (111) substrate was loaded into the sample holder inside the PLD chamber. Now, the Ga₂O₃ has been deposited on the Si (111) substrate using PLD, and the sample was named as G2. All the deposition parameters for the sample G2 were same as G1. Thus, only there was a change in the Si substrate orientation.

Ohmic contacts or cathode electrodes were formed on the backside of all the samples by evaporation of the Aluminum (Al). The deposition pressure of the thermal evaporator was kept at 2×10^{-6} mbar. Further, the samples were annealed at 265 °C for 2 min under the vacuum environment to improve the ohmic behavior of the contacts. Then, Au metal was sputtered on the top of the samples to form the Schottky contacts or anode electrodes. The base pressure and the processing pressure of the sputtering chamber were maintained at 5.2×10^{-6} mbar and 3.4×10^{-3} mbar, respectively. Anode electrodes for both the samples were circular, with an area of 0.000565 cm². Fig. 1 depicts the cross-section schematics of fabricated device structures for both samples.

The material characterizations of all the samples were done by x-ray diffraction (XRD: Smart lab, Rigaku Japan) equipped with a Cu-K α radiation source. Both plane view and cross-sectional morphology of the samples were characterized by field-emission scanning electron microscope (FESEM, Nova Nano-SEM 450, FEI, USA). The electrical characteristics of the diodes were measured using the Keithley 4200 semiconductor measuring unit (SMU) at room temperature (~300 K).



Fig 1. Cross-sectional schematic illustration of the fabricated devices.

III. RESULTS AND DISCUSSIONS

The crystal orientations of the deposited thin films for both the samples have been obtained by the XRD instrument, as shown in Fig. 2. All the diffraction peaks in the patterns may be attributed to the monoclinic structured β -Ga₂O₃. All the obtained diffraction peaks and corresponding planes of the Ga₂O₃ are mentioned in the XRD pattern. The peaks (20) of the gallium oxide were at 18.95°, 30.29°, 38.33, 44.32, 58.02° and 64.51° and the corresponding planes were (-201), (110), (-402), (601), (-603) and (-221), respectively. The obtained diffraction peaks are in good agreement with the reported peaks of Ga₂O₃ with β -phase ^{5,25}. The diffraction peaks (20) of Si (111) and Si (100) substrates were obtained at 28.30° and 69.34°, respectively. XRD patterns of β -Ga₂O₃ films reveal the polycrystalline nature on both Si (100) and Si (111) substrates. The similar crystalline quality of Ga₂O₃ films grown on (100) and (111) substrates using PLD is also confirmed by Berencén et al. ²⁵. It is difficult to get good crystalline quality of Ga₂O₃ on Si substrates. Dakhel *el al.* ²⁶ have grown Ga₂O₃ film on Si substrate, and the XRD pattern shows the amorphous structure. They have concluded that the substrate temperature is the most crucial for the growth of crystalline Ga₂O₃ films. Moreover, Kim et al. ²⁷ have grown the amorphous Ga₂O₃ films on Si (100) substrates, XRD confirms the amorphous nature of the films.

Fig. 3 (a) and 3 (b) shows the top view field emission scanning electron microscope (FESEM) images of the β -Ga₂O₃ films grown on (100)- and (111)- Si substrates. The images of all the samples were taken

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at $5\times5 \ \mu\text{m}^2$ area. Sample G1 shows the smooth and uniform surface of the Ga₂O₃ film, whereas G2 seems to have a rougher surface with pits like defects. It might be due to the hexagonal projection of Si (111) that is not suitable for obtaining a good monoclinic Ga₂O₃ crystal. Whereas, the similarity of tilted cubic crystal structure on cubic Si (100) may be suitable for obtaining good monoclinic β - Ga₂O₃ crystal ²⁸. The cross-sectional FESEM images of Ga₂O₃ films were also obtained for both the samples, as shown in fig. 3(c) and 3(d). The Ga₂O₃ film thicknesses of ~116 nm, and ~110 nm, were obtained for the samples G1 and G2, respectively. The topology of the samples G1 and G2 has been determined using the atomic force microscope (AFM) technique. The AFM images of the sample G1 and G2 are shown in Fig. 3 (e) and 3 (f) respectively. The root mean square (RMS) roughness (R_q) of the Ga₂O₃ surface was measured to be 3.62 nm, and 5.43 nm for the sample G1 and G2 respectively.

Although, n-Ga₂O₃/p-Si heterojunction has been used to fabricate SBDs, hence, there is a possibility of two back-to-back diodes in the structure. However, the non-existence of back to back diode in the n-Ga₂O₃/p-Si heterojunction has been already obtained in the previous work 29 .



Fig. 2. XRD patterns of the β -Ga₂O₃ films for the samples G1, and G2. XRD pattern of both the samples shows the polycrystalline nature of the β -Ga₂O₃ films.





Fig. 3. (a) Top view FESEM images of the sample G1 shows the smooth and uniform surface of Ga₂O₃ film (b) FESEM image of sample G2 shows the rough surface and peaks on the surface indicates defects. (c) and (d) Cross-sectional view FESEM images to measure the thickness of β -Ga₂O₃ films for the samples G1 and G2 respectively. The thickness of 116 nm and 110 nm were measured for the samples G1 and G2 respectively. (e) and (f) AFM image to determine the RMS roughness (R_q) of the sample G1 and G2 respectively. The RMS roughness of 3.62 nm and 5.43 nm were obtained for the samples G1 and G2 respectively.

Fig. 4 (a) and 4 (b) show the capacitance-voltage (C-V) characteristics and insets of Fig. 4 (a) and 4 (b) represent the $1/C^2$ -V plots for the G1 and G2 SBDs, respectively, at a frequency of 100 kHz. The net donor concentration (N_D-N_A) and built-in potential (V_{bi}) of the SBDs can be extracted from the slope and intercept of the $1/C^2$ -V plots, respectively. The net donor concentration of the SBDs can be expressed as-

$$N_{\rm p} - N_{\rm A} = \frac{2}{q \varepsilon \varepsilon_{\rm A} A^2 slope}, \qquad (1)$$

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where ε_r is the relative permittivity of Ga₂O₃, ε_0 is the permittivity of vacuum. The V_{bi} obtained from the intercept of the plots are 0.98 V and 0.59 V, corresponding to the G1 and G2 SBDs, respectively. The values of N_D-N_A calculated from equation (1) are 1.07×10^{17} cm⁻³ and 1.47×10^{18} cm⁻³ of the G1 and G2 SBDs, respectively. A similar method of calculating ND-NA for Ga2O3 SBDs has been used by Fu et al. ³⁰. The carrier concentration of sample G2 is higher than the G1, which might be due to the more defects present on the surface of sample G2. These defects might also be due to the scarcity of oxygen atoms, meaning increment in the oxygen vacancies which leads to the increment in the carrier concentration 5,31 . The higher surface roughness of sample G2 is also confirmed by the AFM image. Moreover, we have also confirmed the carrier concentration is higher for G2 than G1 using Ga to O compositional ratio obtained by the energy-dispersive X-ray spectroscopy (EDS) technique. Ga and O atomic percentages were 37.85 and 62.15 respectively, hence Ga to O composition ratio was 0.60 for the sample G1. Whereas for the sample G2, Ga, and O atomic percentage were 41.22 and 58.31 respectively, hence Ga to the O composition ratio of 0.71 was obtained. Thus, from EDS data, it can be concluded that the Ga to O ratio is higher for the G2 sample than the G1 because of the scarcity of oxygen atoms in sample G2. This scarcity of oxygen increases the oxygen vacancies which leads to the increament in the carrier concentration ²⁰.

The barrier height of the SBDs can be calculated by C-V characteristics using the following expression³⁰

$$q\phi_{B} = qV_{bi} + (E_{C} - E_{F}) - q\phi_{IBL}, \qquad (2)$$

where ϕ_{IBL} is the image-force barrier height lowering and $(E_C - E_F)$ is the energy difference between conduction band minimum and Fermi level. The rough positions of V_{bi}, ϕ_{IBL} , and ϕ_B are illustrated in Fig. 5. ϕ_{IBL} can be expressed by ³⁰

$$q\phi_{\rm IBL} = \left[qE_{\rm ms} / (4\pi\varepsilon_0\varepsilon_r)\right]^{1/2},\tag{3}$$

where E_{ms} is the electric field at the Au/Ga₂O₃ interface and can be expressed as ³⁰

$$E_{ms} = \left[2q(N_D - N_A)V_{bi} / (\varepsilon_0 \varepsilon_r)\right]^{1/2}, \qquad (4)$$

The calculated values of ϕ_{IBL} using equations (3) and (4) for all the SBDs are stated in Table 1. The (*E_C*-*E_F*) is given by ³²

$$E_{C} - E_{F} = \frac{E_{g}}{2} - kT \ln\left(\frac{N_{D} - N_{A}}{n_{i}}\right),$$
(5)

where E_g is the energy bandgap of the β -Ga₂O₃ equal to 4.8 eV, *ni* (1.79×10⁻²² cm⁻³) is the intrinsic carrier concentration of the Ga₂O₃ semiconductor. After placing all terms into equation (2), the Schottky barrier heights are 1.01±0.01 eV, and 0.49±0.01 eV for the G1 and G2 SBDs, respectively. The barrier heights obtained from the J-V characteristics as listed in Table 1 are smaller than calculated from *C-V* characteristics. It might be attributed to the inhomogeneous Schottky barrier height caused by the defects between metal-semiconductor interfaces ¹¹. The *C-V* Schottky barrier heights are mainly governed by the carrier concentration of the semiconductor and do not include any current conduction, whereas the *J-V* Schottky barrier height signifies the barrier height for current flow ¹¹. Therefore, the *C-V* Schottky barrier height is not responsible for crystal structure and surface properties of Ga₂O₃ film, those dominant the current conduction.

Fig. 6(a) and 7(a) represents the current density vs. voltage (J-V) characteristics of the fabricated fully vertical Schottky barrier diodes (SBDs) in linear scale. The specific on-state resistance (R_{ON}) was measured from the linear fits to J-V data in the forward bias for all the SBDs. The extracted values of R_{ON} are 1.49 Ω -cm² and 1.73 Ω -cm² corresponding to the G1 and G2 SBDs, respectively.

The forward J-V characteristics of most practical SBDs following the thermionic emission mechanism can be expressed as ³³

$$J = J_0 \left[\exp(qV / nkT) - 1 \right], \tag{6}$$

where *V* is the voltage applied across the diode, q is the electron charge, *k* is the Boltzmann constant, and n is the ideality factor signifying the forward bias characteristics deviation from the ideal thermionic emission behavior. J_0 is the reverse saturation current density derived from the intercept of the straightline fitted to the *lnJ-V* plot and can be given as ³³

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Fig. 4. C-V characteristics of (a) Ga_2O_3 on Si (100) (b) Ga_2O_3 on Si (111) SBDs. The insets of Fig 4 (a) and 4 (b) show the $1/C^2$ -V plots for G1 and G2 SBDs, respectively, at a frequency of 100 kHz.



Fig. 5. Schematic of the band diagram for the fabricated SBDs.

$$J_0 = A^* T^2 \exp\left(-q\phi_B / kT\right),\tag{7}$$

where A^* is the Richardson constant equal to 41.1 A.cm⁻²K⁻² for Ga₂O₃, and ϕ_B is the barrier height of the SBDs.

Fig. 6(b) and 7(b) shows the semi-logarithmic J-V plots of the SBDs. The current increases exponentially at lower voltages, and at the higher voltage, the current gets saturated due to the domination of series resistance. The obtained reverse saturation current density (J₀) were 2.72×10^{-5} and 1.52×10^{-1} A.cm⁻² for the diodes G1 and G2, respectively. Hence, The J/J_0 ratios at 5 V were determined to be 7.81×10^4 and 7.62 for G1 and G2 SBDs, respectively, as listed in Table 1. The value of J/J_0 was small for diode G2 may be due to high leakage current as shown in fig. 7(b), whereas diode G1 has a high rectification ratio with a high Schottky nature. Since the Schottky barrier of the diodes increases



with the increase in the crystalline quality of the growth film ³⁴, thus the higher Schottky nature and lower reverse saturation current density of G1 may easily be attributed to the superior crystalline quality and the smoother surface of the deposited film.

The barrier heights of the SBDs have been calculated by rearranging the terms of equation (7)

$$\phi_{\rm B} = \frac{kT}{q} \ln\left(\frac{A^*T^2}{J_o}\right),\tag{8}$$

The values of Schottky barrier heights were determined using J-V characteristics to be 0.67 eV and 0.43 eV for the G1 and G2 SBDs, respectively. The barrier height is higher for the G1 as compared to G2 because the reverse saturation current density is lower for G1 and higher for G2, as the barrier height is inversely proportional to the reverse saturation current density mentioned in equation (8). Moreover, the high Schottky barrier height and low reverse saturation current density of G1 may be due to the smoother surface of the deposited film as compared to the G2.

The effect of the series resistance Rs is typically exhibited with the connection of a diode and a resistance Rs in series, over which the current flows. The voltage applied (V) across the diode can be expressed in terms of the total voltage drop V_D across the series connection of a diode and resistance. Thus, $V = V_D - IRs$, hence, the equation (6) becomes

$$J = J_0 \left[\exp\left\{ q(V_D - R_S A_e J / nkT) - 1 \right\} \right], \tag{9}$$

Where A_e is the effective area of the diode. For V>3kT/q, the equation (9) becomes

$$J = J_0 \exp\left[q(V_D - R_s A_s J / nkT)\right],\tag{10}$$

By differentiating the equation (10) with respect to J, the obtained form of the equation can be expressed as

$$\frac{dV_D}{d(\ln J)} = R_S A_e J + \eta \left(\frac{kT}{q}\right), \qquad (11)$$

Thus, the value of series resistance and ideality factor can be obtained using $d(V_D)/d(lnJ)$ vs. J plots. The slope (R_sA_e) of the plot will give the value of Rs, and the intercept (nkT/q) of the plot will give the value of the ideality factor. A similar method of determining the series resistance has been reported by *Cheung*



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et al. ³³, and *Çaldıran et al.* ³⁵. The obtained values of series resistances from the $d(V_D)/d(lnJ)$ vs. J plots are 0.229 k Ω and 0.796 k Ω for the SBDs G1 and G2, respectively.

The series resistance is responsible for the shape of the forward bias nonlinear *I-V* characteristics of the diode. The curvature of the *I-V* curve will be broad when the series resistance is high. The shunt resistance is responsible for the current losses at the junction. Thus, the series resistance of the diode should be lower, whereas shunt resistance should be kept as high as possible to reduce the current loss at the junction. The series resistance and shunt resistance of the SBDs can be determined by the *dV/dI* (device resistance R_i) vs. *V* plots. Fig. 8 shows the variation of device resistance and shunt resistance bias. Ideally, the values of series resistance and shunt resistance should be zero and higher than $10^8 \Omega$, respectively ³⁶. However, in practice, the value of series resistance in the forward bias decreases for the higher voltages. In contrast, the shunt resistance in the reverse bias is saturated at high reverse voltages, as shown in fig. 8. SBD G1 has a lower series resistance, and higher shunt resistance might be due to the smoother surface and good crystal quality of the deposited Ga₂O₃ film. Sample G2 has significantly higher series and lower shunt resistance, attributed to the rougher surface of the film and the presence of more defect states at the metal-semiconductor interface.

The ideality factors (n) of the G1 and G2 SBDs were obtained to be 2.38 and 5.85, respectively, from the slope of the linear fit to the *lnI-V* plots ¹⁵. The electrical parameters extracted for all the SBDs are illustrated in Table 1. The values of the ideality factors of both the SBDs are greater than unity. Higher values of ideality factor are attributed to the presence of interface states, defect states on the Ga₂O₃ surface, barrier height inhomogeneities, and higher series resistance because of the polycrystalline nature of the Ga₂O₃ films ^{20,22,37,38}. The ideality factor of G1 is lower owing to the lower value of series resistance as compared to G2 SBD.

Besides, the current-voltage (I-V) characteristics in the log-log scale are plotted to understand the charge transport mechanisms within the fabricated diode structures. Fig. 6(c) shows the forward bias *logI-logV* plot of the SBD G1. It consists of three different regions, namely regions I, II, and III. The *logI-logV* plot of the Schottky diode is following a power-law relationship of $I \propto V^m$ (with varying values of

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exponent "m"). In the region-I (at lower voltage), the slope of the *logI-logV* plot is 3.07. It can be argued that the charge transport in region-I is primarily governed by the space charge limited current (SCLC) mechanism. It means the current conduction is affected by the space charges, which consist of the trapped charge carriers near the Fermi level ²². The SCLC conduction mechanism is fairly a standard phenomenon in the wide bandgap semiconductors ³⁹. In region II, the slop is equal to 7.79, where the current conduction might be due to the diffusion of charge carriers. Therefore, in region-II, the current increases exponentially with applied voltage. The slope of the region-III is 2.67, which implies that the charge transport is corresponding to another typical SCLC mechanism. In the SCLC mechanism, the current conduction is mainly due to the injection of free charge carriers since the injected charge carriers' density is relatively larger than that of thermally generated free charge carriers. Zhang et al.²² have also been shown a similar charge transport behavior for the p-Si/n-Ga₂O₃:Nb heterojunction.

The *logI-logV* plot for the G2 is shown in fig. 7 (c). There are two different regions with two different conduction mechanisms. The slope of the region-I is equal to 1.078, which is very close to unity. In this region, the charge transport is governed by the ohmic conduction mechanism, where the current is linearly dependent on the voltage. The ohmic conduction in the device is primarily due to the thermally generated carriers without the existence of any energy barrier to them⁴⁰. Region II has a slope of 2.84, which is corresponding to the SCLC mechanism. At higher bias, the linearity of the forward bias I-V plot might be deviated mostly due to the existence of the high series resistance ⁴¹.



Fig. 6. (a) J-V characteristics of vertical SBD in linear scale for sample G1. The on-state resistance of SBD is extracted to be $1.49 \ \Omega$ -cm². (b) J-V characteristics of vertical SBD in the semi-logarithmic scale. The reverse saturation current density and barrier height are obtained to be 2.72×10^{-5} A.cm⁻² and 0.67 eV, respectively. (c) Forward bias *logI-logV* plot of the SBD to explain the conduction mechanism.

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Fig. 7. (a) J-V characteristics of vertical SBD in linear scale for sample G2. The on-state resistance of SBD is extracted to be 1.73 Ω -cm². (b) J-V characteristics of vertical SBD in the semi-logarithmic scale. The reverse saturation current density and barrier height are obtained to be 1.52×10^{-1} A.cm⁻² and 0.43 eV, respectively. (c) Forward bias *logI-logV* plot of the G2 SBD.



Fig. 8. Variation of the device resistance along with the applied voltage in forward and reverse bias.

Generally, thermionic emission (TE) is dominant for carrier transport in Ga_2O_3 SBDs due to the low mobility of Ga_2O_3 . In addition to TE, field emission (FE) and thermionic field emission (TFE) are also the main current transport mechanism in SBDs. However, an in-depth study is needed to understand the dominant carrier transport mechanism. According to the metal-semiconductor theory, the current transport mechanisms can be described using the tunneling parameter. The tunneling energy (E₀₀) is given by

$$E_{00} = \frac{qh}{4\pi} \left[\frac{N_D - N_A}{m^* (\varepsilon_s / \varepsilon_0)} \right]^{0.5}, \qquad (12)$$

$$E_{00} \approx 1.85 \times 10^{-11} \left[\frac{N_D - N_A}{(A^* / 120\alpha)(\varepsilon_s / \varepsilon_0)} \right]^{0.5},$$
(13)



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where h is the Plank constant, m^{*} (=0.342 m₀) is the effective mass of electron of Ga₂O₃, ϵ_0 is the permittivity of free space, ϵ_s is the dielectric constant of the semiconductor, and α is the empirical factor. The value of α is calculated to be 1 for A^{*} of 41.1 Acm⁻²K⁻². After putting all the terms in equation (12), the values of tunneling parameters (E₀₀/kT) are 0.12 and 0.51 for G1 and G2 SBDs, respectively.

Now, the dominant current transport mechanisms in SBDs can be determined by E_{00}/kT , which has the following conditions,

(i) TE is the dominant mechanism when E_{00}/kT is much lesser than 1

(ii) TFE is the dominant mechanism when $E_{00}/kT \approx 1$

(iii) FE is the dominant mechanism when E_{00}/kT is much greater than 1

The value of E_{00}/kT is much lesser than 1 for the G1 SBD, which is corresponding to the TE dominant current transport mechanism. Whereas, E_{00}/kT value for G2 is close to unity, which means TFE is the dominant current transport mechanism in G2 SBD.

Further, the possibility of the different current transport mechanisms can be checked by TE and TFE models. Fig. (9) (a) and (b) shows the calculated TE models from the equation (5) at room temperature for sample G1 and G2. The J-V characteristics of the sample G1 at low voltages is well fitted with the calculated TE model as shown in Fig. 9 (a). It means TE is the dominant current transport mechanism in sample G1. However, the TE model at low voltages is not well fitted for the sample G2 as shown in Fig. 9 (b). Thus, TE is not the dominant transport mechanism in sample G2, there might be the possibility of electric field-induced tunneling at the Schottky contacts.



Fig 9. calculated TE models of the J-V characteristics for the (a) sample G1 (b) sample G2.



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The current density due to the TFE can be theoretically calculated by the following simplified expression given by Higashiaki et al ⁴².

$$J_{TFE} = \frac{A^{*}TqhE}{2\pi k} \sqrt{\frac{\pi}{2m^{*}kT}} \times \exp\left[-\frac{1}{kT} \left(\phi_{B} + \phi_{IBL} - \frac{(qhE)^{2}}{24m^{*}(2\pi kT)^{2}}\right)\right]$$
(14)

where h is the Plank constant and E is the electric field. The electric field at the Schottky interface can be expressed as

$$E = \sqrt{\frac{2q(N_D - N_A)(V_{bi} - V)}{\varepsilon_r \varepsilon 0}} , \qquad (15)$$

The values of (N_D-N_A) and V_{bi} have been calculated using C-V characteristics of the SBDs for the samples. Thus, the electric field values can be calculated using equation (15). By rearranging the terms of equation (14)

$$\frac{J_{TFE}}{E} = \frac{A^{*}Tqh}{2\pi k} \sqrt{\frac{\pi}{2m^{*}kT}} \times \exp\left[-\frac{1}{kT} \left(\phi_{B} + \phi_{IBL} - \frac{(qhE)^{2}}{24m^{*}(2\pi kT)^{2}}\right)\right]$$
(16)

Let us consider

$$\frac{\phi_{\scriptscriptstyle B} + \phi_{\scriptscriptstyle IBL}}{kT} = C \,, \tag{17}$$

$$\frac{q^2 h^2}{24kTm^* (2\pi kT)^2} = D, \qquad (18)$$

$$\frac{A^*Tqh}{2\pi k}\sqrt{\frac{\pi}{2m^*kT}} = A,$$
(19)

the equation (16) can be expressed as

$$\frac{J_{TFE}}{E} = A \exp\left[-\left(C - DE^2\right)\right],\tag{20}$$

$$\ln\left(\frac{J_{TFE}}{E}\right) = \ln A - \left(C - DE^2\right),\tag{21}$$

$$\ln\left(\frac{J_{TFE}}{E}\right) = \left(\ln A - C\right) + DE^{2},$$
(22)



let us consider $(\ln A - C) = B$, then the equation (22) can be expressed as

$$\ln\left(\frac{J_{TFE}}{E}\right) = B + DE^2, \qquad (23)$$

Equation (23) is a form of expression $y = m_x + c$, where m and c are the slope and intercept of the straight line. Now we can plot ln (J_{TFE}/E) Vs. E² graph using J-V characteristics for both the diodes. The theoretically calculated TFE models for both the samples G1 and G2 are shown in Fig. 10(a) and 10(b) respectively. As shown in Fig. 10 (a), the calculated TFE current density model is not well fitted with the J-V characteristics of the SBD, thus the TFE transport mechanism is not dominant in the sample G1. Whereas, the calculated TFE model is in good agreement with the J-V characteristics of the diode as shown in Fig. 10 (b). Therefore, the TFE transport mechanism is the dominant current transport mechanism in the sample G2 which is responsible for the tunneling of electrons from the metal to Ga₂O₃. Thus, it can be corroborated that polycrystalline Ga₂O₃ film on Si(100) leads to less defects emerging from the Ga₂O₃/Si heterointerface due to the rectangle symmetry of Ga₂O₃ and Si(100) crystal projections unlike Ga₂O₃/Si(100) where we have observed typical thermionic dominating carrier transport mechanism in Ga₂O₃/Si(111).



Fig.10 calculated TFE models of the J-V characteristics for the (a) sample G1 (b) sample G2.

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Fig.11. crystal structure of monoclinic Ga_2O_3 orientated along (-201) plane and Si oriented along (100) and (111) plane computed using Vesta software⁴³. Ga_2O_3 (-201) and Si (100) show the square structure, whereas Si (111) has a hexagonal type of structure.

Table. 1. Experimental values of the electrical parameters obtained from the J-V characteristics for both the fabricated SBDs.

Samples/ Parameters	G1	G2
п	2.38	5.85
$J_{0}(\mathrm{A.cm}^{-2})$	2.72×10 ⁻⁵	1.52×10^{-1}
J/J_0 at 5 V	7.81×10^4	7.62
$R_{ON}(\Omega$ -cm ²)	1.49	1.73
$R_{S}(\mathbf{k}\Omega)$	0.229	0.796
$\phi_{B_J-V}(eV)$	0.67	0.43
V_{bi} (V)	0.98	0.59
$N_D - N_A (\text{cm}^{-3})$	1.02×10^{17}	1.74×10^{18}
$\phi_{IBL} (eV)$	0.052	0.112
$\phi_{B_C-V}(eV)$	1.01	0.49
E_{00}/kT	0.12	0.51

IV.CONCLUSION

In summary, Ga_2O_3 film deposited on (100)- and (111)- oriented p-Si substrates using the PLD technique exhibits the polycrystalline nature of the films evaluated using XRD. The thicknesses of samples were 116 nm, and 110 nm for the samples G1, and G2, respectively measured using cross-sectional FESEM. Sample G1 shows better device performance along with higher Schottky barrier height, smaller ideality factor, higher J/J₀ ratio, lower on-state resistance, and lower series resistance. Sample G2 shows the pseudo ohmic behavior with the lower barrier height, subsequent lower the J/J₀ ratio might be attributed to the rough surface and presence of defects at the metal-semiconductor interface. The thermionic field emission current conduction mechanism is responsible due to the tunneling of the carriers leading to degraded device performance of the G2 diode. Hence, it can be concluded that the sample G1 shows

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better device performance as compared to the G2 for potential high-power applications. Thus, Si (100) is evidenced to be a better substrate than Si (111) to deposit Ga₂O₃ due to the similarity of the tilted-cuboid crystal structure of β -Ga₂O₃ on cubic Si (100) whereas hexagonal projection of Si (111) may not be suitable for obtaining good monoclinic β -Ga₂O₃ crystal. Further atomic-level studies at the interface of Ga₂O₃ on Si are presently under investigation.

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AVAILABILITY OF DATA

The data that supports the findings of this study are available within the article.

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Au	Au
β-Ga ₂ O ₃	β-Ga ₂ O ₃
Si (100) G1	Si (111) G2
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