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Integration of High-Performance Cost-Effective Copper-Metal-Organic-Nanocluster-based Gate Dielectric for Next-Generation CMOS Applications

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The suitability of metal-organic frameworks (MOFs) as functional materials for future electronic logic devices with desirable dielectric constant, bandgap, high-quality interface, low leakage current, and better compatibility is still an open challenge. Owing to the synergistic complementary properties of MOFs systems, a low-cost copper-metal-organic nanoclusters (Cu-MOCs) has been synthesized comprising inorganic copper metal unit allied organic m-toluic acid ligand by facile sol–gel strategy. It offers large-area thin-films uniformity, high dielectric constant ($\kappa \approx 5.49$), improved interfacial properties, dynamic switching behavior with the stimuli field, and extends the realization of metal-organic-framework dielectric for scalable complementary-metal-oxide-semiconductor (CMOS) logic applications over customary hybrid counterparts. Various techniques such as single crystal X-ray diffraction, X-ray photoelectron spectroscopy, thermogravimetric analysis, and energy dispersive X-ray spectroscopy have been used to validate the Cu-MOCs formulation. In particular, the fabricated Cu-MOCs, metal–insulator–semiconductor structures exhibit promising dynamic switching behavior responsive to the applied field, hysteresis-free capacitance–voltage characteristics, low interfacial trap density ($\approx 1.4 \times 10^{11}$ eV^{-1} cm^{-2}), low effective oxide charges ($\approx 1.1 \times 10^{11}$ cm^{-2}), and noteworthy small leakage current density (≈ 1.29 nA cm^{-2} @ 1 V) ever since in electrical analysis. Cost-effective novel Cu-MOCs successfully demonstrate high-performance, reliable gate dielectrics for next-generation CMOS logic devices.

1. Introduction

Presently, there has emerged great interest toward a new set of electronic materials; metal-organic-frameworks (MOFs) for next-generation complementary metal-oxide-semiconductor (CMOS) applications due to integrated properties of high-κ metal oxides and low cost, easy processing, and flexible organic molecules.[1–4] The mere process of solution-based synthesis, spin-coating for the thin-films formation, and low-temperature operation for device processing strategies do have the robust potential to replace the more complicated processes involved with conventional silicon technology.[5–8] However, firmly anchored, the unprecedented growth of the semiconductor industry in general and the integrated circuits, in particular, was driven by the advancement of metal–insulator–semiconductor field-effect transistors (MIS-FETs). Ever since, silicon dioxide or its derivatives have been carrying out a dominating role as active dielectric materials for the advancement of MIS-FETs, which is certainly the basic building block of integrated circuit (IC) technology.[9] Mostly, conventional dielectrics have shown moderately low dielectric constants which results in large static power dissipation for scaled technology. Hence, they limit their practical applications in reducing corresponding dielectric thicknesses in the nanometric regime as requisite by next-generation technology nodes. Indeed, serving the vital needs of equivalent oxide thickness (EOT), new-age high-κ dielectrics permit the technology to increase the physical thicknesses of the gate stacks and to reduce the gate leakage currents significantly. Henceforth, to meet the demands of electronic markets, profitable exploitation of novel, compatible, alternate high-κ dielectric materials is imperative.[10,11] Ergo, potential gate dielectrics must favor significant large bandgap (E_G) and high dielectric constant (κ), along with facile possessing and an even tradeoff between E_G and κ intrinsic properties.[12] Recent advancements in various high-κ dielectrics deliver commendable dielectric properties, higher capacitances with EOT, low-voltage operations, increased dielectric thicknesses, better retention characteristics, lower leakage current densities < 1 A cm^{-2} at 1V gate bias, smaller static power dissipation, higher breakdown voltages > 1 MV cm^{-1}, pinhole-free dense film morphologies, and good thermal stability, etc.[13–15] Especially, inorganic/solid-state dielectrics such as Al_2O_3, HfO_2, ZrO_2, Y_2O_3 have been popular since the last decade for providing substantially higher dielectric constants (high-κ) engenders the admirable gate-dielectric properties.[16–18] However, inorganic materials are much brittle to be compatible with diverse substrates for cost-effective processing, and the integration of high-quality

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layers into large-area facile coating processes at room temperature is also unseemly.[19] Likewise, deposition techniques for electronic device-level films typically require expensive industrial materials and high-vacuum equipment.[20] On the contrary, organic polymers such as poly(methyl methacrylate) ($\kappa \approx 3.5$), poly(vinyl phenol) ($\kappa \approx 4.2$), polystyrene ($\kappa \approx 2.6$)[21], poly(vinylidene fluoride-co-hexafluoropropylene)-HFP[22], 4-C-4-MMA-co-GMA-co-HEMA polymer, and 3,5-C-4-MMA-co-GMA-co-HEMA polymer[19] are easy in operation and have high flexibility but, provide typically low to moderate dielectric constants because of weak intermolecular forces and also have limited thermal management due to modest thermal stability.[20,23]

Thus, the attempt to utilize the best of both worlds, moderate properties of the organic and inorganic parts were brought into a hybrid dielectric formulation; HfO_2 (inorganic)-PMMA (organic) by Mullapudi et al.[24] However, the complexity to mix incompatible inorganic–organic phases, poor solubility, nonuniform solutions, and unexpected agglomerations lead to degraded dielectric performance. Consequently, there arose the need for cordially physical and chemical compatibility for the integration of inorganic–organic counterparts to stimulate the exceptional gate dielectrics for device applications. Not only that, but the novel materials like MOFs correspondingly possess highly tunable physical, electronic, and mechanical properties, which make them exemplary gate dielectric candidates for future CMOS integrated circuits applications. Beforehand, metal-organic-clusters (MOCs) have been widely explored as active materials such as conductors[25,26], semiconductors[2,27], and insulating[28–34], gate dielectrics in various electronic applications such as MOS-Cs[20], OFETs[8], etc.[3,35–38] Anqi Hu et al.[39] discussed the epitaxial growth and integration of insulating MOF, and Salvator Eslava et al.[40] used ZIF-8 dielectric MOF films for microelectronic applications. Ryder et al.[30] and Warmbier et al.[32] showcase low-κ and ultralow-κ dielectric MOF where bandgap tuning is possible with different metals and linkers and static dielectric constant is mainly related to the framework, respectively. However, to the best of our knowledge, hardly a few reports on MOCs acting as dynamic gate dielectrics with stimuli field in metal–insulator–semiconductor field-effect-transistors (MIS-FETs) structures have been reported. For instance, Pathak et al.[31] reported high-κ dielectric samarium-based MOF for gate applications. Usman et al.[33] also, showcase high-κ dielectric Sr-MOF with dielectric modulation based on polar molecule confinement. For a while, Engelbert Redel et al. demonstrated the study of dielectric and optical properties of MOFs thin films.[41] Hence, the integration of compliable high-κ inorganics and flexible organics, into MOCs dielectric formulation for MIS-FETs applications may provide a possibly rewarding solution.[40] MOCs or coordination polymers, the latest class of ordered trimmable nanoporous solids which can suitably form large-area uniform thin-films, have been recently attracting immense attention owing to their well-established advantages. Advantages such as high surface area, good thermal and mechanical properties, and easy tunable composition of MOCs by varying the organic linker and inorganic counterparts, particularly useful for better control in high-quality thin film formation.[3,27] Moreover, high purity material formation, low-cost, ease-of-synthesis, low molecular weight, and robust stability of MOCs nanostructures and their competency to form thermally and mechanically stable thin films are the major advantages which favor them toward electronic applications.[1] On top of this, these hybrid MOCs formulations are besides proficient to result in high-κ solution-processable materials by incorporating guest particles in the empty pores' locations. Typically, the MOCs system without guest particles exhibited low dielectric constant, independency of temperature and frequency maybe for the clusters don't have positional freedom in the crystalline state.[42] However, with entrapping or coordination of polar guest particles which are typically free to move accompany high polarizability into the nanoporous materials, illustrating the opportunity to tune host-guest interactions and certainly a large dielectric constant, higher thermal and mechanical stability could be achieved.[29,42] It might be possible that the obtained reliable thin films of MOCs exhibit the dielectric constant that is more than three times higher than that of the bulk MOC material.[20] Owing to these properties, MOCs may be strong potential candidate alternate for high-κ gate dielectrics in nanoscale CMOS logic devices.

There are, however, some constraints utilizing a metal-organic-clusters based approach for successful adaptation as gate dielectrics for logic applications and need comprehensive interfacial and bandgap engineering. Broad agreement that metal-organic-clusters films are crystalline and highly nanoporous and the formation of large-area, high interface quality, transistors-level uniform thin-film is a major challenge. By that, the introduction of guest molecules in nanopores locations may result in poor mechanical flexibility and enhanced surface roughness.[19] Hence, the main challenge lies in the realization of uniform, defect-free, high interface quality device level thin-films for high-performance CMOS applications. However, the best possible coordination interactions of the metal-center and organic linkers may result in good adhesion and compatibility with the existing silicon technology and may prevent the formation of undesirable interfacial defects. Hence, the dynamic control of stimuli applied field over MOCs dielectrics and good interfacial compatibility with silicon substrates can be imperative for next-generation transistors applications.

Montañez et al. demonstrated the fabrication of metal–insulator–semiconductor capacitors (MIS-CAP) using $Cu_3(BTC)_2$ MOF as the insulating material.[43] Wei-Jin Li et al. presented a rational design of metal-organic-frameworks thin films on conductive supports with high-performance dielectric properties.[20] Hence, MOCs show great potential as high-κ gate dielectrics in MIS transistor structures and imperative to provide better dielectric and interfacial properties, uniform thin films, lower leakage currents, desired capacitance, lower operating voltages, smaller static power dissipation, and higher breakdown voltages.

Here, for the first time, low-temperature solution-processable novel copper-metal-organic-nanoclusters (Cu-MOCs) dielectric based metal–insulator–semiconductor capacitor structures are fabricated for reliable low-voltage CMOS applications. The formulated, Cu-MOCs in this study employs bandgap and dielectric constant engineering to deliver a decent tradeoff between bandgap and dielectric constant, through adjusting its inorganic copper metal and organic ligand compositions. The dielectric films of Cu-MOCs are deposited by a simple

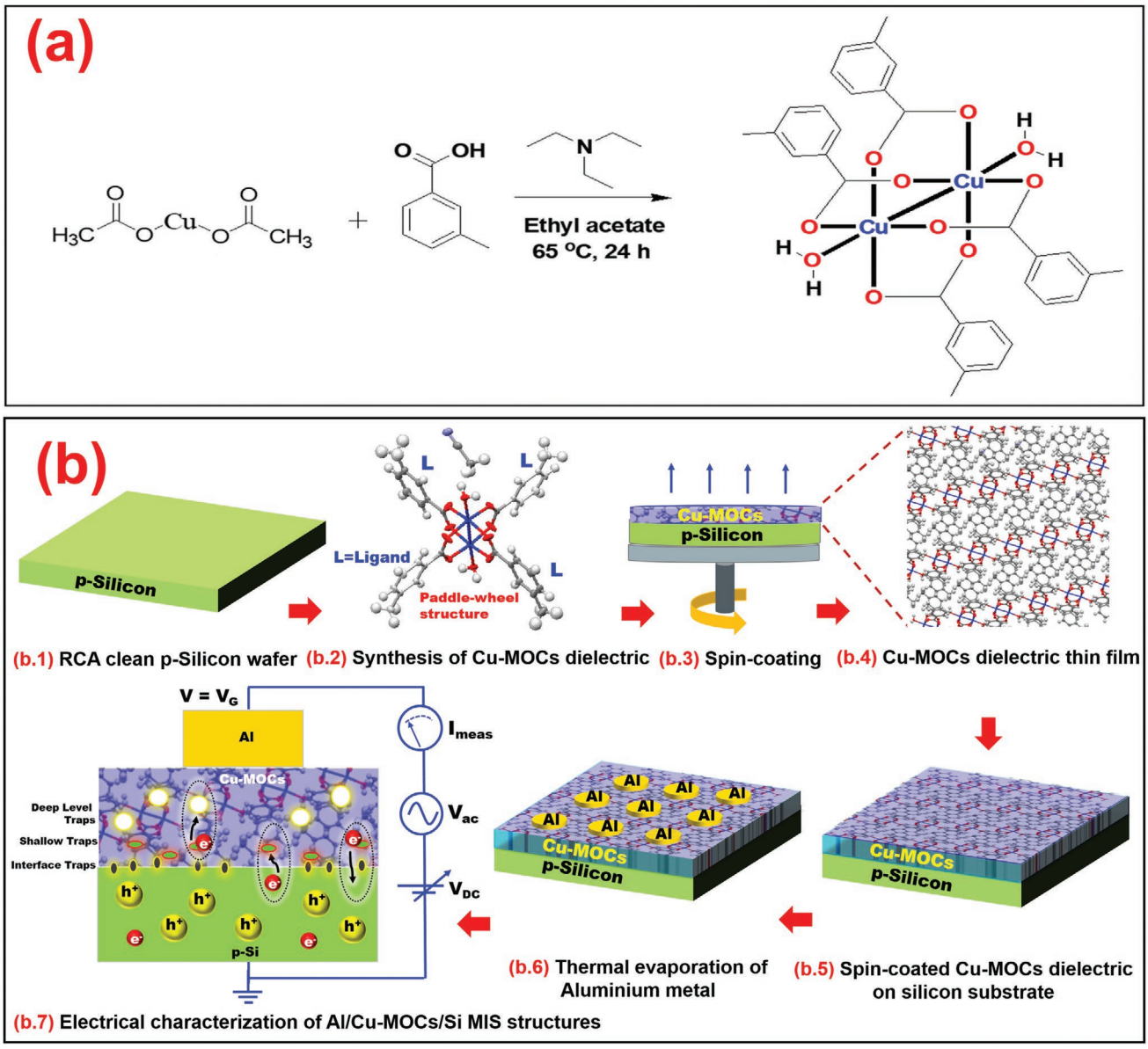

Figure 1. Schematic process flow. a) Synthesis methodology for novel Cu-MOCs dielectric using copper acetate hydrate with m-toluic acid in the presence of tri-ethyl amine and ethyl acetate at 65 °C for 24 h to give paddle-wheel structure-based copper metal-organic nanoclusters. b) Fabrication of metal–insulator–semiconductor capacitor (MIS-CAP) structures using Cu-MOCs dielectric. b.1) RCA clean p-silicon wafer. b.2) Synthesis of Cu-MOCs dielectric. b.3) Spin-coating. b.4) Cu-MOCs dielectric thin film. b.5) Spin-coated Cu-MOCs dielectric on a silicon substrate. b.6) Thermal evaporation of aluminum metal. b.7) Schematic representing electrical characterization of Al/Cu-MOCs/Si MIS-CAP structures with electron conduction at the interface, shallow, deep-level traps.

spin-coating method to obtain large-area highly quality uniform thin-films. Aluminum electrodes are patterned by the standard process to form metal contact for MIS-CAP structures. The dynamic control of the stimuli field over Cu-MOCs dielectric thin film has been established from electrical characteristics; *C–V*, |*J*|*–V*, *G–V*, stress-based *C–V*, and |*J*|*–V*. The thin films' surface roughness and thicknesses were inspected with atomic force microscopy (AFM) and ellipsometry, respectively. In this study, we systematically investigated the dielectric properties of Cu-MOCs material; the results may provide a new perspective for the design of next-generation transistor electronics.

2. Results and Discussions

MIS-CAP structures for CMOS logic applications were fabricated with novel Cu-MOCs dielectric as synthesized from processing steps as shown in **Figure 1**a. The novel solution-processed Cu-MOCs dielectric comprises of copper-based metal building inorganic unit linked with monovalent m-Toluic acid organic ligand constituting into a single unit, deposited in the form of large-area uniform thin films on p-type RCA cleaned silicon wafers. Aluminum gate electrodes were patterned over Cu-MOCs/Si systems with standard semiconductor processing

techniques to form the Al/Cu-MOCs/Si structures as depicted in the schematic of Figure 1b. Here, the Cu-MOCs system was employed as an active gate dielectric layer in Al/Cu-MOCs/Si MIS-CAP structures in place of conventional inorganic/organic gate dielectrics. The advantage of novel Cu-MOCs formulation, which was synthesized with a facile sol–gel method, is that it is easy to scale up and hence is much cheaper than the corresponding inorganic/organic high-κ conventional dielectrics. The realization of high-quality large-area uniform thin film formation from developed dielectric formulation requires a simpler and cost-effective spin-coating based deposition technique, as compared to corresponding inorganic/organic high-κ counterparts, which are generally deposited through highly expensive sputtering or atomic layer deposition (ALD) based standard semiconductor processing techniques. Hence, novel Cu-MOCs show cost-effectiveness, high efficiency, and potential candidature for bulk production for replacing conventional dielectrics as active gate material in semiconducting devices such as MOS-Cs and MOS-FETs.

2.1. Dielectric Constant and Thin Films

The foremost desirable property of potentially high-κ gate dielectric material for MIS-CAP structures is the suitable high-value dielectric constant, preferably greater than the conventional inorganic dielectric SiO_2 $\kappa > 3.9$. The optimum high-κ dielectric constant must accommodate high polarizability in dielectrics leading to higher capacitance and thereby high-charge injection as for the MIS-CAP structures. The dielectric constant (κ) of Cu-MOCs dielectric-based MIS-CAP structures was measured as a function frequency ranging from 10 kHz to 1 MHz as shown in **Figure 2**a. The value of the dielectric constant was obtained as $\kappa \approx 6.03 \pm 0.49$ at the 20 kHz frequency, whereas its value decreases slowly as frequency 1 MHz was approached. The dielectric constant at the desirable high frequency of 500 kHz was found as $\kappa \approx 5.49 \pm 0.01$, where this value was averaged for multiple measurements of MIS-CAP structures. Low error percentage ≈0.3% in the measured value of dielectric constant depicts the highly repeatable nature of electrical characteristics for manifold MIS-CAP structures. Hence, formulated Cu-MOCs dielectric shows suitable properties as a prospective candidate for high-performance gate dielectrics in advanced MIS-CAP structures.

The high-quality smooth surface morphologies of large-area uniform dielectric thin films influence the interfacial engineering of various interfaces of MIS-CAP structure and reduce the defects as well as facilitate the charge transfer, and thereby improve the performance of the MIS-CAP devices. By this means, the AFM technique was used for surface morphology analysis of novel Cu-MOCs dielectric thin films deposited on silicon substrates. 2D and 3D surface microscopy images of 10×10 μm^2 area along with measured root-mean-square (RMS) roughness of deposited Cu-MOCs/Si thin films are shown in Figure 2b,c, respectively. As anticipated, deposited Cu-MOCs thin films showed very low RMS roughness of ≈1.43 ± 0.3 nm. It reveals that thin films of novel high-κ, organic–inorganic Cu-MOCs dielectric are highly uniform in large area with very low surface roughness, which makes them particularly attractive preference as a gate dielectric replacement of SiO_2 in MIS-CAP transistors. The Cu-MOCs thin film thickness was measured from the Accurion EP4 ellipsometer and was found to be ≈29.6 ± 0.3 nm. Besides this, the cross-section and top surface morphology of thin films were also analyzed with field-emission scanning electron microscopy (FESEM) as shown in Figure 2d,e, respectively. Figure 2d shows the FESEM cross-section view of Cu-MOCs/Si thin films with a 200 nm scale bar. It clearly distinguishes the thin interface of deposited Cu-MOCs films over the crystalline silicon substrate. Whereas, Figure 2e shows the FESEM top-view large area uniform image of Cu-MOCs/Si thin

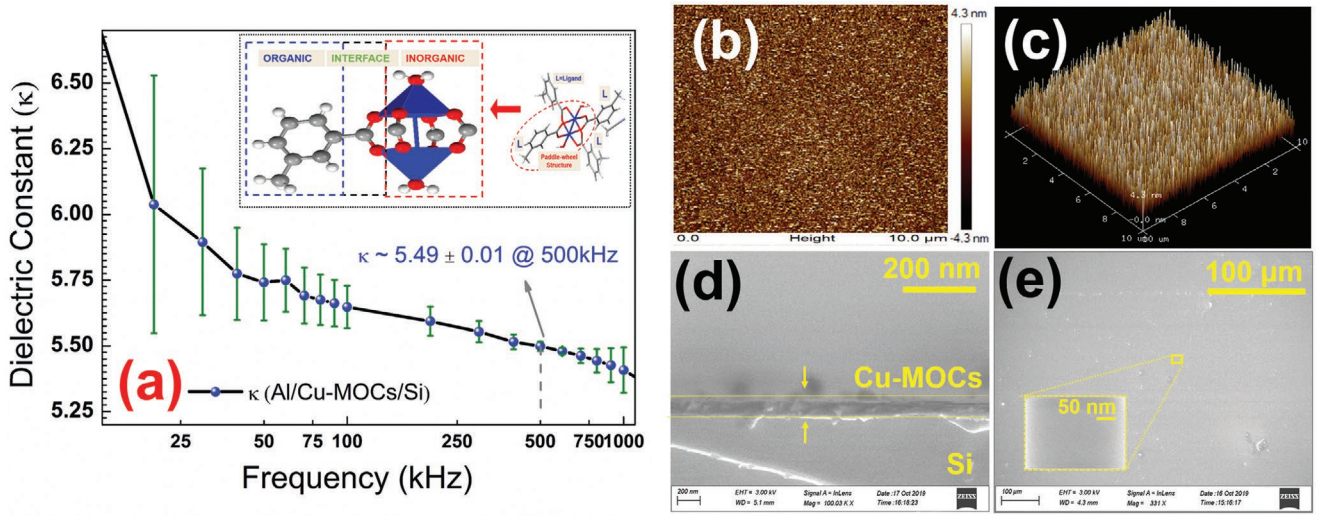

Figure 2. a) Dielectric constant versus frequency characteristics for Al/Cu-MOCs/Si structures from 10 to 1000 kHz. a-inset) Single branch elaboration of unit copper-metal-organic nanoclusters distinguishing its organic, inorganic, and interface components. b) 10×10 μm^2 2D AFM microscopy images of Cu-MOCs/Si thin films. c) 10×10 μm^2 3D AFM microscopy images of Cu-MOCs/Si thin films. d) 200 nm scale FESEM cross-section view image of Cu-MOCs/Si thin films. e) 100 μm scale FESEM top view image of Cu-MOCs/Si thin films. e-inset) 50 nm scale FESEM top view image of Cu-MOCs/Si thin films.

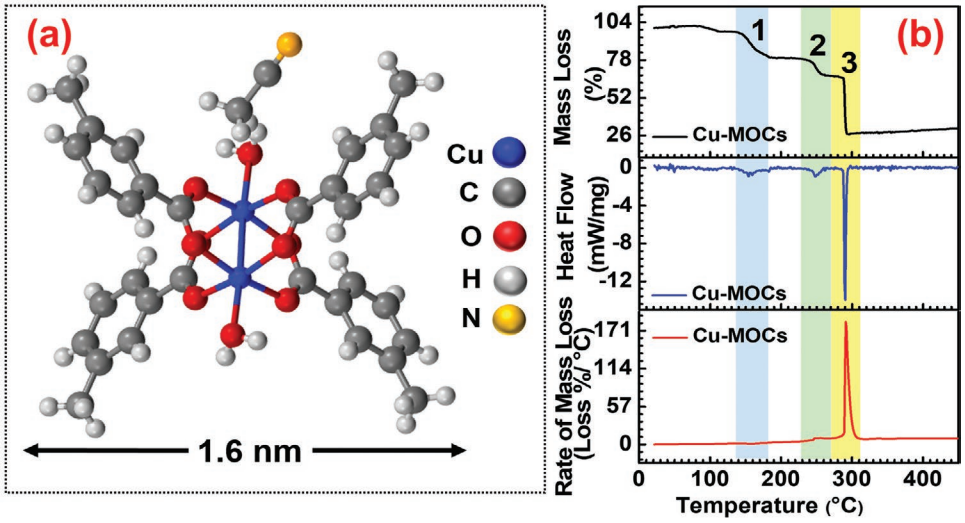

Figure 3. a) Single-crystal X-ray diffraction of copper-metal-organic nanoclusters constituting Cu, C, O, H, N elemental atoms with ≈1.6 nm as the cluster size. b) Thermogravimetric analysis and differential scanning calorimetry of Cu-MOCs dielectric material with temperature variation from 25 to 450 °C defining the weight loss in three distinct steps 1–3.

films at 100 µm scale along with magnified reduced scale top-view image of Cu-MOCs thin films at 50 nm scale as shown in Figure 2e (inset). These microscopy images reveal high uniformity and smooth Cu-MOCs large-area thin film formation with minimal nonuniformities. Both the FESEM surface and cross-sectional microscopy images divulge a quality large-area uniform and smooth dielectric thin film formation. Hence, Cu-MOCs dielectric proves to be best suited for thin-film based gate dielectrics for next-generation CMOS applications.

2.2. Crystal Structure and Composition

The pure single-crystal of Cu-MOCs was grown at room temperature and the grown-single crystal was characterized by single-crystal X-ray diffraction (SC-XRD, Model-Supernova, Rigaku) as shown in **Figure 3**a to investigate the crystal structure, size, bond length, and bond angles between the atoms. The Cu-MOCs crystal, consisting of copper (Cu), carbon (C), oxygen (O), hydrogen (H), nitrogen (N) elemental atoms, has two Cu atoms where each Cu atom is connected to five oxygen atoms resulting in a paddle-wheel structure formation. Here, each m-Toluic acid ligand is associated with the two corresponding oxygen atoms. The size of the nanoclusters as measured with SC-XRD is found out to be ≈1.6 nm, and the corresponding distance between the Cu-Cu atoms was measured to be ≈2.611 Å. The detailed single crystal structure is presented in (Figure S1a, Supporting Information) along with supporting tabular crystallographic information contained in Tables S1–S7 (Supporting Information), respectively. To establish the high-quality electronic device thin-films interface, after ascertaining X-ray diffraction (XRD, Smart Lab, 9kW rotating angle, Rigaku) was used to analyze the crystalline nature and lattice planes of synthesized Cu-MOCs formulation and thin-films. Furthermore, the measured SC-XRD data of the single-crystal of Cu-MOCs was verified with XRD data by comparing the corresponding results of Cu-MOCs systems, as shown in (Figure S1b, Supporting Information). Thin-films of Cu-MOCs were also characterized with XRD, to verify the corresponding results with XRD data of Cu-MOCs systems as shown in (Figure S1b, Supporting Information). It can be seen that the XRD data of Cu-MOCs thin films illustrate a polycrystalline behavior due to the formation of thin-film from the dissolution of Cu-MOCs single crystal in the organic solvent with the phases as indexed in the (Figure S1b, Supporting Information). Hence, the crystal structures obtained from single-crystals and thin-film of synthesized Cu-MOCs dielectric material are consistent with Cu-MOCs formulation, as measured with SC-XRD and XRD, respectively. Also, energy-dispersive X-ray spectroscopy (EDX) was used to analyze the presence of various elements in Cu-MOCs dielectric formulation as shown in (Figure S1c, Supporting Information). The inset of (Figure S1c (inset), Supporting Information) shows the elemental composition table of Cu-MOCs material.

The glass transition temperature of Cu-MOCs dielectric formulation was obtained by thermogravimetric analysis (TGA) and differential scanning calorimetry (DSC) analysis. Figure 3b shows the TGA and DSC characteristics of Cu-MOCs dielectric material with temperature variation ranging from 25 to 450 °C under the nitrogen ambient. Distinctively, a three-step 1–3 steps weight loss process was observed at correspondingly three temperature ranges as 140–160, 230–260, and 280–300 °C, respectively. The first step-1 weight loss is mainly attributed to the removal of solvents trapped in the material and the unbound moisture.[44] The second step-2 of weight loss is unclear while the third step-3 of weight loss is due to the loss of organic ligands attached in the Cu-MOCs dielectric material. The total weight loss attributed to 73 wt% in Cu-MOCs, thereby, leading to 27 wt% of dielectric material remains in the form of inorganic copper oxide counterparts. The DSC characteristics likewise confirm the evolution of heat around temperature range 280–300 °C during the third step-3 of mass loss, which is mainly due to the decomposition of organic moieties present in Cu-MOCs dielectric material. Hence, the above noted high-temperature stability of synthesized Cu-MOCs dielectric

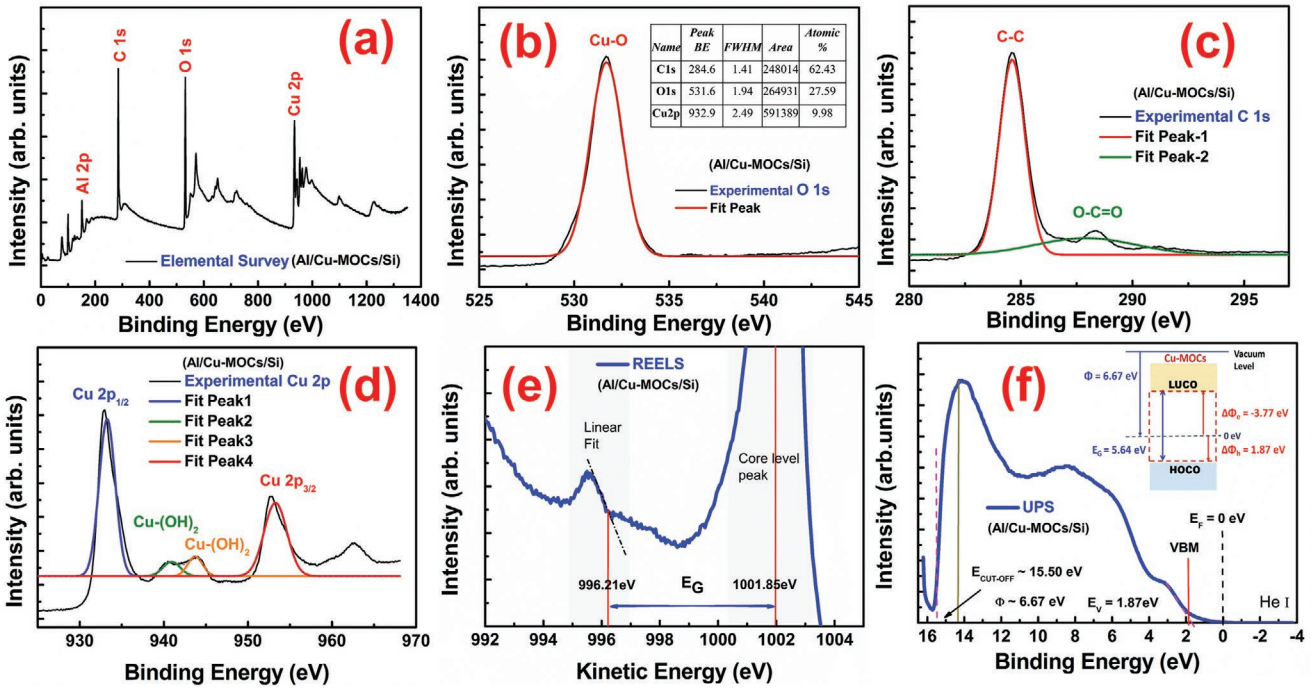

Figure 4. XPS analysis of Cu-MOCs dielectric material. a) Elemental survey scan constituting C 1s, O 1s, Cu 2p, and Al 2p peaks. b) O 1s peak spectra fitting. b-inset) XPS elemental survey scan peak table with peak BE, FWHM, area, and atomic percentages. c) C 1s peaks spectra fitting. d) Cu 2p peak spectra fitting. e) Bandgap measurement from REELS scan. f) Work function and HOCO band values measurement from UPS scan. f-inset) Energy band-level diagram of Cu-MOCs dielectric material.

material provides insights to its low-temperature processing and a good agreement to its easy integrability in semiconductor processing conditions.

Figure 4a shows the X-ray photoelectron spectroscopy (XPS) elemental survey scan of Cu-MOCs dielectric material constituting C 1s, O1s, Cu 2p, and Al 2p peaks. Here, the oxygen 1s, carbon 1s, and copper 2p peaks are clearly visible at the binding energies of 531.6, 284.6, and 932.9 & 952.7 eV, respectively. The aluminum 2p peak is observed due to the presence of aluminum electrodes in the Al/Cu-MOCs/Si MIS-CAP structures. Figure 4b shows the XPS spectra of O 1s peaks, where the first peak observed at 531.6 eV corresponds to the copper metal-oxygen bond in the Cu-MOCs system. The XPS elemental survey scan C 1s, O1s, Cu 2p peak table with peak binding energy (BE), full-width at half-maximum (FWHM), area, and the atomic percentages values are shown in Figure 4b (inset). In the C 1s peaks XPS spectra, the first peak observed at 284.8 eV is related to the C—C bond whereas the second peak identified at 288.7 eV is related to the O—C=O bond as shown in Figure 4c. The deconvoluted Cu 2p peaks XPS spectra are shown in Figure 4d. The peaks observed at 932.9 and 952.6 eV correspond to Cu $2p_{1/2}$ and Cu $2p_{3/2}$ compositions, respectively. The other shakeup satellite peaks of copper are identified at 940.2 and 944.1 eV, which depict the Cu-$(OH)_2$ auger peaks.

2.3. Energy Bands of Cu-MOCs

The bandgap (E_G) of dielectric Cu-MOCs thin film was determined using reflected electron energy loss spectroscopy (REELS) as described in Figure 4e. The measured $E_G \approx$ 5.64 eV wide-bandgap assuredly provides large band-offsets, thereby, offering a significant reduction in leakage currents caused by electrons as well as holes in the Cu-MOCs dielectric thin-films.[45] The work function (φ) and the position of the highest occupied crystal orbital (HOCO) ($\Delta\varphi_h$) were determined experimentally with ultraviolet photoelectron spectroscopy (UPS). These values are calculated to be $\varphi \approx 6.67$ eV and $\Delta\varphi_h \approx 1.87$ eV, respectively as shown in Figure 4f. The absolute positions of energy bands derived from REELS in Figure 4e and UPS in Figure 4f for Cu-MOCs dielectric material are represented with an energy-level diagram as shown in Figure 4f (inset). We further performed the XPS depth profile analysis of Cu-MOCs/Si thin films through argon ion etching at a constant time interval of 10 s as shown with etching profiles of O 1s, Cu 2p, C 1s, Si 2p in (Figure S2a–d, Supporting Information), respectively. As the Cu-MOCs was successively etched with time, XPS depth profiles show a continuous decrease in atomic concentrations of O 1s, Cu 2p, and C 1s until Cu-MOCs/Si interface is reached, as shown in (Figure S2a–c, Supporting Information), respectively. Also, it indicates an increase in the atomic concentration of Si 2p when the Cu-MOCs/Si interface is approached as shown in (Figure S2d, Supporting Information). Hence, depth etches profiles of O 1s, Cu 2p, C 1s, Si 2p verifies that first Cu-MOCs dielectric thin film was fully etched and further Cu-MOCs/Si interface was reached and thereafter silicon surface was approached as per anticipations.

Several inherent/intentional characteristics of metal-organic clusters are responsible for obtaining the desirable electronic

structure and a reasonable tradeoff between the obtained dielectric constant $\kappa \approx 5.49$ (described in Section 2.1) and bandgap $E_G \approx 5.64$ (described in Section 2.3), as in the case of novel copper-MOCs. The dielectric properties of MOCs are strongly governed by the type, size, composition, functionalization of organic linker molecules as well as inorganic metal nodes which can be utilized to engineer its bandgap and dielectric constant.[30,31] The Cu^{2+} metal node with open-shell metal ion[29], large radius, less electrical conductivity, high activation energy, charge density[31], and single valency as compared with counterpart metal nodes provide large bandgap and excellent insulating properties to the Cu-MOCs.[5,46,47] Small conjugated chains with a single COOH group attached to the benzene ring in m-Toulic acid (MTA) organic linker[48] along with the presence of acetonitrile in small quantities as a guest solvent molecule aid in achieving the desired large bandgap and high dielectric constant in the Cu-MOCs.[32,49] Also, without any intentional metal substitution as well as ligand functionalization in Cu-MOCs, it displays its inherent large bandgap, which is imperative for high-performance gate dielectric material for transistor applications.[47] Employment of polar high-$\kappa \approx 15.7$ ethyl lactate organic solvent and polar MTA organic linker molecules are certainly responsible for the existence of high polarization property in Cu-MOCs dielectric material.[7,33,50] Furthermore, the percentage composition of organic and inorganic components in metal-organic nanoclusters likewise strongly influence its polarizability properties and the overall bandgap engineering.[30,37] The low percentage of inorganic copper oxide (27%) and the high percentage of organic ligand (73%) are obtained as shown through TGA and DSC analysis of curves in Figure 3b. That's why less copper percentage indicates lesser availability of free charge carriers for conduction in the novel Cu-MOCs system. Whereas, the presence of high organic ligand composition offers a relatively lower mean free path to free charge carriers for conduction, which may be accountable for reducing leakage currents in Cu-MOCs dielectric. On top of this, the measured crystal size of Cu-MOCs nanocluster ≈1.6 nm as shown in Figure 3a confirms the existence of the highly compact nanocrystals arrangement and highly dense copper nanoclusters with nanosize pores location. The tight packing or minimal voids of nanoclusters leaves negligible space for guest molecules in slender pores' location providing very low conduction[48] and high dielectric constant.[33] In the present case, the small amount of guest acetonitrile solvent molecule may be present in the Cu-MOCs system during the low-temperature drying process in the air. This trivial number of guest-molecules in nanopore locations in Cu-MOCs/Si thin films also justifies high dielectric constant, low roughness, smooth and large area uniform thin film formations. Numerous metal-organic-frameworks counterpart materials[30] with comparatively large pore size exhibit low dielectric constant $\kappa < 2$, therefore, the presence of small pore size of developed uniform thin films of Cu-MOCs directly implies high dielectric constant $\kappa \approx 5.49$.[34,41] Adjacent to this, Cu-MOCs also show insulating properties due to poor overlap between copper node d-orbital and organic MTA π orbitals causing the charge to be highly localized.[25] Thus, the formulated novel Cu-MOC nanodielectrics provide enhanced dielectric properties paving their superiority for Al/Cu-MOCs/Si transistor applications.

2.4. Electrical Response of Al/Cu-MOCs/Si Structures

Capacitance–voltage (*C–V*) characteristics have been measured for Al/Cu-MOCs/Si MIS-CAP structures, to inspect the dielectric properties of newly developed Cu-MOCs gate dielectric thin films as shown in **Figure 5**. Figure 5a depicts the *C–V* characteristics of Al/Cu-MOCs/Si at 500 kHz along with corrected dynamic series resistance effect on MIS-CAP structures when stimuli gate voltage swept from −3.5 to 2.5 V at 0.1 V step. At negative gate bias voltage (−3.5 V) sweep, accumulation of majority carriers' holes occurred at Cu-MOCs/silicon interface which resulted in the capacitance, $C_{OX} \approx 5.53 \times 10^3$ pF cm^{-2} in the MIS-CAP structures. As the gate bias approached toward the positive side, accumulated holes at the interface, started to deplete and lead to a decrease in C_{OX}. Thereby, at the onset of the depletion, the computed flat-bands capacitance was $C_{FB} \approx 4.71 \times 10^3$ pF cm^{-2} at V_{FB} −1.66 V. Subsequently, with further sweeping of gate bias toward the more and more positive side, holes progressively repelled from Cu-MOCs/silicon interface making the depletion region widen evermore, eventually resulting in the decrease in Cu-MOCs/silicon interface hole density, and the corresponding increase in minority carrier's electron density, known as inverted Cu-MOCs/silicon interface. The computed threshold voltage (V_{TH}) at the onset of strong inversion and inversion capacitance, (C_{INV}) were $V_{TH} \approx 0.17$ V and $C_{INV} \approx 0.41 \times 10^3$ pF cm^{-2}, respectively. With the application of more positive gate bias toward 2.5 V, the weak inversion saturates to a strong inversion region. The smooth, large-capacitance, continuous *C–V* curves indicate the presence of high polarizability of Cu-MOCs dielectric and thus justifies its high dielectric constant as falling in line with the discussion in Section 2.1. The reasonably low flat-band and threshold voltages indicate good adhesion of Cu-MOCs and their compatibility with the silicon technology providing a device-level high-quality interface between Cu-MOCs/Si along with low RMS roughness. Hence, novel Al/Cu-MOCs/Si structures are proven as a potential candidature for low cost, high-performance, low-voltage operating MIS-CAP structures for next-generation CMOS logic circuits applications such as MOS-Cs and MOS-FETs applications.

To further establish the *C–V* characteristics and steadiness of Al/Cu-MOCs/Si structures, the variation in sweep delay measurements were performed to investigate the interface trap dynamics as shown in (Figure S3, Supporting Information).[51] *C–V* characteristics were measured at 0.02, 0.05, 0.1, 0.2, 0.5, 1 V s^{-1} sweep rates at 500 kHz with dynamic gate bias sweep from −3.5 to 2.5 V and a step of 0.1 V. As shown in (Figure S3, Supporting Information), *C–V* characteristics measured at all 0.02, 0.05, 0.1, 0.2, 0.5, 1 V s^{-1} sweep rates show invariance in accumulation, depletion as well as inversion capacitances, because, in typically at lower sweep rates, interface traps remain fairly in equilibrium with stimuli gate bias, yielding steady-state capacitance. Whereas at faster sweep rates, interface traps may not remain in equilibrium with gate bias and vary the measured capacitance.[52,53] Here, the insignificant variation in *C–V* characteristics, certainly indicates the presence of a reasonably less number of interface traps in Al/Cu-MOCs/Si structures. The presence of fewer interface traps indicates low RMS roughness, smooth, uniform, large-area thin films, and the better interface

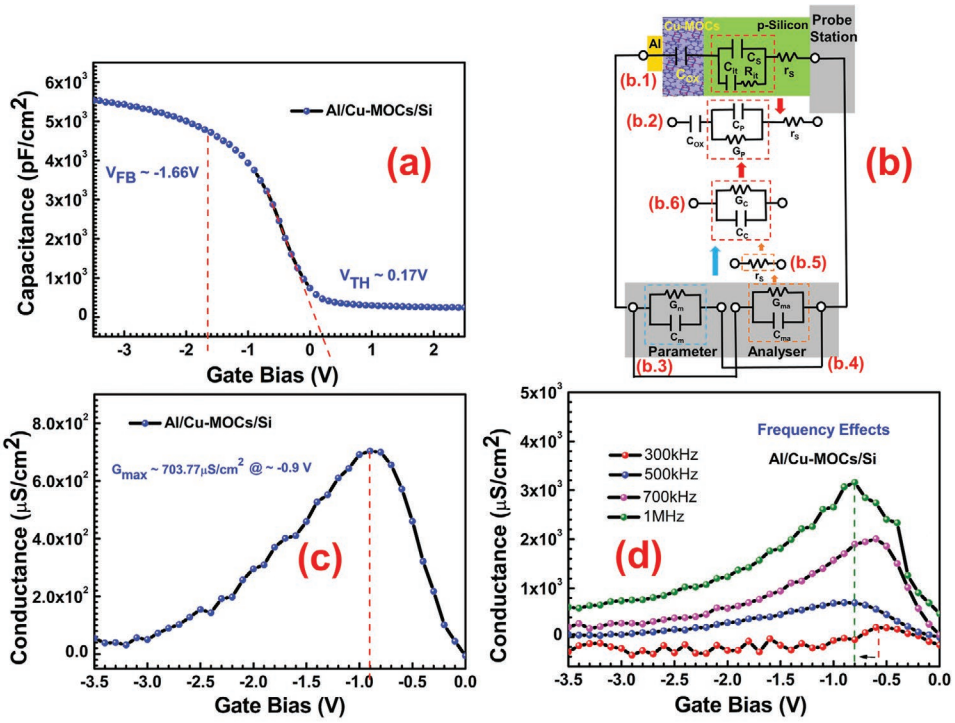

Figure 5. Electrical characteristics of Al/Cu-MOCs/Si MIS-CAP structures. a) Series resistance corrected *C–V* characteristics at 500 kHz. b.1) Equivalent electrical circuit of Al/Cu-MOCs/Si MIS-CAP structures including C_{OX}, C_S, C_{it}, R_{it}, and r_S. b.2) Parallel equivalent circuit of (b.1) including C_{OX}, C_P, G_P, and r_S. b.3) Equivalent measurement circuit of parameter analyzer containing C_m, G_m. b.4) Equivalent measurement circuit of parameter analyzer with MIS-CAP structures biased in strong accumulation region containing C_{ma}, G_{ma}. b.5) Equivalent of (b.4) containing series resistance r_S. b.6) Equivalent series resistance corrected circuit obtained from (b.3) and (b.5) containing G_C, C_C. c) *G–V* characteristics at 500 kHz. d) *G–V* characteristics at variable frequencies 300 kHz, 500 kHz, 700 kHz, and 1 MHz.

of Cu-MOCs dielectric with silicon, thereby, furnishing low conduction and high-performance of Cu-MOCs based MIS-CAP structures. Besides this, (Figure S4, Supporting Information) shows the dual-sweep cyclic *C–V* characteristics at 500 kHz frequency with gate bias voltage sweep from −3.5 to 2.5 V and a step of 0.1 V. Cyclic sweep *C–V* characteristics are essential for understanding the presence of effective oxide charges including fixed oxide charges (Q_F), trapped oxide charges (Q_{OT}), mobile ionic charges (Q_M) located at the Al/Cu-MOCs/Si systems as exhibited by bulk/deep-level traps, border/shallow traps and interface traps indicated in Figure 1b.7.[52,54] As shown in (Figure S4, Supporting Information), cyclic *C–V* was swept as forward sweep (black curve) from negative to positive gate bias of −3.5 to 2.5 V and reverse sweep (red curve) from positive to negative gate bias of 2.5 to −3.5 V. It was observed that the measured reverse sweep is slightly shifted left with shift $\Delta W \approx 0.08$ V toward the negative gate bias in comparison to forward sweep. This negligible shift window obtained with cyclic sweep indicates the negligible trapping/de-trapping of interface charges in Al/Cu-MOCs/Si structures.[55] However, the presence of a nonzero shift in negative flat band voltage V_{FB} of −1.66 V, toward the negative gate bias side, indicates the presence of positive fixed oxide charges (Q_O) at or very near Cu-MOCs/Si interface. The effective oxide charge density, N_{eff} (cm^{-2}) may be calculated by relation (equation S1, Supporting Information).[52] The effective oxide charge density for Al/Cu-MOCs/Si structures is calculated to be $\approx 1.1 \times 10^{11}$ cm^{-2}. Highly, smooth hysteresis-free *C–V* characteristics measure low trapping/de-trapping of effective oxide charges indicating defect-free, high-quality Cu-MOCs thin films thus providing excellent dielectric and charge storage properties with high dielectric constant and considerable bandgap as established in Section 2.3.

The corresponding electrical equivalent circuit for fabricated Al/Cu-MOCs/Si MIS-CAP structures is depicted through a schematic Figure 5b.1. Where, novel Cu-MOCs dielectric capacitance exhibits as C_{OX}, for Al/Cu-MOCs/Si structures, and C_S is the semiconductor capacitance, as a function of dynamic gate bias variation. In fact, the effective capacitance per unit area of the MIS-CAP structure will be a series combination of semiconductor capacitance (C_S) and dielectric capacitance (C_{OX}). Whereas the interface trap level can be expressed as a series combination *R–C* circuit including i) all parallel equivalent capacitances and ii) parallel equivalent conductance together to obtain a lumped equivalent parallel circuit comprising the interface trap capacitance C_{it} and interface trap resistance R_{it}.[56,57] Series resistance may be caused by various sources as described in (Section S1.1, Supporting Information). While most of the series resistance sources can be minimized by following standard optimized device fabrication & measurement protocols. Even though, there are certain parameters where the series resistance effect is difficult to estimate. Hence, the most general approach is to rectify the series resistance effect to apply a correction factor for it, which is known as series resistance (r_S).[57] For that reason, the most credible equivalent

circuits comprising of dielectric capacitance, C_{OX}, and possible contributors in the silicon as C_S, C_{it}, R_{it}, and r_S for Al/Cu-MOCs/Si structures are shown in Figure 5b.1. Likewise, the silicon equivalence of Figure 5b.1 can also be further expressed comprising of parallel capacitance (C_P) and undesirable parallel leakage path known as conductance (G_P), in series with dielectric capacitance (C_{OX}) and series resistance (r_S) as shown in Figure 5b.2. The magnitude of parallel capacitance (C_P) and parallel conductance (G_P) can be given by relations (1) and (2)[57]

$$C_P = C_S + \frac{C_{it}}{1+(\omega R_{it} C_{it})^2} \tag{1}$$

and

$$G_P = \frac{\omega^2 R_{it} C_{it}^{\ 2}}{q[1+(\omega R_{it} C_{it})^2]} \tag{2}$$

where $\omega = 2\pi f$, is the frequency, C_S is semiconductor capacitance, C_{it} is the interface trap capacitance, R_{it} is the interface trap resistance, and q is the electronic charge, respectively. To prevent small-signal energy loss in Al/Cu-MOCs/Si MIS-CAP structures, the series resistance is measured and applied correction factor for extraction of corrected *C–V* as well as *G–V* characteristics as shown in Figure 5a,c, respectively. The series resistance r_S is determined as discussed in Section S1.2 and equation (S2) (Supporting Information). As depicted in Figure 5b.6 the corrected series resistance, the values corrected capacitance $C_{C,}$ and corrected conductance G_C can be calculated from measured capacitance, conductance as shown in Figure 5b.3, and series resistance is shown in Figure 5b.5. The values of series resistance corrected capacitance C_C and corrected conductance G_C is given by relation (equations S3–S5, Supporting Information).[52] Also, the equivalent parallel conductance (G_P), as mentioned in Figure 5b.2, can be expressed in terms of C_C and G_C as illustrated in Figure 5b.6 and given by relation (equations S4–S6, Supporting Information).[56] In Figure S5 (Supporting Information), blue and red curves indicate with and without series resistance corrected *C–V* curves, respectively. In the accumulation region, after series resistance correction blue curve shows the marginally higher capacitance ΔC_C as compared to without a series correction red curve. This follows in line with the reason that the probable error in capacitance occurs in the accumulation and mainly depletion region. In the inversion region, $(\omega R_S C_C)^2 << 1$; hence, series resistance produces very little error. Also, the small value of ΔC_C indicates lesser effects and the existence of a small value of series resistance in the electrical characterizations of Al/Cu-MOCs/Si structures. This reveals that the optimized processing steps, standard measurement techniques, and the use of compatible Cu-MOCs dielectric material are utilized to minimize series resistance in the fabrication process of Al/Cu-MOCs/Si structures.

Figure 5c shows the series resistance corrected conductance–voltage (*G–V*) characteristics of Al/Cu-MOCs/Si MIS-CAP structures. In the *C–V* accumulation region at −3.5 V, minimum conductance (G_{min}) ≈ 38.88 μS cm^{-2} was measured. When increasing toward positive gate bias, the conductance curve rises slowly and reaches a sharp peak at ≈–0.9 V with maximum conductance value as G_{max} ≈ 703.77 μS cm^{-2} in the depletion region. Moving further right side toward increasing positive gate bias, conductance now decreases rapidly toward the onset to inversion region. This quick decrease in conductance as a function of gate bias in the inversion region symbolizes dominant small-signal energy loss is due to interface/shallow trap levels instead of bulk/deep-level trap levels.[52] The maxima of conductance (G_{max}) peak is useful in the calculation of interface trap density D_{it} (eV^{-1} cm^{-2}) by relation (equation S7, Supporting Information).[52] The computed value of interface trap density of Al/Cu-MOCs/Si structures is D_{it} ≈ 1.4×10^{11} eV^{-1} cm^{-2}. The sharp and small magnitude conductance peak with smaller FWHM indicates the presence of a smaller number of defects/interface traps density in uniform Cu-MOCs/Si structures, which indicates its good adhesion with silicon and hence, justifies its low RMS roughness, high dielectric constant, and bandgap. Also, dominant loss due to shallow/interface traps rather than deep-level/bulk traps indicates the formation of smooth large-area Cu-MOCs thin films with minimal uniformities aligning suitably with discussion in Section 2.1. At high frequencies, both capacitance and conductance measurements are affected by series resistance;[58] hence series resistance corrected (blue curve) and noncorrected (red curve) normalized *G–V* characteristics are shown in (Figure S6, Supporting Information) for Al/Cu-MOCs/Si structures. The series resistance corrected conductance G_C is extracted from *C–V* characteristics given by relation (equation S3, Supporting Information). As seen in Figure S6 (Supporting Information), only after series resistance correction, the sharp peak in conductance curve is obtained in the depletion region, as per description in Figure 5c. In comparison of Figures S5 and S6 (Supporting Information), it is observed that parallel *G–V* characteristics are more informative and prone to series resistance effects than the corresponding *C–V* characteristics. This indicates that the effects of series resistance are dominant only in the depletion region as compared to the accumulation and inversion region. Due to the marginal effects of series resistance on *C–V* and *G–V* curves, Al/Cu-MOCs/Si MIS-CAP structures are consistent with producing smooth, uniform large-area thin films interfaces containing fewer defects/interface traps for next-generation high-performance CMOS devices.

Figure 5d shows the effect of frequency variation on the series resistance corrected parallel conductance–voltage *G–V* characteristics in Al/Cu-MOCs/Si structures at frequencies 300 kHz, 500 kHz, 700 kHz, and 1 MHz, respectively. Correspondingly, Figure S7 (Supporting Information) shows the effect of frequency variation on the series resistance corrected capacitance–voltage *C–V* characteristics of Al/Cu-MOCs/Si structures at frequencies 300 kHz, 500 kHz, 700 kHz, and 1 MHz, respectively. In comparison to Figure 5d and Figure S7 (Supporting Information), it reflects that *C–V* characteristics are far less frequency-dependent, as compared to more prominent effects of frequency variations on *G–V* characteristics. Hence, the study of *G–V* characteristics is of more importance to grasp the effects of frequency variation on the Al/Cu-MOCs/Si structures interface. *C–V* characteristics in Figure S7 (Supporting Information) show only a slight shift in threshold voltage ΔV_{TH} ≈ 0.15 V toward the negative gate bias side with a change in frequency from 300 kHz to 1 MHz. *G–V* characteristics in Figure 5d show

a left shift (negative gate bias side) in the peak magnitudes of conductance increasing from 190, 700, 1900 to 3100 μS cm^{-2} with increasing frequency from 300 kHz, 500 kHz, 700 kHz to 1 MHz, respectively. This may be attributed that dielectric capacitance variation is in series with interface trap *R-C* network as specified in the equivalent electrical circuit of Al/Cu-MOCs/Si structures by Figure 5b.1.[52] Also, there is a $\Delta G_{max} \approx 0.4$ V shift in the maximum of conductance peak toward a gate bias closer to flat band voltage −1.66 V with the increase in frequency from 300 kHz to 1 MHz. This behavior may be attributed due to the different time responses of interface states.[43] Insignificant dependence on frequency by *C–V* and *G–V* characteristics of Al/Cu-MOCs/Si structures indicates their high polarizability thus manifesting a high dielectric constant of Cu-MOCs dielectric-based MIS-CAP structures. Hence, Cu-MOCs dielectric proves to be ideal candidates for high-quality MIS-CAP for next-generation logic and memory devices.

2.5. Leakage Current and Conduction

Figure 6a shows the gate leakage current density-voltage ($|J|$–V) characteristics for Al/Cu-MOCs/Si structures. Linear ramp voltage is applied to the gate and the resulting gate current is measured against changing dynamic gate bias as the minority charge carriers find a low energy pathway from gate to substrate producing leakage current. The leakage current may be caused by the presence of trap sites, such as interface traps, border/shallow traps, bulk/deep-level traps in the metal-organic-nanoclusters dielectric film, forming leakage paths along dielectric between gate and back contact.[59] When a negative gate bias voltage is applied to Al/Cu-MOCs/Si structures, in the accumulation region, carriers may attain sufficient energy to hop from one trap site to another reaching from Al/Cu-MOCs/Si interface through Cu-MOCs/Si system.[52] Hence, a gate leakage current of the order ≈67.37 nA cm^{-2} is measured at −3 V. As moved toward positive gate voltage, availability of fewer carriers may find the energy to hop from intermediate trap to trap originating in Al/Cu-MOCs/Si system causing much lesser gate leakage current ≈1.29 nA cm^{-2} at 1 V. When a large positive gate bias was applied, in the inversion region, gate current rises with a small slope and saturates to ≈6.04 nA cm^{-2} at 3 V. In this region, inverted minority carriers attain sufficient energy to hop between the adjacent lying traps or trap-assisted tunneling in the Cu-MOCs dielectric from Al/Cu-MOCs/Si structures. Partially ohmic characteristics are obtained from ln $|J|$–V plot of Al/Cu-MOCs/Si structures. Where, ln $|J|$–V characteristics in Figure 6a depict very low gate leakage current density from −5 to 5 V gate bias in Al/Cu-MOCs/Si structures with a minimum of ≈11.8 pA cm^{-2} at 0.63 V. Leakage currents described with Dielectric loss (D) (equation S11, Supporting Information) and corresponding percentage error of measurements (equation S12, Supporting Information) as a function of frequency ranging from 10 kHz to 1 MHz are shown in Figure S8 (inset) and S8 (Supporting Information), respectively. Percentage error of measurements of dielectric loss in Figure S8 (Supporting Information) reveals values well below (<1%) for the entire frequency range which indicates lower leakage currents in Al/Cu-MOCs/Si MIS structures. The presence of low leakage current density in Al/Cu-MOCs/Si structures indicates the excellent dielectric properties of Cu-MOCs and considerable bandgap.

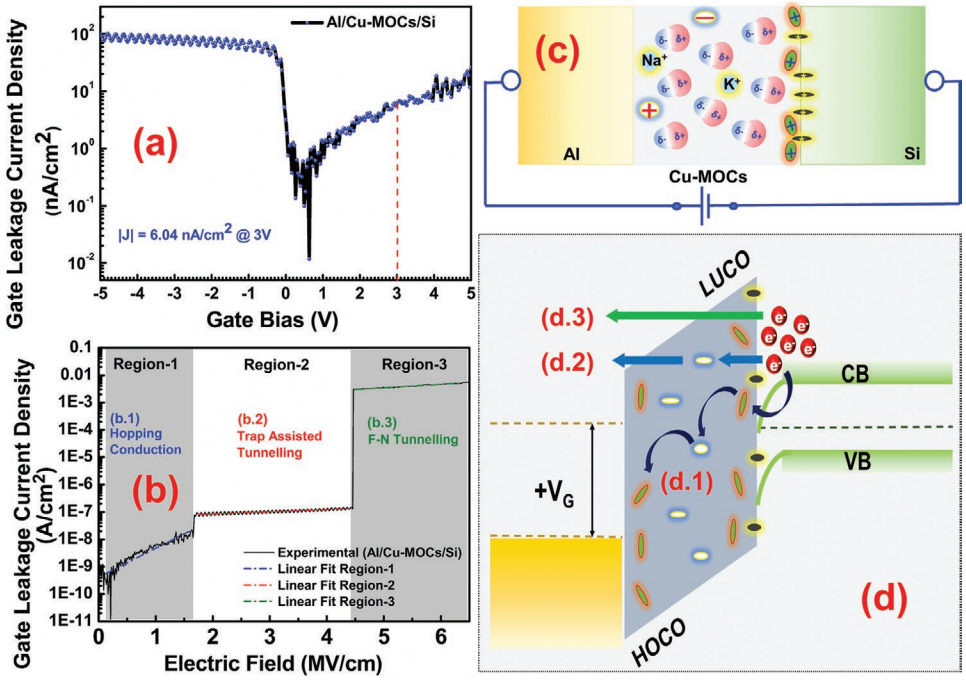

Figure 6. a) $|J|$–V characteristics of Al/Cu-MOCs/Si structures. b) $|J|$–E characteristics revealing current conduction mechanism of Al/Cu-MOCs/Si MIS-CAP structures at low and high electric fields. c) Schematic of Al/Cu-MOCs/Si MIS-CAP structures. d) Energy band bending diagram of Al/Cu-MOCs/Si structures when V_G is positive and $>V_{TH}$

Figure S9 (Supporting Information) shows the log gate leakage current density-electric field (ln $|J|$–E) characteristics for Al/Cu-MOCs/Si structures limited by breakdown of Cu-MOCs gate dielectric at $E_{BR} \approx 4.47$ MV cm^{-1}, high electric field. When $E_{applied} < 1$ MV cm^{-1}, the ln $|J|$–E characteristics before breakdown (blue curve) is arched down and increases till 1 MV cm^{-1}, reveals a low leakage at the lower field. After $E_{applied} > 1$ MV cm^{-1}, ln $|J|$–E characteristics before breakdown (blue curve) becomes arched up, indicating a rise in leakage current with increasing in the field. Whereas, at a high electric field of $E_{BR} \approx 4.47$ MV cm^{-1}, the ln $|J|$–E characteristics (red curve) are arched down with steep slope, indicates the breakdown limit of Cu-MOCs dielectric for Al/Cu-MOCs/Si structures, where leakage current rises quickly. The red curve depicts a $\approx 10^5$ orders higher gate leakage current density as compared to the blue curve. That's why ln $|J|$–E characteristics in Figure S9 (Supporting Information) reflect a considerable high value of breakdown field for Al/Cu-MOCs/Si structures. A high value of the break-down field of Al/Cu-MOCs/Si structures justifies the presence of high-κ of Cu-MOCs with considerable bandgap. Figure 6b shows the current conduction mechanism of Al/Cu-MOCs/Si structures for $|J|$–E characteristics with as specified three distinguishable regions. Region-1, 2, 3 are defined from b.1) 0–1.75 MV cm^{-1}, b.2) 1.8–4.40 MV cm^{-1}, and b.3) 4.45–6.46 MV cm^{-1}, respectively with corresponding differences in their slopes. In the very low electric field of (b.1) region-1 from 0 to 1.75 MV cm^{-1}, $|J|$–E plot shows a linear slope ≈ 1 as shown in the linear fit of plot ln (J)–E (Figure S10a and equation S8, Supporting Information). It attributes to conduction through the hopping mechanism for Al/Cu-MOCs/Si structures.[60–62] When the applied electric field further increases as shown in (b.2) region-2 from 1.8 to 4.40 MV cm^{-1}, the slope of $|J|$–E graph was far below ≈ 0.08, and ln (J/E)–$E^{1/2}$ plot fitting did not justify the experimental values of leakage current density of region-2. Thus, the ln (J)–$1/E$ plot was sketched for the region-2, which gives a linear fit indicating the presence of trap assisted tunneling mechanism as shown in Figure S10b and equation S9 (Supporting Information).[56,63] Furthermore, at the higher electric field, $E_{BR} \approx 4.47$ MV cm^{-1} of region-3, breakdown of Al/Cu-MOCs/Si structures occurred in which the current various abruptly. Plot ln (J/E^2)–$1/E$ was sketched to test a linear fit, which indicates the presence of partial F-N tunneling mechanism in the region-3 as shown in Figure S10c and equation S10 (Supporting Information).[64,65] With the low leakage current density in Al/Cu-MOCs/Si structures even at high voltages, it justifies the less presence of defects/interface trap density and less effective oxide charges as also outlined in Section 2.4. The low conduction due to hopping, trap-assisted tunneling mechanisms support the excellent high-κ properties of Cu-MOCs gate dielectrics. Hence, Al/Cu-MOCs/Si MIS structures demonstrate their exemplary candidacy for next-generation CMOS logic circuits and devices.

Figure 6c shows the schematic of Al/Cu-MOCs/Si MIS structures, which presents high-κ Cu-MOCs dielectric guided with polar covalent van der Waals dipole moments comprising of less effective oxide charges and less bulk/shallow trap densities as described in Section 2.4. Under the dynamically applied bias, the inherent dipole moments align themselves in the direction of the external stimuli applied electric fields.[66] Figure 6d shows the energy band diagram of Cu-MOCs based on Al/Cu-MOCs/Si MIS-CAP structures. The actual band positions of MOCs differ with the metal centers and organic ligands systems.[67] The metal-organic crystal (Cu-MOC) based dielectric thin film may be articulated with molecular orbital or solid-state energy band or metal nodes based periodic solids.[68] Combining the molecular functionalities and control of solid-state systems, the Cu-MOC materials may be modeled with a more localized highest occupied crystal orbital (HOCO) and lowest unoccupied crystal orbital (LUCO). Here, HOCO and LUCO levels are separated correspondingly by the energy or bandgap (as described in Section 2.3) approximated to the same energy gap likewise between delocalized valence and conduction bands in the inorganic systems.[5,47,69] At equilibrium, the Fermi level of Al, Cu-MOCs, and Si are aligned at the specified flat band voltage as shown in Figure S11a (Supporting Information). When the applied gate voltage (V_G) is less than the flat band voltage (V_{FB}), the silicon band bends downward in response to the applied gate voltage. Although, developed Cu-MOC dielectric materials fundamental conduction understanding, certainly are far away from well-established inorganic high-κ dielectrics that govern standard charge transport based band bending, hence, the most conceivable conduction mechanism in Cu-MOCs system, might be charge carriers hopping.[26,60–62] As shown in Figure S11b (Supporting Information), the current conduction may be limited by the hopping mechanism at small negative voltages as discussed in Figure 6b.1. Here, charge carriers are localized at specific nonbonded sites with discrete energy levels and hop between neighboring trap sites.[26] Afterward, when applied gate bias (V_G) conceals at $V_{FB} < V_G < V_{TH}$ results the silicon bands bend slightly upward and conduction once more limited by hopping as shown in Figure S11c (Supporting Information). Furthermore, when applied V_G is greater than V_{TH}, silicon bands bend more upward as shown in Figure 6d, and current conduction is governed by interface-trap assisted tunneling (blue arrow) at low electric fields and partial F-N tunneling (green arrow) at high fields as discussed in Figure 6b. Trap assisted tunneling is aid by low energy electrons tunneling to the intermediate interface, border/shallow traps, bulk/deep-level traps[70], and corresponding triangular barrier. However, F-N tunneling is aid by electrons that have sufficient energy to directly overcome the triangular barrier.[65] Hence, the energy band bending diagram proposed for high-κ, considerable bandgap, large area uniform Cu-MOCs thin films dielectrics based Al/Cu-MOCs/Si structures are in line with the current conduction mechanism, as discussed in Figure 6b and truly justifies the MIS-CAP systems.

2.6. Reliability Tests

In order to determine the reliability of fabricated Al/Cu-MOCs/Si structures, the analysis related to variable positive and negative constant-voltage electrical stress (CVS) on the C–V and $|J|$–V characteristics of Al/Cu-MOCs/Si structures were performed at room temperature.[51] **Figure 7**a shows the C–V characteristics at applied positive voltage stresses of 5, 10, 15, 20 V voltage on Al/Cu-MOCs/Si structures at 500 kHz with dynamic gate bias sweep from – 3.5 to 2.5 V with a step of 0.1 V. With

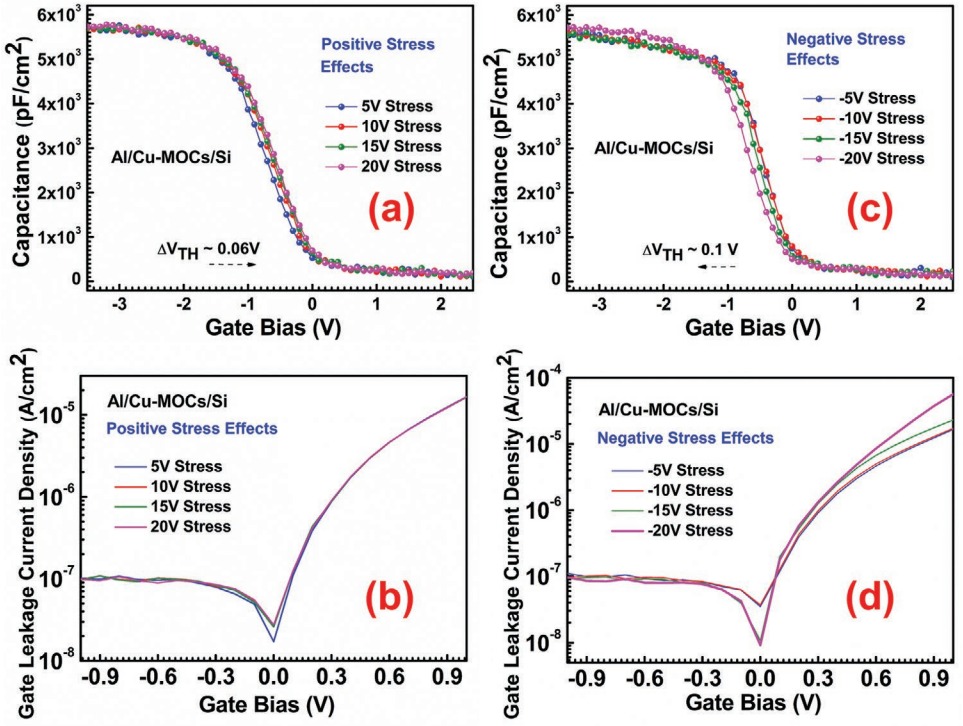

Figure 7. a) *C–V* characteristics of Al/Cu-MOCs/Si structures with 5, 10, 15, 20 V positive stress voltages. b) $|J|$–*V* characteristics of Al/Cu-MOCs/Si structures with 5, 10, 15, 20 V positive stress voltages. c) *C–V* characteristics of Al/Cu-MOCs/Si structures with −5, −10, −15, −20 V negative stress voltages. d) $|J|$–*V* characteristics of Al/Cu-MOCs/Si structures with −5, −10, −15, −20 V negative stress voltages.

the increasing application of CVS with positive stress voltages from 5 to 20 V, no considerable change was observed in the accumulation region of *C–V* characteristics from gate bias −3.5 to −1.66 V. Similarly, no considerable change was also noticed in the inversion region of *C–V* characteristics from gate bias 0.17 to 2.5 V. Slight shift in threshold voltage $\Delta V_{TH} \approx 0.06$ V of *C–V* curve toward positive gate bias side was detected with the variation of positive stress voltages from 5 to 20 V. It indicates the increased accumulation of minority charge carrier's density in the inversion region at the Al/Cu-MOCs/Si systems, due to the application of additional positive stress voltages. Figure 7b shows the effect of CVS with positive stresses of 5, 10, 15, 20 V voltages on the $|J|$–*V* characteristics with the voltage sweep from −1 to 1 V and a step of 0.1 V. With the increasing positive stress voltages from 5 to 20 V, no sizable change in $|J|$–*V* characteristics on either side of positive and negative gate voltages were observed. At much high stress of 20 V, a slight increase in gate leakage current density $\Delta J \approx 10.3$ nA cm^{-2} was observed. Similarly, Figure 7c shows the *C–V* characteristics at CVS with negative stresses of −5, −10, −15, −20 V with bias voltage sweep from −3.5 to 2.5 V and a step of 0.1 V at 500 kHz frequency. With the increasing application of negative stress from −5 to −20 V, no substantial change is observed in the inversion region of *C–V* characteristics from gate bias 0.17 to 2.5 V. However, with increasing application of negative stress from −5 to −20 V, a slight increase in capacitance $\Delta C \approx 2.6 \times 10^2$ pF cm^{-2} was noticed at a gate bias of − 2.5 V. Figure 7d shows the effect of negative stresses −5, −10, −15, −20 V on the $|J|$–*V* characteristics with bias sweep from −1 to 1 V and a step of 0.1 V. With the increase of negative stresses from −5 to −20 V, insignificant change in $|J|$–*V* characteristics was observed. However, a slight increase in gate leakage current density $\Delta J \approx 9.9$ μA cm^{-2} was observed at 1 V gate bias. Also, a small decrease in gate leakage current density $\Delta J \approx 25.7$ nA cm^{-2} was observed at 0.1 V. At much higher stress voltages of −20 V, the minimum leakage current density ≈9.17 nA cm^{-2} was observed at 0.1 V. Hence, the investigated Al/Cu-MOCs/Si structures demonstrate a considerable degree of electrical reliability with the application of CVS even at higher positive and negative electrical stresses. This also justifies the high performing electrical properties such as high-κ of Cu-MOCs in real-time conditions for next-generation CMOS and memory device applications. Table 1 compares figures of merit in terms of the electrical parameters' performance of high-κ, Cu-MOCs gate dielectric-based Al/Cu-MOCs/Si structures with earlier reported inorganic, organic, and metal-organic-frameworks gate-dielectric materials-based MIS-CAP structures.

Figure 8 shows the benchmarking of threshold voltage versus dielectric constant of Al/Cu-MOCs/Si MIS structures as related with previously reported MOFs, inorganic, and organic dielectrics based p-MIS structures[43,55,72,77,80,81]. The fabricated Al/Cu-MOCs/Si MIS structures reported a dielectric constant of ($\kappa \approx 5.49$), and threshold voltage of (≈0.17 V), respectively as shown in Figure 8. Cu-MOCs dielectric based Al/Cu-MOCs/Si MIS structures, exhibit positive threshold voltage as compared to mainstream, especially inorganic dielectric based MIS structures[55,77,81]. Also, Cu-MOCs show high dielectric constant in comparison with state-of-art

Table 1. Electrical performance comparison of previously reported metal–insulator structures comprising inorganic, organic, and metal-organic-framework dielectrics with this work.

Fabricated device structure	Type of dielectric (organic/inorganic/MOFs)	Dielectric capacitance, C_{OX} (F cm^{-2})	Gate leakage current density, $\|J\|$ (A cm^{-2})	Break down voltage, V_{BR} (MV cm^{-1})	Device operating voltage, V_G (V)	References
Ag/2DMF.EtOH/Ag	MOF	–	1×10^{-7}	0.5	0 to 10	[20]
Al/$Cu_3(BTC)_2$/SiO_2/p-Si	MOF	9×10^{-8}	–	–	–4 to 1	[43]
Pt/Er_2O_3 (RTA)/Si/Pt	Inorganic	1×10^{-6}	4×10^{-7}	–	–3 to 3	[55]
Pt/Ti/HfO_2/$SrFeO_xF_y$/SiO_2/Si	Inorganic	5×10^{-7}	1×10^{-7}	4	–5 to 5	[71]
Au/Hydrocarbon/Si	Organic	6×10^{-6}	1×10^{-5}	10	–4 to 4	[72]
Al/Al_2O_3/Si	Inorganic	9×10^{-7}	2×10^{-8}	6.4	–4 to 4	[73]
Ni/α-Ga_2O_3/Si	Inorganic	5×10^{-8}	8×10^{-7}	3.3	–2 to 2	[74]
Ni-Au/AlN/Si	Inorganic	4×10^{-8}	–	–	–20 to 20	[75]
Al/Al_2O_3/n-Si	Inorganic	8×10^{-7}	2×10^{-10}	7	–3 to 3	[76]
Pt/La_2O_3/SiO_X N_Y/Si/Pt	Inorganic	2×10^{-8}	3×10^{-8}	–	–4 to 2	[77]
Ni/Au/HfO_2/Y_2O_3/AlGaN/GaN/Ti/Al	Inorganic	3×10^{-7}	5×10^{-11}	7.1	–6 to 6	[78]
Ti/Al/Ni/TiN/SiN_x/AlGaN/GaN	Inorganic	2×10^{-7}	1×10^{-9}	4.0	–8 to 4	[79]
Al/Cu-MOCs/p-Si	MOC	5×10^{-9}	9×10^{-11}	4.4	–3.5 to 2.5	This work

MOFs based dielectrics[43,80]. Hence, Al/Cu-MOCs/Si MIS structures stand tall with high performance operations, and being highly desirable for futuristic CMOS transistor applications.

3. Conclusions

The novel low-cost metal-organic linker nanoclusters Cu-MOCs were successfully synthesized by the eco-friendly low-temperature sol-gel method. Cu-MOCs gate-dielectric material fabricated Al/Cu-MOCs/Si MIS-CAP structures illustrate high dielectric constant (high-κ), bandgap, and large-area thin-films uniformity. Systematic material characterizations such as SC-XRD, TGA, DSC, EDX, XPS, AFM, FESEM, and electrical characterizations such as *C–V*, *G–V* and $|J|$–*V*, and CVS demonstrate uniform, low roughness, large-area thin films with high capacitance density, very low gate-leakage current–density, reduced operating voltage, lesser defects/interface states, lesser effective oxide charges, negligible effects of CVS, and a broad range of operating frequencies. Hence, novel metal organic-linker Cu-MOCs based high-κ gate dielectric is substantiated its potential as one among the best candidates for replacing conventional inorganic/organic dielectric materials as active gate materials for future high-performance DRAM-CMOS and in other semiconducting device applications such as MOS-Cs, MOS-FETs, and sensors, etc.

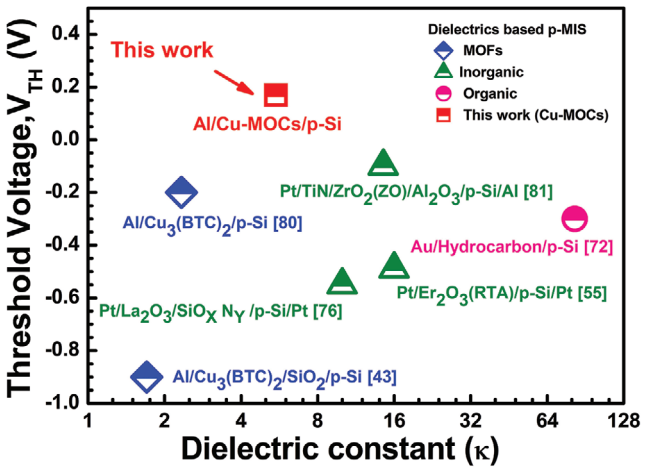

Figure 8. Benchmarking threshold voltage versus dielectric constant for Al/Cu-MOCs/Si MIS structures in this work with the state-of-the-art MOFs, inorganic, and organic dielectric based p-MIS applications.

4. Experimental Section

Materials: Copper acetate hydrate ($Cu(CH_3COO)_2$. H_2O), triethylamine ($C_6H_{15}N$), and ethyl acetate ($C_4H_8O_2$), acetonitrile (C_2H_3N) were purchased from S D fine-chemicals. Ethyl lactate ($C_5H_{10}O_3$) was purchased from TCI. 3-methyl benzoic acid ($C_8H_8O_2$) was purchased from Merck. All the materials were used without any purification.

Synthesis of Copper-Metal-Organic Nanoclusters: First, 1.8 g of copper acetate hydrate was mixed with 7.5 mL of ethyl acetate by magnetic stirring to form solution A. After that, 9.8 g of m-Toluic Acid, 1.4 g of trimethylamine, and 15 mL of ethyl acetate were mixed to form solution B. Then solution B was slowly added into solution A dropwise at 60 °C with continuous stirring. The reaction was performed at 60 °C for 24 h as shown in Figure 1a and the final product was washed with acetone and dried in an oven at 60 °C for 12 h. The 10 wt% synthesized Cu-MOC dielectric nanoclusters were dissolved in the acetonitrile solvent and were kept undisturbed at room temperature for 7 d to crystallize into a single crystal.

Cu-MOCs Spin-Coating Solution Preparation: The fresh oven-dried 20 mg of Cu-MOCs material was dissolved in 2 mL of ethyl lactate solvent by the aid of the vortex mixture without exposure to air ambient. The above mixture was put to mixing for 10 min until the powder was completely dissolved in the solvent to result in a

clear blue-colored solution. This solution was filtered twice with a 0.22 µm pore-size syringe filter to obtain a uniform solution C for spin coating.

Fabrication of Metal–Insulator–Semiconductor Capacitor (MIS-CAP) Structures: p-type (100) silicon wafers with 300 µm thickness, 2–10 Ω cm resistivity substrates were utilized for fabrication of MIS transistor structures in class 100 cleanroom facility. Substrates were cleaned using a standard RCA cleaning procedure. Silicon wafers were first cleaned in RCA 1 to remove organic impurities, followed by RCA 2 to remove inorganic impurities. HF dip cleaning was performed to remove the native oxide, SiO_2 contamination. Finally, ultraclean wafers were nitrogen blow-dried for the deposition of dielectric material for MIS-CAP structures as shown in Figure 1b.1. Freshly prepared Cu-MOCs solution C was spin-coated onto RCA cleaned silicon wafers with 2000 rpm for 30 s, with a ramp-up time of 10 s as shown in Figure 1b.3. The spin-coated wafers were kept on the hot plate at 85 °C for 120 s for drying up the solvent. A clear uniform thin-film of Cu-MOCs dielectric was formed for the fabrication of MIS-CAP structures as shown in Figure 1b.5. For gate electrode deposition, circular aluminum metal electrodes were deposited and patterned through a standard shadow mask technique. Thermal evaporation was performed from aluminum pellets at 12–14 amperes current, 2.5×10^{-6} torr chamber pressure to deposit the thin film of ≈100 nm for best results as shown in Figure 1b.6. Al/Cu-MOCs/p-Si structures were fabricated using a simple, cost-effective sol-gel method for CMOS logic applications.

Material Characterizations: For systematic material characterizations, surface roughness and morphology of Cu-MOCs thin films were first observed with AFM (Dimension Icon, Bruker) and next with field emission scanning electron microscopy (FE-SEM, Gemini SEM 500, Zeiss, Germany). The grown single-crystal of Cu-MOCs was characterized by single-crystal X-ray diffraction (SC-XRD, Model-Supernova, Rigaku) to obtain detailed crystal structure, whereas, the synthesized Cu-MOCs formulation and thin-films were characterized by X-ray diffraction (XRD, Smart Lab 9 kW rotating anode x-ray diffractometer, Rigaku corporation) to obtain the lattice planes and crystalline nature of Cu-MOCs systems, respectively. XRD was analyzed from the 2θ range from 5° to 80° with the scan speed of 2° min^{-1}. Energy-dispersive X-ray spectroscopy (EDX) was applied to check the presence of various elements and elemental mapping was performed to check the distribution of elements. TGA and DSC (STA 449 F1 Jupiter, NETZSCH) were performed from room temperature to 450 °C in a nitrogen atmosphere at 10 °C min^{-1} for analysis of thermal stability and study of heat absorption and evolution, respectively. The chemical and electronic states of Cu-MOCs were analyzed through X-ray photoelectron spectroscopy (XPS, Nexsa base, Thermo Fisher Scientific). The XPS survey scan spectra were recorded from 0 to 1350 eV binding energy. The depth profile was performed using XPS by etching the surface of Cu-MOCs/Si through low energy argon ions until the interface of Cu-MOCs/Si was achieved. REELS and UPS scans were performed using (XPS, Nexsa base, Thermo Fisher Scientific).

Electrical Characterizations: For this study, the electrical characteristics of fabricated Al/Cu-MOCs/p-Si structures were performed using Keithley 4200 SCS as shown in Figure 1b.7. *C–V*, *G–V* characteristics were performed at room temperature and 500 kHz frequency. The measurements were conducted with a small AC signal of 25 mV and by sweeping the DC gate bias from − 3.5 to 2.5 V. The frequency-dependent dynamic *C–V* and *G–V* characteristics were carried out at a frequency range of 300 kHz to 1 MHz at room temperature. $|J|$–*V* characteristics pre and post breakdown was performed at room temperature from −5 to 5 V DC gate bias. Electrical stress analysis of *C–V* and *I–V* characteristics were also performed with CVS positive and negative stress ranges from +5 to +20 V and −5 to −20 V, respectively. Also, the surface morphology and roughness of Cu-MOCs dielectric thin films were analyzed by using an atomic force microscope (AFM) from Bruker Dimension Icon in tapping mode. The thickness of dielectric Cu-MOCs thin films and aluminum electrodes were measured using ellipsometry from Accurion EP4 Ellipsometer using the Sellmaier model for Cu-MOCs dielectric.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

high-κ dielectrics, metal–insulator–semiconductors, metal-organic nanoclusters

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