Applied Physics Letters

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Cite as: Appl. Phys. Lett. **119**, 063505 (2021); https://doi.org/10.1063/5.0055792
Submitted: 03 May 2021 • Accepted: 25 July 2021 • Published Online: 12 August 2021

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Applied Physics Letters ARTICLE scitation.org/journal/apl

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Shivendra K. Rathaur,[1,2] Robin Khosla,[1,3,4] and Satinder K. Sharma[1,a)]

AFFILIATIONS

[1]School of Computing and Electrical Engineering, Indian Institute of Technology (IIT)-Mandi, Mandi 175075, Himachal Pradesh, India
[2]Department of Electrical Engineering, Indian Institute of Technology (IIT)-Delhi, Delhi 110016, India
[3]Institute of Semiconductor Engineering, University of Stuttgart, Pfaffenwaldring 47, 70569 Stuttgart, Germany
[4]Department of Electronics and Communications Engineering, National Institute of Technology (NIT), Silchar, Assam 788010, India

[a)]**Author to whom correspondence should be addressed:** satinder@iitmandi.ac.in

ABSTRACT

Extended data retention is a cardinal impediment for ferroelectric memories and serves a pivotal role for nonvolatile memory applications. Here, nonvolatile Metal–Ferroelectric–Insulator–Semiconductor (MFIS) structures are fabricated by using thin films of Strontium Bismuth Tantalum Oxide ($SrBi_2Ta_2O_9$) as ferroelectric and high-κ lanthanum oxide (La_2O_3) as a buffer insulator on p-Si substrates via RF magnetron sputtering. The grazing incidence x-ray diffraction analysis confirms the dominant (111) and (115) ferroelectric perovskite phases of $SrBi_2Ta_2O_9$ thin films. Albeit, atomic force microscopy surface micrographs revealed highly smooth La_2O_3 and SBT ($SrBi_2Ta_2O_9$) thin films with a surface roughness of $\sim 0.22 \pm 0.04$ nm and $\sim 1.05 \pm 0.03$ nm, respectively. Capacitance–voltage (C–V), capacitance–time (C–T), and current–voltage (I–V) characteristics of Pt/$SrBi_2Ta_2O_9$/La_2O_3/Si, MFIS structures, exhibited a high memory window of ~ 1.1 V at ± 5 V sweep voltage, data retention measured until $\sim 10^4$ s even on the extrapolation up to 10 years, and a low leakage current density of ~ 12.8 μA/cm^2 at -1 V and 300 K. Far from it, the probed conduction mechanism is studied for Pt/$SrBi_2Ta_2O_9$/La_2O_3/Si MFIS device structures. The optimum nonvolatile memory characteristics are attributed to the high-quality SBT ferroelectric and the buffer layer La_2O_3/Si interface of the investigated MFIS structure and also assert from the control Pt/SBT/Pt and Pt/La_2O_3/Si results. Thus, the proposed Pt/$SrBi_2Ta_2O_9$/La_2O_3/Si structure is a potential candidate for a gate stack of one-transistor (1T) type Ferroelectric Field-Effect Transistors nonvolatile memory applications.

Nonvolatile memories (NVMs) retain their data storage even when power is turned off. From the class of NVM, ferroelectric random access memory (FeRAM) draws much attention due to its low power consumption, fast read/write speed, high security, good retention, and endurance time.[1] FeRAM finds a wide range of applications in low memory density devices, consisting of a 1T–1C structure with a destructive readout operation similar to dynamic random access memory (DRAM). On the other hand, the 1T type structure where the ferroelectric is integrated into the gate stack is called a Ferroelectric Field Effect Transistor (FeFET).[2] In front of FeRAM, FeFETs offer the additional advantage of nondestructive readout and the need for a single 1T element, which performs both switching and storage. While 1T FeFET is generally investigated using a metal/ferroelectric/insulator/semiconductor (MFIS) device structure, it prevents interdiffusion and interface reactions and provides better insulation amidst ferroelectric to the semiconductor surface.[3] Hence, it results in superior device performance and reliability. The major challenge for FeFETs to compete with the state-of-the-art NVM is to achieve a reasonable memory window (preferably multilevel), scaling concern related to low cost-per-bit, and good reliability,[4,5] incredibly long data retention of greater than 10 years.[6,7]

In MFIS structures as described above of FeFETs, the ferroelectric material must have high-κ, low leakage current density, reasonable remanent polarization (P_r), coercive field (E_c), and high thermal budget for integration with compatible front-end-of-line (FEOL) complementary-metal–oxide–semiconductor (CMOS) technology. The insulating material must have a high dielectric constant to avoid high voltage drop across the buffer layer, good interface with a semiconductor, low leakage

current, and good thermal stability.[8] A good deal of ferroelectric materials, like $BaTiO_3$,[9] $BiFeO_3$,[10] Pb(Zr, Ti)O_3,[11] $SrBi_2Ta_2O_9$ (SBT),[12] and Fe-HfO_2,[13] are investigated for FeFETs. Bi-layer perovskite structures based on SBT show an excellent endurance of $>10^{12}$ cycles, crystallization temperature up to 800 °C compatible with FEOL processing, and decent P_r (~5–10 μC/cm^2) and E_c (0.03–0.05 MV/cm) values.[11,12] Alternatively, numerous high-κ insulator layers, like Al_2O_3,[14] HfO_2,[15,16] TiAlO,[17] TiON,[18,19] and so on,[20,21] are investigated as a buffer layer of ferroelectric memories.[6,22] Among these, La_2O_3 is an attractive candidate for the buffer layer due to its high dielectric constant (~27), high bandgap (>6 eV), large conduction band offset with Si (>2 eV), and low leakage current density even at lower effective oxide thickness (EOT) < 1 nm.[23]

This Letter reports Pt/SBT/La_2O_3/Si, MFIS structures for nonvolatile memory applications. The crystallinity of SBT thin films is analyzed using grazing incidence x-ray diffraction (GIXRD) to confirm the ferroelectric phase of SBT. The surface topography of La_2O_3 and SBT thin films is evaluated using atomic force microscopy (AFM). The electrical characteristics, i.e., memory, data retention, and leakage characteristics, along with the current conduction mechanism, at 300 K, are systematically investigated using capacitance–voltage (*C–V*), capacitance–time (*C–T*), and current–voltage (*I–V*) measurements, respectively. Additionally, the ferroelectricity of SBT is confirmed through pulse current–time (*I–T*) measurements of the Pt/SBT/Pt, Metal/Ferroelectric/Metal (MFM) system. Also the quality of the buffer layer is validated in Pt/La_2O_3/Si, Metal/Oxide/Semiconductor (MOS) structures using the *C–V* and *I–V* measurements.

The Pt/SBT/La_2O_3/Si (MFIS), Pt/La_2O_3/Si/Pt (MOS), and Pt/SBT/Pt/Ti/SiO_2/Si (MFM) structures are fabricated on standard RCA cleaned p-Si (100) with a resistivity of ~8–12 Ω-cm. For Pt/SBT/La_2O_3/Si MFIS structures fabrication, after RCA cleanings and HF dip, the insulating buffer layer (La_2O_3) was deposited using the lanthanum oxide sputter target (purity 99.99%) by RF magnetron sputtering. La_2O_3 thin films are deposited by sputtering at RF power 60 W, Ar (100 sccm) at 300 K followed by *in situ* post-deposition annealing (PDA) at ~700 °C in N_2 for 30 min to improve the quality of the buffer layer. The ferroelectric SBT thin films are also deposited by RF Magnetron sputtering at the RF power of 60 W, Ar (100 sccm) at 300 K, followed by *in situ* PDA at ~700 °C in O_2 for 1 h to form the desired ferroelectric phase of SBT. For the deposition of thin films by RF Magnetron sputtering, the base pressure, process pressure, and annealing pressure were maintained at ~2×10^{-6}, ~5×10^{-3}, and ~6×10^{-3} mbar, respectively. Also pre-sputtering is done for ~10 min to remove any impurities present on the target surface before the deposition on the active surface. Herein, to take care of the hygroscopic nature of La_2O_3, the thin films of La_2O_3 and SBT are deposited and thermally annealed *in situ* in a controlled environment without breaking the vacuum. Furthermore, the thickness of deposited La_2O_3 and SBT thin films is estimated to be ~10.2 ± 0.6 nm and ~115 nm by the Accurion EP4 imaging Ellipsometer using the Cauchy model. For metal contacts, platinum (Pt) ~60 nm of purity 99.99% is sputtered by DC magnetron sputtering at the DC power of 35 W, Ar (40 sccm) at 300 K via shadow mask with circular dots of area ~2.5×10^{-3} cm^2 for top contact to complete the fabrication of MFIS structures. Likewise, following the similar fabrication process steps, control Pt(~60 nm)/SBT(~155 nm)/Pt(~60 nm), MFM structures were also fabricated on Ti(~10 nm)/SiO_2/Si substrates. Subsequently, Al/La_2O_3/Si, MOS structures were fabricated to confirm the ferroelectric polarization and the quality of the La_2O_3 buffer layer, respectively. The electrical characteristics of all the fabricated devices investigated using the Keithley SCS 4200 system equipped with a cascade four-probe station. GIXRD spectra of SBT/Si structures were recorded using Panalytical XPert with CuKα ($\lambda = 0.154$ nm) radiation at a grazing angle of 0.5°. The deposited and annealed SBT and La_2O_3 thin films' surface morphology was inspected using standard tapping mode atomic force microscopy (Dimension Icon from Bruker).

Initially, the crystallinity of SBT thin films needs to be confirmed to support the ferroelectric phase of SBT thin films. The GIXRD patterns of post-deposition annealed SBT thin films on Si revealed polycrystalline SBT thin films with the presence of dominant (111) and (115) phases along with minor (02$\underline{1}$0) and (23$\underline{1}$1), as shown in Fig. 1, where peaks are identified from *ICDD 01–081-0557*.[24] Nonetheless, dominant SBT (111) and (115) phases are generally observed for admirable ferroelectric characteristics, such as fatigue endurance and higher remanent polarization. Hence, the XRD analysis approves the ferroelectric phases of SBT thin films.

The surface morphology of the post-deposition annealed La_2O_3 and SBT thin films on Si is inspected by the standard tapping mode atomic force microscopy (AFM). Figures 2(a) and 2(c) show the 2D surface topology, and Figs. 2(b) and 2(d) show the 3D surface topology of La_2O_3 and SBT thin films, respectively. The surface rms roughness is measured from 1 × 1 μm^2 scan area, and AFM surface micrographs of La_2O_3 and SBT thin films are ~0.22 ± 0.04 nm and ~1.05 ± 0.03 nm, respectively. Thus, it confirms the highly smooth thin films, especially the La_2O_3 buffer layer, as required for MFIS device structures for ferroelectric memory device applications.

Figure 3 shows the memory characteristics of Pt/SBT/La_2O_3/Si, MFIS devices. As set out and presented in Fig. 3(a), Pt/SBT/La_2O_3/Si measured cyclic C–V characteristics of MFIS devices with variation in sweep voltage from accumulation to inversion to accumulation regions at a fixed frequency of 1 MHz. The capacitance of accumulation (C_{acc}) and inversion (C_{inv}) regions is ~122 pF and ~20 pF, respectively. Here, the memory window or hysteresis is defined by the shift in the flatband voltage measured during forwarding voltage sweep from

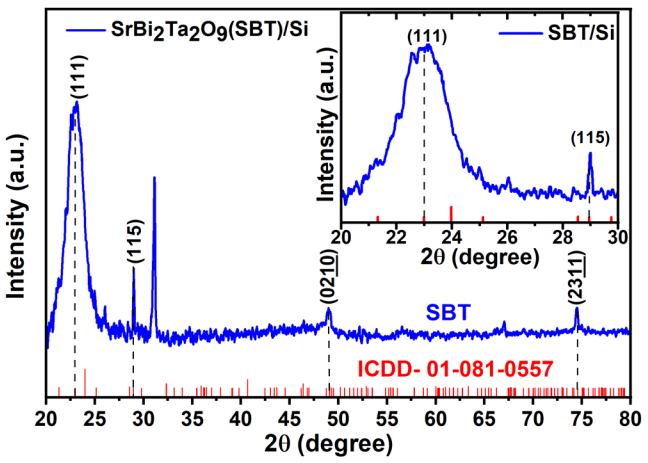

FIG. 1. GIXRD patterns of SBT thin films on silicon. The inset shows the magnified view of dominant (111) and (115) ferroelectric phases.

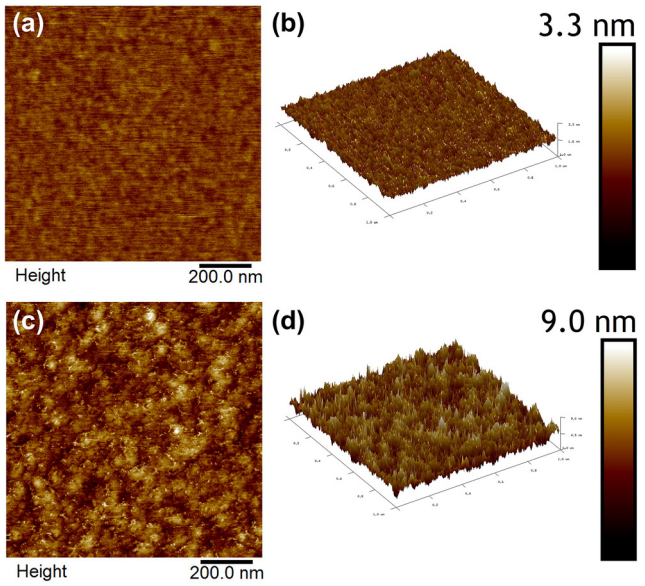

FIG. 2. The surface topography of SBT and La_2O_3 thin films: (a) 2D and (b) 3D AFM surface micrographs of La_2O_3; (c) 2D and (d) 3D AFM surface micrographs of SBT thin films.

accumulation to inversion and reverse voltage sweep from inversion to accumulation regions. The clockwise memory window of ∼1.1 V is observed at a sweep voltage of ±5 V, which predicts the memory window due to SBT ferroelectricity (not due to charge trapping) and is in agreement with theoretical memory window (ΔW), as related using the following relation:[21,25]

$$\Delta W \approx 2 d_f E_c, \tag{1}$$

where d_f is the thickness of SBT thin films and E_c is the coercive field of ferroelectric SBT thin films (∼50 kV/cm).[11,12] Here, the memory window increases up to ∼1.1 V at sweep voltage of ±5 V to ∼1.5 V at a sweep voltage of ±6 V due to an increase in polarization of ferroelectric SBT thin films with the electric field. However, on a further rise of sweep voltage to ±7 V, the memory window saturates to ∼1.5 V and intends to decrease or turn anticlockwise [Fig. 3(a)]. A similar trend was also observed for other analogous reported MFIS structures.[19] The memory window was found to increase up to a specific optimum voltage beyond which it starts to decrease. This behavior is generally expected to be due to charge injection ($\Delta V_{FB,ci}$) in the gate stack due to a higher electric field across the buffer layer at higher sweep voltages that oppose the ferroelectric polarization. The memory window, including the effect of charge injection, is related as follows:[21]

$$\Delta W \approx 2 d_f E_c - \Delta V_{FB,ci}. \tag{2}$$

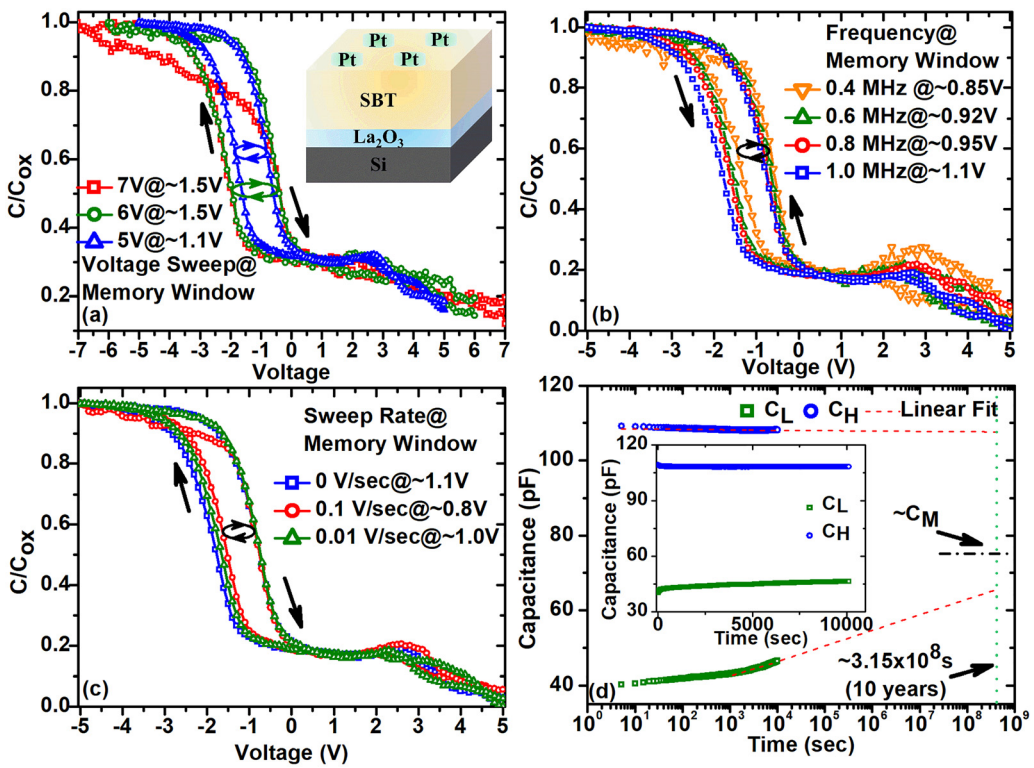

FIG. 3. Memory characteristics of Pt/SBT(∼115 nm)/La_2O_3(∼10 nm)/Si, MFIS devices: C–V characteristics with variation in (a) sweep voltage, (b) frequency, and (c) sweep rate. The inset of (a) shows the MFIS device structure. (d) The data retention C–T characteristics linearly extrapolated up to 10 years. The inset (d) shows the measured C–T characteristics on a linear scale.

Here, the voltage drop across the insulating buffer layer (V_i) and ferroelectric layer (V_f) is related as

$$\frac{V_f}{V_i} = \frac{d_f}{d_i} * \frac{\varepsilon_i}{\varepsilon_f}, \quad (3)$$

where d_i, ε_i, d_f, and ε_f are the thickness and dielectric constants of the insulating and ferroelectric thin films, respectively.[16] Using (3), V_f/V_i is estimated to be $(115*30)/(10*200) \approx 1.7$, assuming the values of d_i, ε_i, d_f, and ε_f to be 10 nm, 30, 115 nm, and 200, respectively. Additionally, the total gate voltage is equal to the sum of V_f and V_i. Therefore, on the 5 V gate voltage application, ~3.17 V appears across the ferroelectric SBT thin films, corresponds to the electric field of ~0.27 MV/cm well above the coercive field of SBT, and so appropriate for SBT polarization.[12] In contrast, the remaining ~1.83 V drops across the La_2O_3 insulator, which relates to the electric field of ~1.83 MV/cm well below the breakdown field of La_2O_3 dielectric. Therefore, the Pt/SBT(115 nm)/La_2O_3(10 nm)/Si, MFIS structure showed a reliable memory window of ~1.1 V at an optimum sweep voltage of ±5 V (agreement with theoretical calculations) and considered for further measurements.

Hereafter, authorization is needed that the observed clockwise memory window up to ±6 V sweep voltage is due to ferroelectric polarization and not due to random variations or charge trapping. Thus, C–V characteristics are measured with variation in frequency at a fixed sweep rate of 0 V/s [Fig. 3(b)] and alteration in sweep rate at a fixed frequency of 1 MHz [Fig. 3(c)]. It is evident from Figs. 3(b) and 3(c) that the variation in memory window is trivial (~0.95 ± 0.15 V) with a variation in frequency and sweep rate, which confirms that the observed memory window is due to ferroelectric polarization and not due to random variations or charge trapping.[15,18] Here, the insignificant variation in memory window of ~±0.15 V with the variation in frequency and sweep rate may be due to statistical variations expected in the ferroelectric material system.

Furthermore, for data storage NVM, device reliability, especially long-term data retention, is critical. Thus, the data retention characteristics of fabricated Pt/SBT(~115 nm)/La_2O_3(~10 nm)/Si, MFIS structures are investigated by the capacitance–time (C–T) method as shown in Fig. 3(d). For data retention measurements, a "write" voltage pulse of +5 V in height for the "ON" state and −5 V in height for the "OFF" state is applied for ~100 ms, followed by a read voltage of −1 V, close to the flatband voltage. The write voltage of −5 V for the high capacitive state (C_H) and +5 V for the low capacitance state (C_L) is observed. The inset of Fig. 3(d) shows the experimental data in a linear scale measured up to 10^4 s at room temperature, revealing exponential decay of capacitance states. Moreover, the high and low capacitance states remain distinguishable even if extrapolated to $\sim 3.15 \times 10^8$ s (~10 years), which reveals excellent data retention of Pt/SBT(115 nm)/La_2O_3(10 nm)/Si, MFIS structures suitable for NVM applications. As a part of future work, additional studies are needed to determine a more clarifying data retention time as a function of temperature.[26]

The extended data retention is expected for the La_2O_3 buffer layer, possibly because of its predicted lower leakage current density among high-κ dielectrics.[8] Therefore, the gate leakage characteristics are further investigated for the fabricated Pt/SBT(115 nm)/La_2O_3(10 nm)/Si, MFIS devices, as shown in Fig. 4(a). The low gate

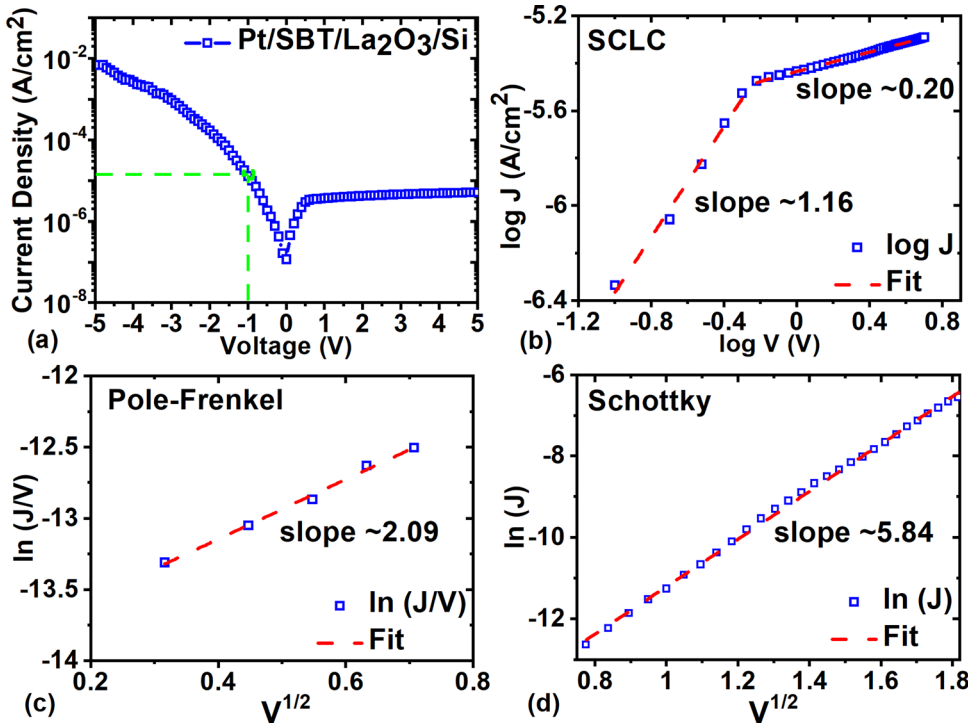

FIG. 4. Leakage characteristics and the conduction mechanism of Pt/SBT(115 nm)/La_2O_3(10 nm)/Si, MFIS devices: (a) the current density (J) vs voltage (V) characteristics; (b) the log(J) vs log(V) characteristics for the positive voltage range from 0 to 5 V; (c) the ln(J/V) vs $V^{1/2}$ relation for the absolute negative voltage range from 0 to 0.5 V; and (d) the ln(J) vs $V^{1/2}$ relation for the absolute negative voltage higher than 0.6 V.

leakage current density observed to be ∼12.8 μA/cm^2 at −1 V in accumulation signifies the suitable interfaces of the SBT/La_2O_3/Si system and confirms exceptional quality SBT and La_2O_3 thin films.

Additionally, the leakage current density is essential, especially for 1T type FeFET nonvolatile memory devices. In general, a lower leakage current is believed to support better data retention characteristics.[14–19] Therefore, the leakage characteristics and the corresponding conduction mechanism are analyzed as presented in Fig. 4. Pt/SBT (∼115 nm)/La_2O_3(∼10 nm)/Si, MFIS devices showed lower leakage current density of ∼12.8 μA/cm^2 at −1 V gate voltage as revealed from Fig. 4(a). Thus, it corroborates the high quality of SBT, La_2O_3 thin films, and SBT/La_2O_3/Si gate stack as desired for NVM applications.

Furthermore, the current conduction mechanism is analyzed to elucidate the reason behind low leakage current density and long data retention. For the bulk current conduction mechanism, the relation of log (J) vs log (V) is extracted from Fig. 4(a) for a positive voltage range from 0 to 5 V, as shown in Fig. 4(b). For lower applied voltage range less than 0.6 V (i.e., log V < −0.2), J is directly proportional to V, confirming Ohm's law [related by Eq. (4)], i.e., the log (J) increases directly in proportion to log (V) with a slope of ∼1.16. For a higher applied voltage range greater than 0.6 V (i.e., log V > −0.2), the slope decreases to ∼0.2, portraying current saturation and the minimum number of bulk oxide traps in this region,[27,28]

$$J_{ohm} \approx qn_0\mu\frac{V}{d}, \tag{4}$$

where q, n_0, μ, V, and d are the electron charge, concentration of free charge carriers in thermal equilibrium, mobility, applied voltage, and thickness of gate dielectrics. Thus, the squared voltage dependence is not observed, revealing a lower leakage current for better data retention characteristics. Next, for the electrode limited conduction mechanism, the relation of ln (J/V) vs $V^{1/2}$ and ln (J) vs $V^{1/2}$ is extracted for the absolute value of negative gate voltage range from 0 to −5 V, as shown in Figs. 4(c) and 4(d), respectively. For lower absolute applied voltage range from 0 to 0.5 V, the Poole–Frenkel (PF) emission is recognized, as shown in Fig. 4(c), commencing from electric field induced thermal ionization of trapped charges into the conduction band of SBT and La_2O_3 thin films.[17] The PF emission can be related using Eq. (5) as follows:

$$J_{PF} = CV\exp\left[-\left(\emptyset_t - e\sqrt{eV/d\pi\varepsilon_o\varepsilon_i}\right)/k_BT\right], \tag{5}$$

where C, $\emptyset_t$, ε_i, k_B, e, and T is a constant, the trap ionization energy, the dielectric constant of the gate stack, Boltzmann's constant, electronic charge, and temperature, respectively.[29] While the term $e\sqrt{eV/d\pi\varepsilon_o\varepsilon_i}/k_BT$ represents the slope of the ln (J/V) vs $V^{1/2}$, which is ∼2.09 for the Pt/SBT(115 nm)/La_2O_3(10 nm)/Si, MFIS devices, as shown in Fig. 4(c). Afterward, for a higher absolute applied voltage range greater than 0.5 V, the Schottky emission is recognized from the linear relation of ln (J) vs $V^{1/2}$, as shown in Fig. 4(d), and related as follows:

$$J_{SE} = AT^2\exp\left[\left(\emptyset_B - \sqrt{q^3V/4\pi\varepsilon_o\varepsilon_i}\right)/k_BT\right], \tag{6}$$

where A and $\emptyset_B$ are a constant and the potential barrier height, respectively.[30]

Furthermore, Pt/SBT/Pt, MFM structures were fabricated on Ti/SiO_2/Si substrates to confirm the ferroelectricity of SBT thin films. The electrical characteristics of control Pt/SBT/Pt, MFM structures are shown in Figs. 5(a) and 5(b). For the pulsed charge–voltage measurements, a triangular wave of magnitude 10 V and frequency ∼250 kHz is applied to Pt/SBT/Pt, MFM structures, and the corresponding transient current–time (I–T) characteristics measured are shown in Fig. 5(b). As evident from Fig. 5(a), during time t_1 (∼1 μs), the measured current increases from 0 to ∼10 μA with variation in charge (or voltage) from 0 to 8 pC (or 0 to 10 V), attributed to increasing ferroelectric polarization. Furthermore, during time t_2 and t_3, the measured charge decreases from ∼10 μA to ∼−10 μA, with variation in charge (or voltage) from 8 to ∼−8 pC (or 10 V to −10 V) attributes to switching of ferroelectric polarization. The measured current does not entirely follow the charge curve during time t_2 and t_3 attributes to decent quality Pt/SBT/Pt, MFM structures with minimum leakage. Again, during time t_4, the current increases with a variation in charge from ∼−8 pC to ∼0, which signifies switching of ferroelectric polarization back toward the initial state of t_1. From the measured current–voltage characteristics, the corresponding polarization–electric field (P–E) characteristics of Pt/SBT/Pt, MFM structures are presented in Fig. 5(b). However, we did not observe a saturated P–E hysteresis loop due to instrumental limitations of the voltage up to 10 V supply. Yet, the P–E hysteresis loops are significant enough with maximum polarization up to 0.04 μC/cm^2, to confirm the ferroelectric polarization of SBT in support of C–V measurements of Fig. 3.

Moreover, control samples of Pt/La_2O_3(∼10 nm)/p-Si, MOS structures were analyzed to confirm the quality of La_2O_3 thin films on silicon. The C–V characteristics of control Pt/La_2O_3(∼10 nm)/p-Si, MOS structures, with similar cyclic gate voltage sweep from ± 5 V, are acquired to compare with MFIS devices of Fig. 3. The trivial anticlockwise memory window of <0.3 V at ±5 V sweep voltage is observed, revealing a lower number of defects in La_2O_3 thin films due to charge trapping. This signifies that the anticlockwise memory window of <0.3 V in Pt/La_2O_3(∼10 nm)/p-Si MOS device, indeed, opposes the clockwise memory window of ∼1.1 V in Pt/SBT(∼115 nm)/La_2O_3(∼10 nm)/Si, MFIS devices. However, the ferroelectricity of SBT thin films is enough to overpower this trivial charge trapping and depict an overall clockwise memory window in Pt/SBT(∼115 nm)/La_2O_3(∼10 nm)/Si, MFIS devices. Furthermore, insets (i) and (j) of Fig. 5(c) show the device structure of Pt/La_2O_3(∼10 nm)/p-Si, MOS devices, and the corresponding J–V characteristics, respectively. Again, the lower gate leakage current density of ∼0.84 μA/cm^2 at −1 V in the accumulation region confirms good quality La_2O_3 thin films and La_2O_3/Si interface. Comparatively, the current density in Pt/SBT(∼115 nm)/La_2O_3(∼10 nm)/Si, MFIS devices is ∼12.8 μA/cm^2 at −1 V, which is marginally more, that reveals the presence of a reasonable number of defects in Pt/SBT/La_2O_3/Si MFIS as compared to the La_2O_3 MOS structure. Nevertheless, the overall quality of the La_2O_3 buffer layer is appreciably good that results in exceptional characteristics of Pt/SBT(∼115 nm)/La_2O_3(∼10 nm)/Si, MFIS devices suitable for 1T type FeFET NVM applications.

Finally, the benchmark of memory window with voltage sweep and data retention time of proposed Pt/SBT/La_2O_3/Si, MFIS device structures with related experimental reports is presented in Fig. 5(d). The proposed Pt/SBT/La_2O_3/Si, MFIS device structure provides optimum and reliable performance for nonvolatile memory applications.

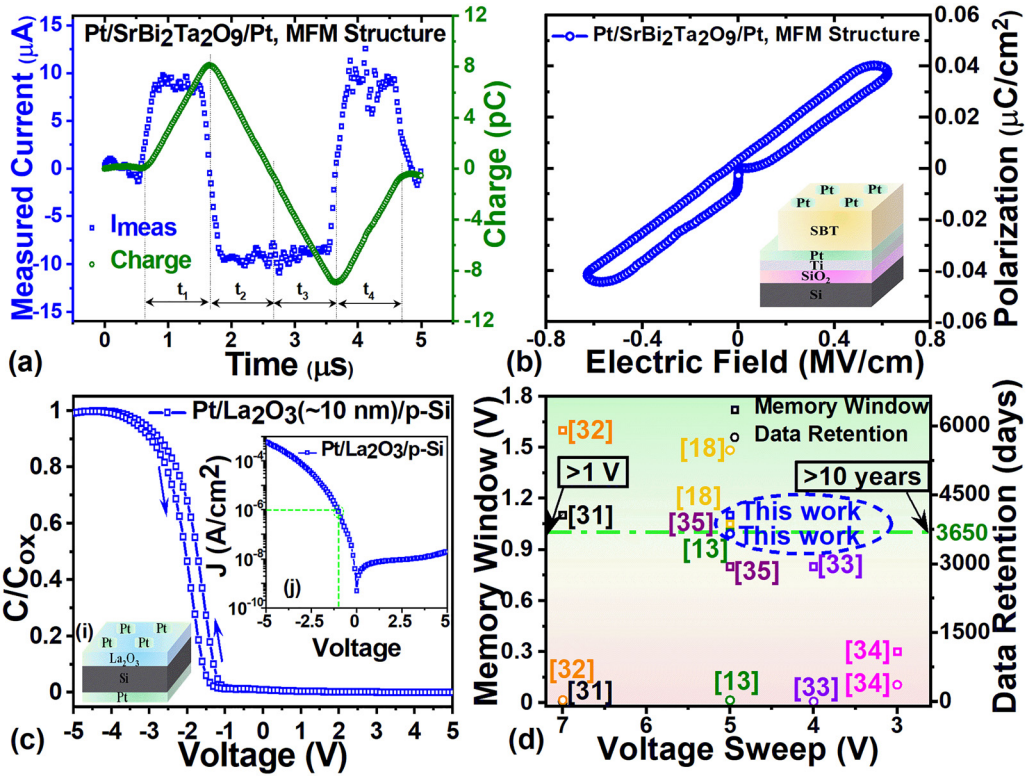

FIG. 5. The electrical characteristics of Pt/SBT/Pt, Metal/Ferroelectric/Metal (MFM) structures: (a) the pulse current–time (*I*–*T*) measurements and (b) the polarization–electric field characteristics extracted from the charge–voltage measurements. (c) Electrical characteristics of Pt/La_2O_3(∼10 nm)/p-Si, MOS structures: capacitance–voltage (C–V) characteristics with a cyclic gate voltage sweep of ± 5 V and insets (i) and (j) show the Pt/La_2O_3(∼10 nm)/p-Si, MOS device structure, and the corresponding J–V characteristics, respectively. (d) Benchmark of memory window with voltage sweep and data retention time of proposed Pt/SBT/La_2O_3/Si, MFIS device structures with related experimental reports.[6,18,19,31–35]

For instance, the 1T type device architecture enabled nondestructive readout, compatibility with the front-end-off-line (FEOL) thermal budget up to 800 °C, the high memory window of ∼1.1 V, low leakage current density, and data retention measured until 10^4 s (>10 years on extrapolation). Additionally, SBT ferroelectric is expected to show high endurance up to 10^{12} cycles. Still, CMOS compatibility is limited due to SBT, and further scalability is expected with downscaling of the gate stack thickness, where reliability and statistical variations are to be encountered as a part of future work.

In summary, Pt/SBT(115 nm)/La_2O_3(10 nm)/Si, MFIS device structures were investigated. The electrical characteristics revealed a high clockwise memory window of ∼1.1 V at ±5 V sweep voltage due to ferroelectric polarization, long data retention measured until ∼10^4 s even on extrapolation to 10 years, and low leakage current density ∼12.8 μA/cm^2 at −1 V at room temperature. The trivial variation in the clockwise memory window of ∼0.95 ± 0.15 V with variation in the sweep rate and frequency confirmed the memory behavior due to spontaneous ferroelectric polarization of SBT thin films. Furthermore, the current conduction mechanism analysis revealed ohms law for lower positive voltage range from 0 to 0.6 V. For higher positive voltage range >0.6 V, the current saturation is observed. Alternatively, for the negative applied voltage range, the Poole–Frenkel conduction from 0 V to −0.5 V and Schottky emission for applied voltage <−0.5 V are observed. Exceptional electrical characteristics of the proposed MFIS structures are attributed to the good-quality La_2O_3 buffer layer and La_2O_3/Si system. Control Pt/La_2O_3/Si, metal–insulator–semiconductor structures showed a trivial anticlockwise memory window of <0.3 V at ±5 V sweep voltage and low gate leakage current density of ∼0.84 μA/cm^2 at −1 V in accumulation. GIXRD-based crystallinity analysis revealed the polycrystalline nature of SBT thin films. Also the presence of dominant (111) and (115) phases results in admirable ferroelectric characteristics. Hence, the proposed Pt/$SrBi_2Ta_2O_9$/La_2O_3/Si, MFIS device structure is a potential candidate as a gate stack of one-transistor (1T) type Ferroelectric Field-Effect transistor devices for nonvolatile memory applications.

The authors acknowledge the Center for Design and Frabrication of Electronic Devices (C4DFED) and School of Computing and Electrical Engineering, Indian Institute of Technology (IIT)-Mandi, for sample preparation and the characterization facility. The authors would like to thank the Center for Nano Science, Indian Institute of Technology (IIT)-Kanpur, India, for providing access to the GIXRD facility.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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