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Review

Integration of Ferroelectric Materials: An Ultimate Solution for Next-Generation Computing and Storage Devices

Robin Khosla and Satinder K. Sharma*

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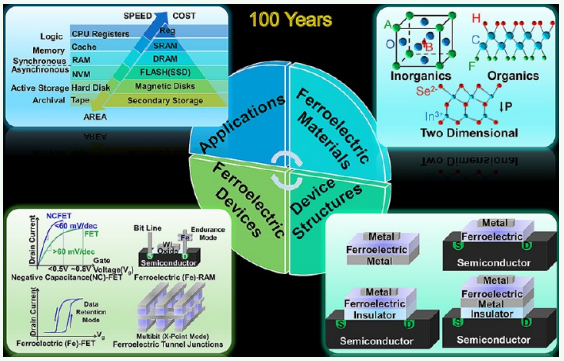
ABSTRACT: Over the decades since ferroelectricity was revealed, ferroelectric materials have emerged as a cornerstone for a wide spectrum of semiconductor technology and electronic device applications, particularly in state-of-the-art complementary metal oxide semiconductor (CMOS) logic circuits and digital information storage media. Recent unprecedented advancements and future perspectives on integrating ferroelectric materials, particularly with high-κ dielectrics for electronic devices, are weighed. The emphasis is on (i) application (logic and memory); (ii) ferroelectric materials (organic, inorganic, and two-dimensional (2D)); (iii) device structures (metal/ferroelectric/metal (MFM), metal/ferroelectric/semiconductor (MFS), metal/ferroelectric/insulator/semiconductor (MFIS), and metal/ferroelectric/metal/insulator/semiconductor (MFMIS)); and (iv) next-generation electronic devices (negative capacitance field effect transistors (NC-FETs), ferroelectric RAM (FeRAM), ferroelectric field effect transistors (FeFETs), and ferroelectric tunnel junctions (FTJs)). In NCFETs, the ferroelectric layer serves as a negative capacitor so that the channel surface potential can be amplified more than the gate voltage. Hence, devices can overcome the "Boltzmann tyranny" and operate with a steep subthreshold swing < 60 mV/dec and supply voltage < 0.5 V. Thus, NC-FETs would be more suitable for high-speed logic operations, scalability, low-power, and cost-effectiveness, targeting applications such as 14T-type CPU registers and 6T-type cache static random access memory (SRAM). Ferroelectrics also opens a path to solving the problems associated with technology scaling due to the unique structural and electronic properties. Ferroelectric memories are anticipated to be in different flavors based on optimum performance, cost, and end-user requirements. Herein, we deliberate on the exciting possibilities for the development of device structures such as one-transistor one-capacitor (1T-1C)-type FeRAM with fast access time (<10 ns), high endurance (~>10^{14} cycles), and moderate data retention being considered as a strong contender for volatile dynamic random access memory (DRAM), while, for nonvolatile memory applications, 1T-type ferroelectric gated transistors, called FeFETs with nondestructive readout, fast access time (~<100 ns), moderate endurance (>10^9 cycles), and high retention time (>10 years) have the potential to compete with embedded solid-state drives (SSDs). Finally, the FTJs with three-dimensional cross-point architecture are strong contenders for high-density niche storage applications to interchange with low-cost per bit external hard disk drives. We conclude with a brief survey of recent ferroelectrics advances and potential futuristic comparisons for next-generation computing and storage device applications so the field may expand and pave the way for high-volume manufacturing of semiconductor technology down to the sub-5 nm node over the coming years.



KEYWORDS: *Ferroelectric Materials, Devices, Field Effect Transistors, CMOS Logic, Negative Capacitance, Memory, Non-Volatile Memory, Ferroelectric Tunnel Junctions*

1. INTRODUCTION

The advent of the Internet of Things (IoT), portable electronic devices (such as mobile phones, tablets, notebooks), cloud storage, and data centers (such as Google, Microsoft, Facebook, and so on) have set up colossal market demand for computing systems. Hence, with thriving human−computer interaction (HCI), the generation of diverse data is flourishing exponentially. As per International Data Corporation, one of the vital projections assesses that by 2025, humanity's accumulated digital data would rise to over 163 zettabytes (163 trillion gigabytes). However, significant components of any computing system are the processors and memories used to perform arithmetic operations and store data/instructions. Efficient

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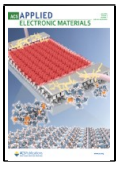

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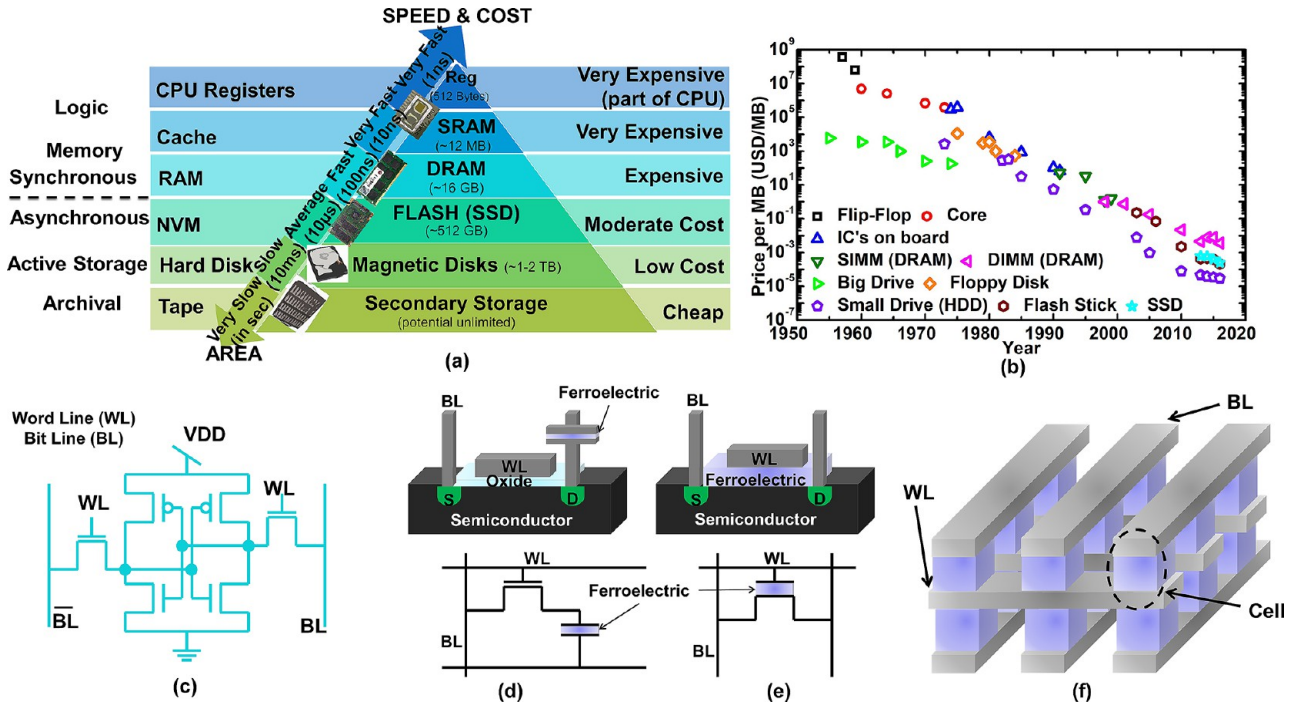

Figure 1. (a) Modern computer memory hierarchy, (b) historical evolution of memory technology,[2] (c) 6T structure of SRAM, (d) 1T-1C structure of FeRAM (alternate to DRAM), (e) 1T structure of FeFET (alternate to NVRAM), (f) cross-point architecture for high-density 3D memories (alternate to external HDDs).

computing relies on the processor's execution speed and the memory's access time. However, accessing the memory is much slower than the processing of instructions in the processor. Hence, modern computing systems have a huge performance gap between the processor and memory, often called the "memory wall." The overall performance depends on the critical (slowest) path. Thus, modern computing systems utilize a hierarchy pyramid of volatile and nonvolatile information storage devices (Figure 1a) to obtain an optimum trade-off between performance and cost.[1] Since the 1960s, the cost of one-bit of semiconductor memory has fallen 100 million times due to scaling, and this trend continues to date, summarized in Figure 1b.[2]

As revealed from Figure 1a, the area (to store per bit), speed (access time), and cost per bit increases as we approach the bottom to the pyramid's top. In contrast, the data storage capacity increases from top to bottom, depicted by the pyramid's width. The memory (cache/static random-access memory (SRAM)) next to the processor (central processing unit (CPU) Registers) is to be accessed frequently. So SRAM requires the fastest possible operating speed and integration with the processor providing low storage capacity and high cost. CPU registers generally require 14 transistors (14T) with an access time of ≤1 ns, while SRAM needs 6T (Figure 1c) with an access time of ≤10 ns to store one bit of information. Here the term "random access" is used to specify that the CPU has the provision to randomly access any memory cell from the array of rows and columns. Further, the double data rate (DDR) dynamic RAM (DRAM) utilizes a one-transistor one-capacitor (1T-1C) structure to store one bit with an access time ≤100 ns. For over 30 years, DRAM and SRAM both have dominated the memory hierarchy closest to the processor but are volatile, i.e., lose the stored information when power is turned off.[3] Here it must be noted that the aforesaid synchronous memories need to be accessed frequently by the processor. Therefore, these require high endurance (i.e., data switching cycles >10^{15} cycles). In contrast, data retention of the memory state for an extended duration is not a big concern at this hierarchy level, even if it is of a few milliseconds. The asynchronous nonvolatile memories (NVM) come into the picture that retains their stored data information state even when power is turned off, as indicated on moving further down the memory pyramid. Therefore, data retention is a paramount concern here (usually >10 years is desired at an elevated temperature of 85 °C), while a moderate endurance (>10^{8} cycles) can also resolve the purpose. However, for NVM, the requirements vary as per the application and end-user requirements ranging from small density storage applications (RFIDs) to high-density storages (hard disk drives (HDDs)).[4,5] In the past half-century, magnetic HDDs have primarily been used for nonvolatile information storage applications.[3] Additionally, Flash memory-based, solid-state drives (SSDs) with 1T-structure, multibits (2−3 bits) storage, and fast access time of ≤500 ns were introduced to bridge the enormous performance gap between HDDs with an access time of ≤10 ms and DRAM of ≤100 ns. In the 2000s, IBM instigated the term "storage class memories (SCM)",[6] whose access time lies in between DRAM and HDD and can replace rotating mechanical storage disk drives with nonvolatile solid-state drives (SSDs). As the SSDs cost decreases with technology advancement, they have already started replacing the magnetic HDDs. Apart from the physical storage mechanism, the architecture of such memory technology is also essential; e.g., NOR flash provides random read access using the higher area (two-bit per transistor). Contrary, NAND flash (three-bit per transistor) is optimized for the lowest cost at the price of eliminating the possibility of fast random access. In fact, this is majorly performed by the architecture and not so much by the physical storage mechanism. Finally, to the pyramid's bottom is the long term and cheapest secondary storage like magnetic tapes or disks. Also, it must be noted that the smaller the area or cell size

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of the device, the lower is its cost, which is a significant factor dominating the memory market.

Here, betoken, what if in the future we may achieve a 1T-type memory device (small cell size) with fast (<10 ns) random access like RAM and nonvolatile storage to store one-bit (or multibit) information with high endurance of $>10^{15}$ cycles and data retention of >10 years? The answer is such a memory device can replace the complete memory hierarchy ranging from SRAM to HDDs and is likely to be called a "universal memory." A Universal memory can significantly simplify the design using a single memory instead of multiple memories such as DRAM, SRAM, and HDDs being used today. In fact, in the 1990s, the term universal memory was first familiarized as a memory class with fast random access like RAM, and nonvolatile storage like read-only memory (ROM) emanates at a moderate cost. Alternatively, the terminology "non-volatile random-access memory (NVRAM)" is even better preferred for memory with random access like RAM and nonvolatile storage like ROM or flash.[7,8] However, it is hard to realize such a memory device primarily because of the "voltage-time dilemma".[9,10] For instance, data retention of 10 years at 85 °C is considered a standard benchmark for nonvolatile storage. In a flash memory cell, this can be attained with a reasonable energy barrier (e.g., a tunnel oxide rectangular barrier of ∼5 nm width and ∼1.5 eV height between memory states). Consequently, a sufficiently high voltage (say >10 V) or other stimulus is required to bend the energy barrier fast enough such that electrons can tunnel from the semiconductor to the floating gate and attain the write time of ∼10−100 ns. Here, the voltage can be further related to the energy (CV^2), and a higher voltage corresponds to a higher electric field across the gate stack's thin films, resulting in the higher electric stress or breakdown and limiting the endurance switching cycles.[11] Thus, there is a trade-off between write time, data retention, endurance, and energy. Likewise, considering a ferroelectric memory cell, for instance, in a general metal-ferroelectric-insulator-semiconductor (MFIS) structure, this may be understood from the speed, retention, and endurance trade-off. If the buffer insulator (E_g > 6 eV) thickness is thin (>5 nm), then gate leakage is less, and retention is better but compromising for lower switching speed and higher power consumption. Otherwise, if the insulator thickness is ultrathin (<5 nm), then the switching speed can be increased but at the cost of higher gate leakage and reduced data retention. Therefore, an optimum sweet spot between such parameters is required to be considered.

Otherwise, the term non-volatile memory (NVM) or storage class memory (SCM) can be used for memory with long data retention and access time amid DRAM and HDD, which is brought forth at a moderate cost (similar to HDDs cost/bit). NVMs are cataloged as charge storage memories, i.e., NAND Flash and NOR Flash[12] and noncharge storage-based emerging memories: ferroelectric RAM (FeRAM),[13] magnetic RAM (MRAM),[14] phase change RAM (PCRAM),[15] and resistive RAM (ReRAM).[16] The miniaturization of charge-based memory devices to the next-generation is vulnerable to insufficient electron quantity. Therefore, noncharge storage-based emerging memory technologies are considered as a prospective contender for next-technology node.[17] Among this segment, ferroelectric materials-based memories are attractive, with theoretical ferroelectric polarization and a remarkable switching speed of <220 ps.[18]

In recent times, the advent of IoT and portable electronics has brought an enormous setup demand for NVM devices. The nonvolatile solid-state flash memory plays a leading role in the portable and flexible electronics market and drives modern information and communication technology's memory hierarchy. Moreover, to fulfill the ever-increasing market demand for memory with high performance, large data storage density, and low-cost per bit requirements, the integration of novel materials in the forefront CMOS process flow is considered for emerging memory technologies. In addition, the capability to store two or more stable states in terms of an electrical property (e.g., resistance/capacitance) that can be switched with appropriate voltage/current pulses can compete with current Flash technology.

The integration of novel materials in a high-volume manufacturing CMOS process flow must meet the following scientific research and development parameters: (i) optimization of switching properties of the material: switching speed, signal window, the stability of memory states (data retention), repeatability of switching cycles (endurance), and minimization of wear out effects: imprint and statistical switching; (ii) process control of the effects of new material on the CMOS process: additional thermal budget, contaminations; (iii) control of material degradation by CMOS process flow: reducing atmosphere and thermal budget; and (iv) to realize high-density memory products, the new material formulations must be compatible with next-generation three-dimensional (3D) architectures.[8]

As the scientific community is celebrating 100 years of the invention of ferroelectricity, this is a perfect time to summarize the progress of ferroelectric devices in the past century. Several review articles have been published on ferroelectric devices, especially on ferroelectric materials,[19−25] ferroelectric memories,[4,11,33,34,17,26−32] FTJs,[35,36] NC-FETs,[37−39] 2D-FeFETs,[40] which target a particular application in detail. The intended article primarily differs from the focus and flow, providing a big picture, keeping the explanations straightforward from a newbie perspective to relate to the real-world application while also covering the recent advances in the field. Here, we included the numerous advances and various important reports on integrating ferroelectric materials for different electronic device applications to give a broad picture, perspectives, projections, comparisons, and discussions, especially for those intending to work on ferroelectric materials, high-speed semiconductor computing/logic devices, and emerging nonvolatile ferroelectric memories. The organization of this article is in the following subsequent sections. Section 2 abridges the ferroelectric materials: organic, inorganic, and two-dimensional (2D). Section 3 continues a preface to ferroelectric material's essential characteristics, conventional ferroelectric, and negative capacitance behavior. Section 4 puts forward the emerging device structures: MFM, MFS, MFIS, and MFMIS. In section 5, we catalog the operating principle, recent progress, judgements, and possible use of emerging ferroelectric materials in devices at all levels of memory hierarchy: (i) ferroelectric negative capacitance field effect transistors (NC-FET): 1T structure for low power CMOS logic (basic 1T-component for 14T CPU registers and 6T SRAM); (ii) ferroelectric RAM (FeRAM): 1T-1C structure with fast access time (<10 ns), high endurance ($>10^{14}$ cycles), moderate data retention, and destructive readout for volatile dynamic random-access memory (DRAM); (iii) ferroelectric field effect transistors (FeFET): 1T structure with nondestructive readout, fast access time (∼<100 ns), moderate endurance ($>10^9$ cycles), and high retention time (>10 years) for nonvolatile memories to substitute for current embedded

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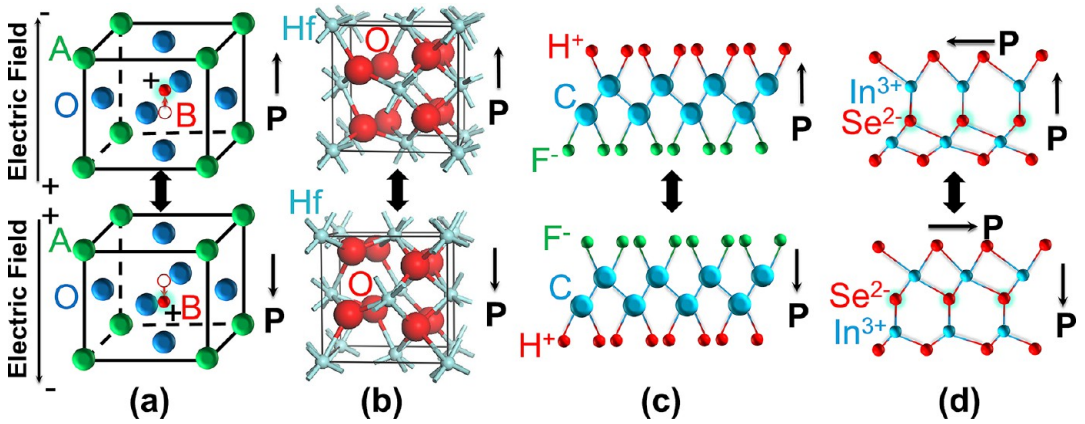

Figure 2. General crystal structure of ferroelectric materials depicting displacement of ions with a change of the electric field direction, where P denotes the spontaneous polarization reversal. (a) Conventional perovskite ABO_3 structure, showing the displacement of the center atom B (e.g., Ti^{4+} in $BaTiO_3$), (b) binary HfO_2 in the orthorhombic phase showing displacement of oxygen (red color) atoms (reproduced from ref 43. Copyright 2011 AIP), (c) organic PVDF in the β-phase where P denotes the dipole moment direction from F^- to H^+, and (d) two-dimensional In_2Se_3 shows the central Se atomic layer displacement in the FE-zinc blende (ZB') configuration.[47]

Table 1. Comparison of Ferroelectric Properties of Potential Inorganic, Organic Thin Films, and 2D Materials

material	K	P_r (μC/cm^2)	E_c (MV/cm)	T_{curie} (°C)	$T_{crystal}$ (°C)	fatigue (cycles)	ref
Inorganic Ferroelectrics							
$PbZr_xTi_{1-x}O_3$ (PZT)	~500	>15	0.05−0.07	350	<600	$<10^8$	4, 72, 293
PZT with IrO_2 electrode/SRO electrode	303/1870	23.1/28.2	0.024/0.017		700	$>10^{11}$	80
						$>10^{11}$	
SBT ($SrBi_2Ta_2O_9$)	200	5−10	0.03−0.05	320	700−800	$>10^{12}$	4, 294
BLT	~84−128	1−10	0.15−0.75		<650	$>10^{10}$	295
HfO_2(undoped)	34	10.6	~1.2		650	$>10^5$	45
(TiN/HfO_2(6 nm)/TiN)							
HfO_2 (doped with Si/Al/Y/Gd/Zr/La/Sr/N)	20−43	12−48	0.8−2.0		400−1000	$>10^6$	22, 51, 87−93, 225
$Hf_{0.5}Zr_{0.5}O_2$	40	15−17	1	up to 400 K	400−800	10^6−10^{12}	229, 232, 233
Organic Ferroelectrics							
PVDF (β-phase)	~8−10	7.5	0.6	<167	<160	$>10^6$	235
PVDF (δ-phase)	~8−10	7	1.15	<172	<160	$>10^6$	98, 106
P(VDF-TrFE)	~8	10	~0.5−5	80−140	<200	$>10^8$	85, 25, 105
PVDF−PMMA		5.4	1.1	>172	~140 ($T_{Process}$ ≈ 200)		296
PVDF-GO	8−16	~0.12	0.005	N.A.	<150		104
2D Ferroelectrics							
$CuInP_2S_6$				~42			118
SnTe				−3			115
In_2Se_3				427			123
α-In_2Se_3			0.2	~27			114
β-In_2Se_3				~200			121
BA_2PbCl_4				~180			119
d1T-$MoTe_2$				>27			116
WTe_2				~77			117

solid-state drives (SSD) inside computers; and (iv) ferroelectric tunnel junctions (FTJ) or ferroelectric resistive random access memory (FR-RAM), with a three-dimensional cross-point architecture for high-density niche storage applications to interchange low-cost per bit external hard disk drives. In the end, section 6, conclusions and future perspectives are highlighted.

2. FERROELECTRIC MATERIALS

Ferroelectric materials exploit the ferroelectric effect of dipole's tendency to instinctively polarize in a particular orientation under the directional electric field's influence and remain polarized even on the electric field's removal. In 1921, Valasek reported the first ferroelectric material in Rochelle salt bulk single crystal.[41] From the 1950s, the research and development followed ferroelectric thin films, though it lingered on a controversial question of whether there is a threshold of thickness limit below which ferroelectricity exists or not. It was believed that the spontaneous polarization vanishes below a critical thickness for traditional perovskite oxides due to a reduced transition temperature in thin films. The increased depolarizing electrostatic field, reduced long-range Coulomb coupling, surface-reconstruction due to surface energy, strain related to interfacial bonding, electron screening, and chemical environment are believed to be the possible reasons.[24] Nevertheless, presently with the advancement of more sophisticated thin-film fabrication techniques, ferroelectricity is demonstrated in remarkable

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heterostructures engineered down to single unit cell thin films.[42] Therefore, the future of ferroelectric materials is not limited by scaling defined by the so-called critical thickness due to the availability of ferroelectric materials and advanced fabrication techniques.

The origin of ferroelectricity (e.g., in perovskite ABO_3 structures) is based on the ion's displacement from symmetric crystalline structure resulting in polarization reversal. For instance, consider the $BaTiO_3$ crystal structure (Ba on corners, O on face centers, and Ti in center of unit cell) or $PbZrTiO_3$ crystal ($PbTiO_3$ or $ZrTiO_3$ unit cells). The center Ti atom (Ti^{4+} ion) displaces slightly out-of-symmetricity, is attributed to two different polarization states with the variation in the electric field direction, as shown in Figure 2a. Alternatively, the polarization reversal can be comprehended due to the displacement of charge (e.g., Ti^{4+} ion in this case). Here, the direction of spontaneous polarization 'P' is depicted from negative to positive or opposite to the direction of movement of the Ti^{4+} ion. Other than the conventional perovskite ferroelectrics, recently ferroelectricity has also been depicted in CMOS-compatible binary HfO_2-based ferroelectrics.[43] Generally, at atmospheric pressure, HfO_2 transforms from monoclinic to tetragonal to cubic phases at extremely high temperatures of 1700 and 2500 °C, respectively. However, under a specific temperature and pressure, it transforms into the orthorhombic phase, e.g., oI-phase space group *Pbca*; oII-phase space group *Pnma*, oIII-phase space group $Pca2_1$, oIV-phase space group $Pmn2_1$, and so on.[44] Ferroelectricity in HfO_2 is believed to be due to the stabilization of the orthorhombic phase; especially, the oIII-phase is the most popular and stable at various ranges of temperature and pressure. Figure 2b shows the displacement of oxygen (red color) atoms in the orthorhombic phase of binary HfO_2.[43] Ferroelectricity in HfO_2 is accomplished through compressive stress generated due to mechanical confinement of HfO_2 in TiN buffer layers to form $TiN/HfO_2/TiN$, the metal−insulator−metal system, or via doping to stabilize the ferroelectric orthorhombic phase in HfO_2.[22,43,45] Alternatively, for organic ferroelectrics such as PVDF, the switching of polarization is depicted in Figure 2c, where the electric dipoles formed by the C−F and C−H bonds can be inverted with the variation in the direction of the electric field. The electron clouds are closer to the fluorine due to its higher electronegativity, resulting in the displacement of a higher δ^- negative charge on the fluorine side and higher δ^+ positive charge on the hydrogen side, thus forming more polar bonds.[46]

Further, the polarization reversal in two-dimensional ferroelectrics, e.g., In_2Se_3, is believed to be due to the central Se atomic layer displacement in the ferroelectric zinc blende (ZB') configuration, indicating the correlation of in-plane and out-of-plane polarization, as shown in Figure 2d.[47] However, it is challenging to observe strong and stable spontaneous polarization (in-plane and out-of-plane polarization) in a few unit cell 2D ferroelectrics.[24] Here, "in-plane" expresses the polarization direction is contained in the surface, i.e., lateral direction (the polarization vector lying on the surface plane), while "out-of-plane" specifies that the polarization vector is perpendicular to the surface, i.e., the vertical direction (plane normal to the surface).

Numerous investigations have been carried out on ferroelectric materials organic, inorganic, and 2D systems as summarized in Table 1. Here, in section 2.1, we initially discuss ferroelectric materials' requirements for real-world device applications to bridge the gap between material scientists and device engineers. Further, in sections 2.2, 2.3, and 2.4, we debate the progress in inorganic, organic, and two-dimensional (2D) ferroelectric materials, respectively.

2.1. Requirements of Ferroelectric Material for Logic and Memory Devices. The choice of ferroelectric material may vary based on the device application. In general, a supreme ferroelectric material necessitates the following properties:[4,48]

- Reasonable dielectric constant (κ): Most ferroelectrics have a high dielectric constant compared to the insulator/oxide buffer layer. Therefore, a significant voltage drop across the buffer layer may cause the buffer layer breakdown. Additionally, a depolarization field (as discussed in detail in section 4.1) evolves at the ferroelectric between the transistor's gate and channel. Thus, the dielectric constant of ferroelectric to the dielectric constant of the buffer layer ratio must be low to minimize the voltage drop across the buffer layer. In other words, either the buffer layer with high permittivity or the ferroelectric film with a low permittivity is required for optimum device operation. Additionally, the ratio of insulator capacitance to ferroelectric capacitance must be high to reduce the depolarization field.[49]
- Sufficiently high remnant polarization (P_r): P_r must be sufficiently high to switch the transistor entirely and maintain the sensing margin. If the P_r becomes too high, the depolarization field becomes too high, and if P_r is too low, then the sensing circuitry cannot distinguish between different memory states.[22,49]
- Appropriate high coercive field (E_c): High coercive field is needed to reach a reasonable memory window even in thin films. For instance, it is demonstrated that if the E_c is about 50 kV/cm, then a memory window of ∼1 V is achieved with a film thickness of ∼100 nm.[50,51] But E_c should not be too high to be too close to the thin film's breakdown. Note that hysteresis or memory window is desired for memory application, but hysteresis-free characteristics are necessary for logic applications.
- Low leakage current: For low static power dissipations, the leakage current should be typically $<10^{-6}$ A/cm^2.
- High switching speed: For high-speed devices, typically <10 ns (theoretically ps) would be appropriate and seem achievable for all applications ranging from SRAM to NVM.
- Long data retention: To retain the stored information for longer durations, typically >10 years is needed for NVM application. However, short retention is acceptable for logic, SRAM, and DRAM applications where data need to be accessed frequently by the processor. Here, data retention implies the aging for which the device can hold the stored digital information.
- High endurance (i.e., good fatigue characteristics): The reliability after several switching cycles, typically 10^{12}−10^{15} cycles (higher the better), is needed. Higher endurance is vital for SRAM and DRAM, where data need to be accessed frequently. However, reasonable endurance of $>10^8$ cycles would be acceptable for NVM storage applications. Additionally, the ferroelectric material must be free from "imprint" that can shift the P−E hysteresis loop along the voltage axis.
- Crystallization temperature ($T_{crystal}$): It depends on the process technology integration concept, i.e., gate first or gate-last.[22] For 1T-1C structure FeRAM and MFM structure FTJs, <400 °C compatible with back-end-of-line (BEOL) CMOS processing is required. Alternatively, for the 1T structure FeFET and NC-FET, >800 °C compatible with front-end-of-line (FEOL) semiconductor processing is needed so that it can withstand the high thermal budget source/drain activation process. Also, the Curie temperature (T_C) of the ferroelectric must be high, at least higher than the operating temperature of ICs (∼>85 °C), to avoid conversion into the paraelectric phase.
- Compatibility with CMOS processing: The control of the effects of new material on the CMOS process, such as additional thermal budget, contaminations, and material degradation by the CMOS process, is needed.

2.2. Inorganic Ferroelectrics. Before 2000, numerous reports were focused on ferroelectricity in perovskites,[52] such as $LiNbO_3$,[53] $YMnO_3$,[54] $PbTiO_3$,[55] and $(Ba,Sr)TiO_3$.[56] From 2000 onward, research on ferroelectric materials was intensive, primarily on $SrBi_2Ta_2O_9$ (SBT),[57−65] $(Bi,La)_4Ti_3O_9$ (BLT),[66−68] $Pb(Zr,Ti)O_3$ (PZT),[69−78] and so on due to their excellent fatigue and leakage characteristics. From the above, PZT emerged as a promising candidate due to its high P_r and low crystallization temperature and was widely adopted in commercial 1T-1C FeRAM applications.[26,79] However, polycrystalline PZT or PZT with Pt electrodes suffers from fatigue ($<10^8$ cycles). PZT opponent SBT shows a high endurance of 10^{12} cycles but with low P_r and high crystallization temperature, as shown in Table 1. However, the PZT fatigue behavior improves to $>10^{11}$ cycles by using oxide electrodes (e.g., IrO_2 and SRO).[80] For PZT, the endurance degradation mechanism is proposed similar to bulk ceramics, thin films, and single

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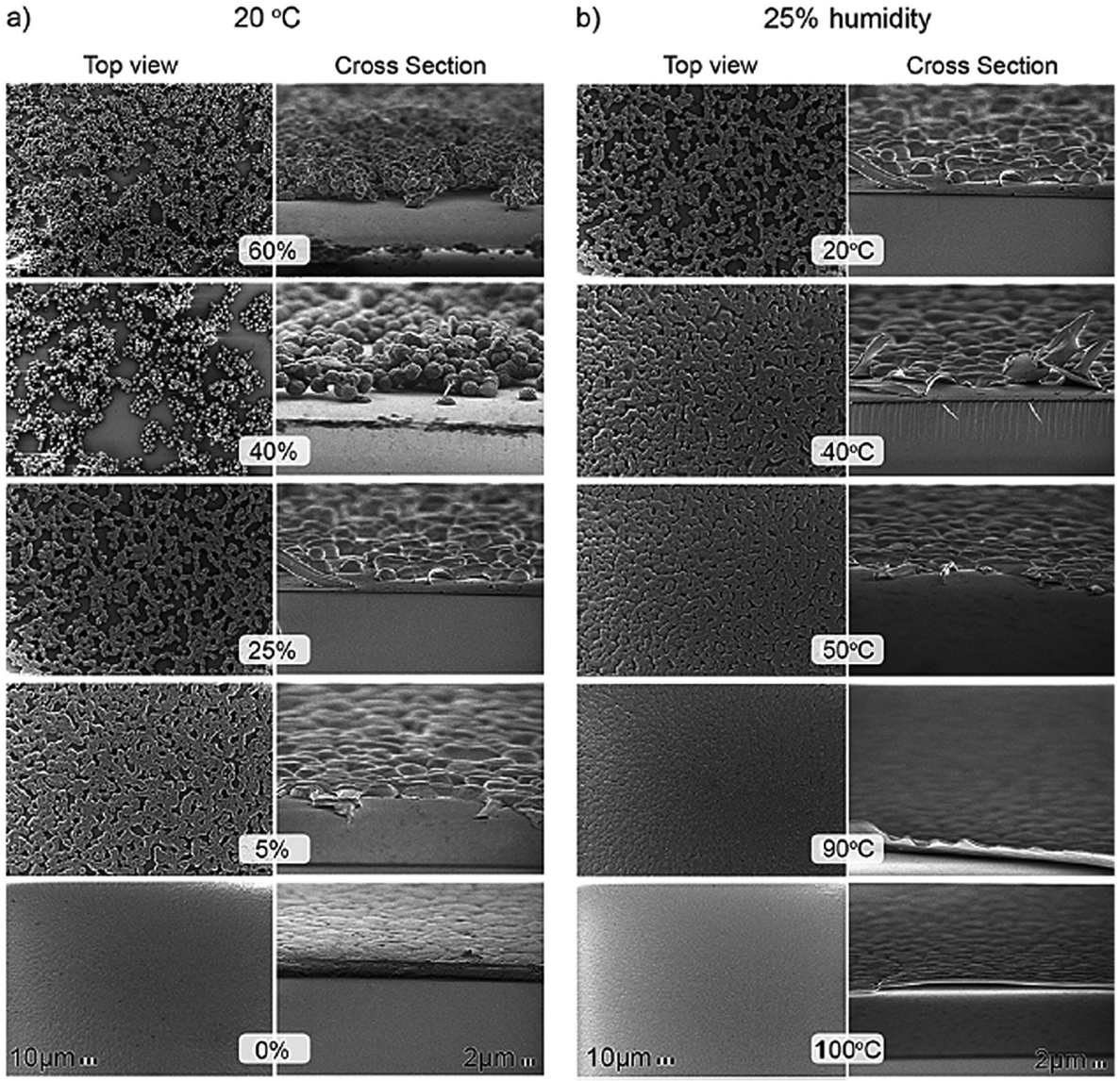

Figure 3. Top view and cross-section SEM images of PVDF thin films, (a) at fixed deposition temperature of 20 °C and with variation in relative humidity from 0 to 60% (PVDF thickness ∼900 to ∼2600 nm) and (b) at fixed relative humidity of 25% and with variation in deposition temperature from 20 to 100 °C (PVDF thickness ∼1500 to ∼1000 nm). Reproduced from ref 99. Copyright 2013 RSC.

crystals as comparable fatigue is reported.[81] Generally, models reported for endurance degradation state that the redistribution (or formation) of defects on electrical stress application influences spontaneous polarization.[82] For example, oxygen vacancies are available at defects that cause domain wall pinning, dead layer formation at the metal/ferroelectric interface, and fatigue due to local phase decomposition.[83,84] Raman measurements confirmed PZT's perovskite phase conversion to paraelectric/pyroelectric phases after bipolar pulse switching. The perovskite phase was found to be restored with oxygen environment thermal annealing of the fatigued capacitor. Hence, it may be concluded that fatigue is a general dilemma of inorganic ferroelectrics (such as PZT) that can be improved on thermal annealing. The formation of oxygen vacancies due to local uncompensated depolarization field is proposed to be the origin of endurance degradation.[85] However, a high production cost and non-CMOS-compatible technology hinder its widespread applications.[86] In recent times, the ability to engineer ferroelectricity in HfO_2-based ferroelectrics has provided new hope for ferroelectric devices. HfO_2 is already adopted as an alternate gate dielectric in Intel's CMOS technology beyond the 45 nm technology node. Hence, the integration of lead-free HfO_2-based ferroelectrics with current metal/high-κ transistors in CMOS technology is convenient. In this respect, various dopants such as Si, Al, Y, Gd, Sr, Zr, La, and N in HfO_2 are investigated.[22,51,87−93] Ferroelectricity in undoped HfO_2 is also reported, comprising the sandwich structure of HfO_2 in TiN buffer layers to form TiN/HfO_2/TiN, the metal−insulator−metal system.[45] The HfO_2-based device shows a high potential for further scaling due to ferroelectricity <6 nm thickness. The only limitation is reasonable endurance of $\sim 10^6$ program/erase cycles in ferroelectric HfO_2-based FeFETs.[94,95] Similar to the endurance improvement in PZT using oxide electrodes, several attempts were also carried out on HfO_2-based ferroelectrics to improve the endurance by using different electrode materials, and TiN electrodes showed superior performance.[96] In the MFM capacitor structure, an endurance of $\sim 10^9$−10^{15} cycles has been demonstrated for use in the 1T-1C structure of FeRAM, while in the 1T structure FeFETs, an endurance of $\sim 10^6$ cycles is achieved, which is probably limited by trapping.[95,97] An NVRAM integrated into 28 nm technology node with an endurance of $>10^6$ cycles is expected as a good product to compete with embedded flash memory solutions at 28 nm and beyond nodes. In the future, some more work like identifying the best array architecture (NAND), identifying the best and reliable

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programming methods, best sensing schemes, and finally showing reliability on the array level is needed.

2.3. Organic Ferroelectrics. In 1921, the first insight between organic molecules and ferroelectricity was realized with the discovery of the ferroelectric nature in Rochelle salt-containing organic tartrate ions.[41] Organic ferroelectrics show a potential candidature due to the low crystallization temperature (<200 °C) and minor interdiffusion, interfacial reactions with silicon, and possibility to directly integrate with forefront silicon process technology without the need of a buffer layer. Also, organic ferroelectrics can be fabricated using low-cost manufacturing techniques such as spin coating, drop cast, and sol−gel, which can also be utilized for future flexible electronics. Numerous organic ferroelectric systems have been investigated, for instance (i) single-compound (polar) organic molecules (Tthiourea, TEMPO, CDA, TCAA, benzil, DNP, TCHM, VDF oligomer, CT complexes, TTF-CA, and TTF-BA); (ii) H-bonded supramolecules (Phz-H_2 ca, Phz-H_2ba, [H-55dmbp][Hia], clathrate, β-quinol-methanol, Nylon-11, PVDF, and PVDF copolymers (PVDF-TrFE, PVDF-PMMA, PVDF-GO)).[20] Among the aforesaid, polyvinylidene fluoride (PVDF) and copolymers show superior ferroelectric properties and are widely used for various device applications. Principally from a scaling point of view, P(VDF-TrFE) thin films showed ferroelectricity down to two monolayers (1 nm) and thus have tremendous potential for use in next-generation ultrascaled and flexible electronics.[42] The 1 nm P(VDF-TrFE) thin film formation is reported by the Langmuir−Blodgett technique, which is not user-friendly compared to traditional semiconductor manufacturing spin-cast. Organic ferroelectrics research mainly focuses on PVDF and copolymers that show superior ferroelectric properties compared to their competitors.

PVDF $(\text{-}CH_2\text{-}CF_2\text{-})_n$ is a semicrystalline polymer of minimal four diverse polymorphs such as α, β, γ, and δ phase, out of which β, γ and δ are ferroelectric phases, and α is paraelectric.[98] The biggest roadblock for PVDF usage in microelectronic applications is the formation of uniform and homogeneous thin ferroelectric films of PVDF. Usually, low-quality porous PVDF films are obtained through the traditional techniques due to the higher hygroscopic nature of films.[99,100] The use of copolymers showed a possible solution to get rid of this concern: P(VDF-TrFE),[101,102] PVDF−PMMA,[103] and PVDF−GO.[104] However, the addition of high copolymer contents (usually >20−25%) degrades the ferroelectric properties of PVDF. Hence, the copolymer's optimum content (<20−25%) is generally added to PVDF to obtain uniform films for microelectronic applications. Thus, P(VDF-TrFE) is an attractive candidate due to convenient thin film formation and the existence of ferroelectricity close to crystallization temperature. Henceforth, considerable efforts were carried out in this direction in past decades to use P(VDF-TrFE) for ferroelectric memory applications.[25] The β-phase P(VDF-TrFE) shows superior ferroelectric properties after postdeposition annealing treatment close to the Curie temperature.[105] However, the Curie temperature of copolymer P(VDF-TrFE) (~80−140 °C) is lower than PVDF (~167 °C). Hence, the high performance and uniform PVDF ferroelectric thin films are highly anticipated. Li et al. reported smooth PVDF films by controlling the humidity and processing temperature, as shown in Figure 3.[99] The SEM micrographs of top and cross-section view of PVDF films deposited at 20 °C and with the effect of relative humidity from 0 to 60% (Figure 3a). It is observed that the films were more porous at a higher relative humidity (60%) and homogeneous and dense at low relative humidity (0%). Similarly, Figure 3b shows the SEM images of the top and cross-section view of PVDF films deposited at a fixed relative humidity (25%) and the variation of substrate temperature from 20 to 100 °C during the deposition process. The smooth and dense films were obtained at ≥90 °C. Alternatively, uniform δ-phase PVDF thin films down to 18 nm, formed by faster evaporation of the solvent during spin coating due to high-temperature processing, are also reported.[98,106] The δ-phase PVDF (P_r = 7 μC/cm^2, E_c = 1.15 MV/cm) showed comparable properties (listed in Table 1) to P(VDF-TrFE) and β-PVDF.

2.4. Two-Dimensional (2D) Ferroelectrics. The 2D materials have attracted the scientific community's immense attention due to their exceptional properties to confine/transport heat and charges within a plane.[24] Ever since the invention of graphene reported in 2004 by Novoselov et al.,[107] numerous 2D materials have been explored, such as hexagonal boron nitride (h-BN),[108] transition metal dichalcogenides (TMDs),[109] Xenes,[110] MXenes,[111] organics,[112] and so on.[113] As compared to bulk form, the van der Waals 2D layered materials show weak interlayer interactions but strong intralayer chemical bonds. Thus, the atomically thin 2D materials with weak van der waal forces amid adjacent layers, low surface roughness, and above all, dangling bond free surface can provide a strong scaling advantage as compared to the bulk form. Various 2D ferroelectric materials are theoretically explored in this regard, as reviewed by Guan et al.[24] However, ferroelectricity in only scarce 2D materials is experimentally validated, such as In_2Se_3,[114] SnTe,[115] d1T-$MoTe_2$,[116] WTe_2,[117] $CuInP_2S_6$,[118] and BA_2PbCl_4.[119] These experimental results are generally debated because of the weak piezoresponse force microscopy (PFM) signals. Therefore, here we focus on some of the experimental reports, from a nonvolatile memory point of view, as listed in Table 1, detailed as follows:

- Group III−VI: The Group III−VI-based 2D ferroelectric materials are broadly investigated, especially indium selenide (In_2Se_3). In_2Se_3 is known to be in five forms α, β, γ, δ, and κ from which the α phase is most stable at room temperature (RT). Thus, α-In_2Se_3 is widely reported to be ferroelectric, though the exact mechanism of ferroelectricity is still argued to be structural distortion, dipole effect, or dipole locking.[47,114,120−124] For α-In_2Se_3, a small E_c of ~0.2 MV/cm is reported.[114] Alternatively, α-In_2Se_3 as a semiconductor channel in FET is also demonstrated.[125]
- Group IV tellurides: The 2D Group IV tellurides of form XTe (where X can be Si, Ge, Sn) are also predicted to be ferroelectric. Experimentally, the 2D SnTe showed spontaneous polarization at liquid helium temperature. As compared to the T_c of bulk SnTe (98 K), the T_c of 1 unit cell SnTe increases to ~270 K.[115] It would be interesting to see ferroelectricity at room temperature to compete with alternate 2D ferroelectric materials.
- Transition metal dichalcogenides (TMD): The TMD materials of form MX_2 (transition metal (M), e.g., Mo, W, and chalcogenide atom (X), e.g., S, Se, and Te) have gained interest for electronics, optoelectronics, and valleytronics.[126] The distorted 1T (d1T) and trimerized (t) phases of TMDs are theoretically predicted to show ferroelectricity.[127] Here, ferroelectricity was shown in the d1T phase of MoS_2 (d1T-MoS_2), due to in-plane Mo displacement of centrosymmetric 1T-MoS_2 and spontaneous dielectric polarization. Recently, out-of-plane ferroelectricity is demonstrated in the d1T phase of monolayer $MoTe_2$ (d1T-$MoTe_2$) at 300 K.[116] Here, we roughly estimate an E_c of ~1 V from the PFM results in a monolayer $MoTe_2$, which corresponds to a pretty good E_c of ~10 MV/cm. Mysteriously, the topological semimetal WTe_2 (two-three layers) also exhibits spontaneous out-of-plane polarization, even if its monolayer is centrosymmetric and nonpolar.[117]
- Transition metal thiophosphate (TMTP): The transition metal thiophosphate (TMTP) family of the form ABP_2X_6 (where A/B is divalent-divalent or monovalent-trivalent blend and X is a chalcogenide such as S, Se, Te) is also predicted to show ferroelectricity. From the TMTPs, ferroelectricity in a few layer (~4 nm) $CuInP_2S_6$ flakes is experimentally demonstrated using PFM.[118] From our estimation, the $P-V$ hysteresis curves, ~2 V E_c is seen for a ~4 nm $CuInP_2S_6$ flake, which corresponds to an E_c of ~5 MV/cm.
- Hybrid (organic−inorganic): The hybrid 2D materials have also shown ferroelectricity, particularly from the Ruddlesden−Popper family of the form $A_{n+1}B_nX_{3n+1}$, (A-, B-site cations and X anions). From this class, bis(benzyl ammonium) lead tetrachloride (BA_2PbCl_4) has experimentally proven ferroelectricity at room temperature. Here, ferroelectricity down to one unit cell (2 vdW layers) is demonstrated due to the in-plane polarization and ordering of electric dipoles to circumvent the depolarization field.[119]

In summary, from the 2D ferroelectric materials, generally, a higher E_c ranging from 0.2 to 10 MV/cm is observed compared to the thin film

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competitors. This is a sound understanding for the memory application point of view, as compared to the competing materials, provided the material is not fatigued. Ferroelectric fatigue can result in reduced P_r values and enhanced E_c values. Also, the weak PFM signal is still debated. Nevertheless, the research on 2D ferroelectrics materials is in the nascent phase.

Since bulk ferroelectrics need a high voltage for reorientation of ferroelectric polarization, they are apparently not suitable for scaled high-volume manufacturing CMOS technology. Therefore, reorientation of ferroelectric polarization enabled by in-plane polarization of ferroelectric thin films is believed to be suitable for lower electric voltage and hence low-power device applications.[128] Alternatively, it is expected that the out-of-plane polarization also (e.g., as predicted for single unit cell 2D ferroelectrics like In_2Se_3) would work similarly as traditional ferroelectric materials in device structures, for instance, to screen the semiconductor channel charges with electric field variation in ferroelectric/semiconductor systems such as MFS, MFIS, and MFMIS device structures.

Nonetheless, it is hard to precisely predict whether in-plane polarization has a particular application for next-generation computing and storage explicitly. Instead, in the future, the integration of 2D ferroelectrics in device structures and the corresponding device results can give a better idea about the actual use of 2D ferroelectrics in computing and storage applications. Much future scope exists on exploring alternate 2D ferroelectric materials, obtaining ferroelectricity at room temperature, and reasonable P_r and E_c on large-area thin films. The imprint, endurance/fatigue, and statistical variations must also be taken care of from a reliability perspective. Additionally, CMOS compatibility must be taken into consideration for high-volume manufacturing. From materials perspectives, further, the essential ferroelectric materials characteristics are discussed in section 3.

3. FERROELECTRIC CHARACTERISTICS

3.1. Conventional Polarization vs Electric Field (P–E) Characteristics of Ferroelectrics. As stated earlier, the ferroelectric materials utilize the ferroelectric effect, i.e., dipole's tendency to instinctively polarize in a particular orientation under the directional electric field's influence and remain polarized even on removal of the electric field. The orientation of polarization can be reversed on applying the reverse electric field. Thus, the system has two stable polarization states (i.e., remanent polarization states $+P_r$ and $-P_r$ as shown in Figure 4) and is used to store nonvolatile digital information, i.e., logic '0' and logic '1'. The inset of Figure 4 shows how the center atom displaces in perovskite (ABO_3) structures with variation in the electric field. Miller et al.[129] projected a modest mathematical fitting model for the experimental P–E relation in a ferroelectric capacitor that fits well to a saturated hysteresis loop but not to a nonsaturated (minor) hysteresis loop. Later, Lue et al.[130] revised the Miller model that explains the saturated as well as the nonsaturated P–E hysteresis loops, as follows:

$$P^{+}(E,\ E_m) = P_s \tanh\left(\frac{E - E_c}{2\delta}\right) + \varepsilon_f\varepsilon_o E + P_a \quad (1)$$

$$P^{-}(E,\ E_m) = P_s \tanh\left(\frac{E - E_c}{2\delta}\right) + \varepsilon_f\varepsilon_o E - P_a \quad (2)$$

$$\delta = E_c\left(\ln\left(\frac{P_s + P_r}{P_s - P_r}\right)\right)^{-1} \quad (3)$$

where $P^{+}(E, E_m)$ and $P^{-}(E,E_m)$ are the positive and negative-going branches of the P–E relation, respectively. The dipole moment's linear contribution is denoted by the term "$\varepsilon_f\varepsilon_o E$". E_m is the maximum electric field, and the polarization is related to E_m as follows:

$$P_a = \frac{1}{2}\left(P_s \tanh\left(\frac{E_m + E_c}{2\delta}\right) - P_s \tanh\left(\frac{E_m - E_c}{2\delta}\right)\right) \quad (4)$$

Initially, the unpolarized ferroelectric material is at the origin ($P = 0$, $E = 0$). When the electric field is increased, the dipole moment follows the polarization curve until it reaches E_m. After this, the polarization follows $P^{+}(E, E_m)$ and $P^{-}(E, E_m)$. Using eqs 1–4, the P–E loop is simulated (Figure 4). Here, the parameters taken for simulation are coercive field (E_c), remnant polarization (P_r), saturation polarization (P_s), the dielectric constant of ferroelectric (ε_f), and thickness of ferroelectric (t_f) with values 50 kV/cm, 2.5 μC/cm^2, 3 μC/cm^2, 150, and 200 nm, respectively.

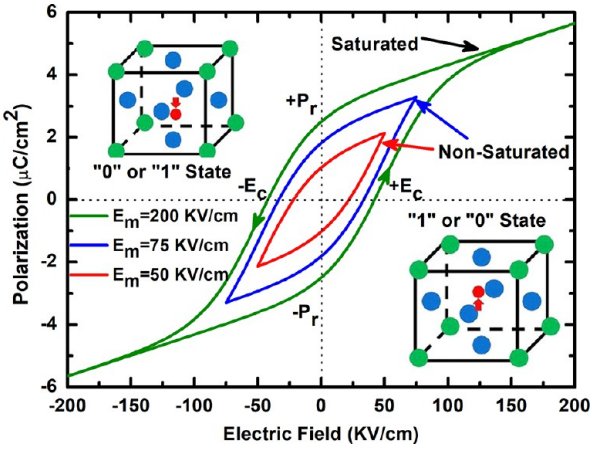

Figure 4. Simulated P–E characteristics for a typical ferroelectric material with variation in the maximum electric field using eqs 1–4.[130] The inset shows how the center displaces in ferroelectric perovskites on application of an electric field.

3.2. Negative Capacitance (NC) in Ferroelectrics. In 1956, Merz et al. detected the transient behavior of negative capacitance (NC) characteristics.[131] Later, In 1957, Landauer et al. portrayed the ferroelectrics P–E characteristics with the NC region.[132] In 2006, Bratkovsky et al. performed a successful measurement of the entire intrinsic hysteresis loop.[141] Later, in 2008, Salahuddin and Datta proposed using NC behavior to provide voltage amplification and achieve sub-60 mV/dec low power devices.[133] Figure 5 shows the transient nature of the negative capacitance effect. The side panels show the instantaneous distribution of the charges on the electrodes (gray) and the ferroelectricity due to polarization reversal that occurs through the domain growth mechanism. Here, polarization direction and electric field are shown by yellow/white and black arrows, respectively. The center panel represents the correlation between charge distributions and the experimentally measured ferroelectric P–E loop characteristics; P is a function of ferroelectric internal node voltage (dotted blue curve) and the voltage across the ferroelectric capacitor (green curve).[134,135] Figure 5b shows the energy landscape of ferroelectrics, where the ferroelectric resides in two polarization states ($+P_r$ and $-P_r$), which can be related to local energy minima states or wells of ferroelectric (denoted by solid green circles in Figure 5b). The negative capacitance region is a nonequilibrium state that lies in between these two states, represented by the dotted box (i.e., where the charge is nearly zero). Suppose a ferroelectric is brought to this unstable negative capacitance state (solid blue

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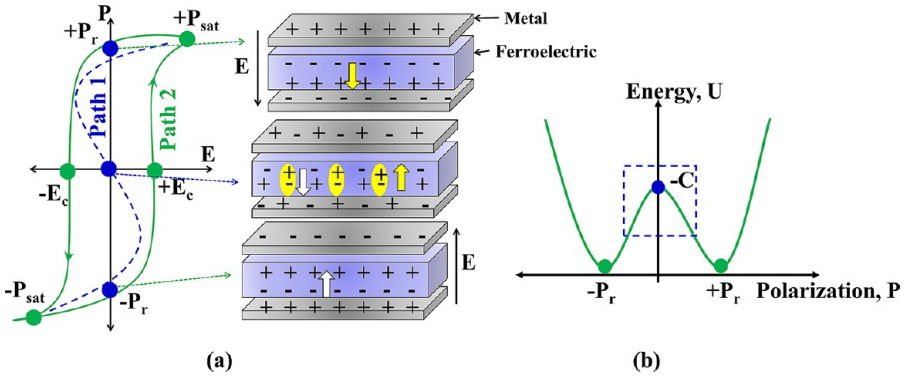

Figure 5. (a) Transient nature of the NC effect, (b) energy landscape of ferroelectric materials, where the dotted box indicate the NC region. Conventional ferroelectric (green curve) and NC behavior (blue curve).[134,135]

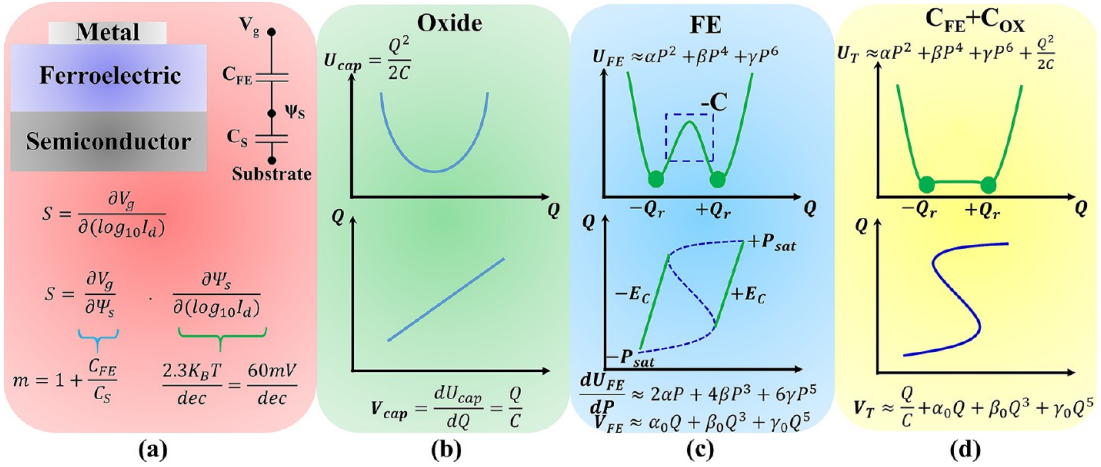

Figure 6. Mechanism of negative capacitance stabilization. (a) The metal/ferroelectric/semiconductor (MFS), structure and corresponding capacitor divider model. Energy landscape (energy (U) vs charge (Q)) and charge (Q) vs voltage (V) characteristics of (b) conventional dielectric positive capacitor (can be related to the LK equation where $\alpha = \beta = 0$), (c) ferroelectric material which follows the (Landau−Khalatnikov) LK equation, $E = 2\alpha P + 4\beta P^3 + 6\gamma P^5$, (d) ferroelectric capacitor (NC) in series with a positive capacitor.

circle). In that case, it falls to one of its two energy minima states or wells, where the capacitance is positive.[136] NC-FET's principle is ferroelectric materials stabilization in this NC region (where dQ/dV is negative). Feynman's lectures on physics[137] suggest that the Clausius−Mossotti equation can explain this negative capacitance region's mechanism in the ferroelectric crystal. According to the Clausius−Mossotti equation, the dielectric constant (κ) of liquids is estimated as $\kappa - 1 = N\alpha/(1 - (N\alpha/3))$, where α is the polarizability of the atom. For a crystal, the factor 1/3 is not exactly equal to 1/3 but near to it. In fact, for a simple cubic crystal, it is just 1/3. In this equation, if $N\alpha$ becomes greater than 3, then κ would become negative, but this cannot be right. However, if α increases in a particular crystal, polarization results in a higher local field, which in turn polarizes every atom more and raises the local field higher. Thus, polarization keeps on increasing without limit due to such a kind of feedback (with the assumption that each atom's polarization rises proportional to the field). This kind of "runaway" state arises when $N\alpha = 3$. However, the polarization does not reach infinite because at higher fields the proportionality of P and E, i.e., $P = \alpha\varepsilon_o E$, breaks down such that equations become invalid.[137] Thus, the mechanism behind the negative capacitance region is understood on the basis of the "positive feedback mechanism" also labeled "internal voltage amplification".[133] However, there is still debate around the issue if a real-world polycrystalline and multidomain ferroelectric can really be stabilized in the desired NC state. For instance, the charge across a ferroelectric capacitor is related as $Q_f = C_f V_f$, where C_f and V_f are the ferroelectric capacitance and voltage, respectively. The decrease of V_f with increased Q_f can be interpreted as a sudden increase of positive C_f,[138] i.e., increasing $C(t)$ or PC model or decrease in voltage across the interfacial layer (between metal and ferroelectric) due to resistance (R_i) degradation (i.e., varying $R_i(t)$ model). Figure 5a shows the $P-E$ loop of a ferroelectric capacitor and two paths that the ferroelectric material may follow when the polarization is switched from $-P_r$ to $+P_r$. Along Path 1, the ferroelectric layer homogeneously varies from $-P_r$ to $+P_r$ polarization state, with an intermediate state (NC state) around $P = 0$, $E = 0$, neglecting any domain boundary related energy. However, conventional ferroelectric switching involves inverse nucleation and domain growth, which requires a swift charge supply from the source voltage, denoted by Path 2 of Figure 5a.

Conversely, the NC state is claimed to be directly observed by connecting a considerable resistance in series to a ferroelectric capacitor.[134] This process limits the supply of charges from the supply voltage, and a ferroelectric may follow Path 1. However, around this NC state, the curve must go through a maximum energy state as indicated by the $U-P$ curve in Figure 5b, which is unlikely to occur because of the higher energy cost compared to

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the domain formation related energy. Therefore, Path 2 may be suited to explain the results of ref 134 without involving any NC effect, e.g., due to variation in interfacial layer resistance[138−141] and/or due to decreased ferroelectric capacitor voltage,[142] that may consequence to voltage enhancement in the remaining circuit.[39] Thus, the NC effect is still debated from the understanding perspective.

As per the current scenario, the NC effect and NC stabilization steps are easy to understand from the presentation in Figure 6. From Figure 6a, the subthreshold swing S is m times 60 mV/dec, where m is called the body factor. This signifies that to reduce S below 60 mV/dec, m must be reduced below 1; i.e., $m = 1 + \frac{C_{FE}}{C_S} < 1$ implies $|C_S| > |C_{FE}|$. To ensure this, $|C_{FE}|$ and $|C_S|$ must be carefully considered. Figure 6b shows for a conventional positive capacitor, the energy landscape $U_{cap} = Q^2/2C$ and voltage (V) vs charge (Q) characteristics, depicting linear $Q-V$ characteristics, which can be related to the LK equation where $\alpha = \beta = 0$. Likewise, Figure 6c shows the energy landscape and $Q-V$ characteristics for a ferroelectric capacitor, that follows, $U_{FE} \approx \varepsilon P^2 + \varepsilon P^4 + \varepsilon P^6$, and $V_{FE} = \frac{dU_{FE}}{dP} \approx \alpha P + 4\beta P^3 + 6\gamma P^5$, or $V_{FE} \approx \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5$, assuming one-dimensional spatial variations and steady-state conditions,[133] where Q is polarization (P) per unit area. Graphically, from the energy landscape of the positive capacitor Figure 6b and a ferroelectric capacitor Figure 6c in the negative capacitance region (blue dotted box), it can be observed that both have opposite behavior. If both can be combined in series, then the resulting energy landscape picture can look like that shown in Figure 6d. Therefore, now the curve does not need to travel uphill the energy curve (Figure 6c), instead follow a direct path (Figure 6d), which is feasible. Thus, keeping $|C_S| > |C_{FE}|$ implies $m < 1$ and achieves ultralow sub-60 mV/dec S. However, the complete understanding of the ferroelectric NC effect is still under study. Furthermore, the NC effect is not restricted to FETs, instead also applicable to wide-ranging two-state systems parted by an intrinsic barrier (stored energy), e.g., piezoelectric gate barrier transistors, tunneling relays, NEMS devices, HEMT, etc.[136,143−148] The FET devices based on the NC effect are further discussed in section 5.1. From ferroelectric materials and their characteristics, further, we move to the device structures as discussed in section 4.

4. DEVICE STRUCTURES

The ferroelectric materials are investigated in various device structures depending on the targeted applications. Figure 7 shows the principally used four device structures employed for logic and memory applications, i.e., (a) metal/ferroelectric/metal (MFM) capacitor, (b) metal/ferroelectric/semiconductor (MFS), (c) metal/ferroelectric/insulator/semiconductor (MFIS), and (d) metal/ferroelectric/metal/insulator/semiconductor (MFMIS) structures.

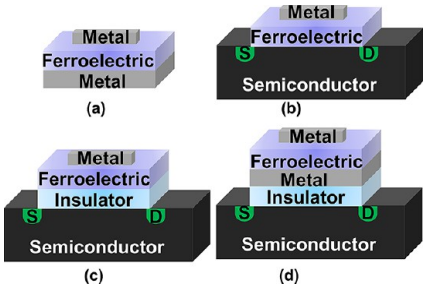

Figure 7. Ferroelectric devices structures: (a) MFM capacitor structure, (b) MFS structure, (c) MFIS structure, and (d) MFMIS structure.

Generally, the MFM capacitor structure (as shown in Figure 7a, usually fabricated on an insulated system that is SiO_2/Si dummy substrate) is used as a reference to extract the $P-E$ characteristics of the ferroelectrics and give an estimate of the general ferroelectric properties such as P_r and E_c. A simple method to extract the $P-E$ characteristics is to input a triangular wave to the MFM capacitors and measure the corresponding charge (Q)−voltage (V) characteristics, further related to the $P-E$ characteristics. The MFM structure is also used as a capacitor element in the 1T-1C-type FeRAM devices. Additionally, if the ferroelectric layer is made too thin, down to a few nanometers in the MFM structure, quantum mechanics dominate, which is more useful for FTJ devices, as detailed later in Section 5.4.

The ferroelectric materials integration into the FET's gate stack is employed in three popular device configurations: MFS, MFIS, and MFMIS device structures, which are famous for 1T-type FeFET or NC-FET device applications. NC-FET can be considered a FeFET as both have similar device structures. The main difference is that, in NC-FET, the ferroelectric is stabilized in the NC state. Here, we use the terminology FeFET for ease unless stated otherwise. However, it must be remembered that the operation of both is different, especially with NC-FET targeting hysteresis-free logic applications and FeFET pointing hysteretic nonvolatile memory applications.

MFS structure (Figure 7b) is the simplest FET device structure where a ferroelectric material replaces a traditional MOSFET's gate oxide. On top of that, the MFS device structure can be appropriate for low thermal budget applications such as organics, where interface reactions are not too harsh, and the ferroelectric layer provides good insulation. For general inorganic-type CMOS-compatible applications, the MFS structure's performance is hindered by the interdiffusion and interface reaction amid the semiconductors ferroelectric system. Thus, it results in the degradation of device performance, reliability, and complexity in process technology integration.[27,54,77,149−152]

The MFIS structure (Figure 7c) provides the solution to overcome the interface reaction and interdiffusion concern. In the MFIS structure, an additional insulating/buffer layer is introduced amid the semiconductor and ferroelectric structure to enhance the reliability of the devices.[153−155] The buffer layer prevents the interdiffusion and interface reactions and provides a potential barrier for charge injection between ferroelectric and semiconductor substrate.[13] Additionally, the buffer layer also provides better insulating properties by minimizing the gate leakage current, and the impact of leakage current can only be localized on the film's weak spots. Therefore, the MFIS structure is widely adopted and is a superlative configuration for FeFET device applications. Moreover, the ferroelectric/insulator capacitance matching is also considered useful for stabilizing the ferroelectric in the negative capacitance region.[136]

Another alternative is the MFMIS structure (Figure 7d), which requires higher gate stack thickness and an extra processing step, and the leakage current spreads to the floating metal that destroys the charge neutrality in a short time resulting in low retention particularly for FeFET devices. This is a big concern compared to an MFIS structure where the effect of

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leakage current is only localized on weak spots in a film and gives better retention. However, the MFMIS structure is considered useful for NC-FET device investigations where the floating metal serves as an internal gate electrode to estimate the voltage amplification.[133] It is also proposed that the internal metal electrode can provide stable capacitance matching to achieve sub-60 mV/dec S in an NC-FET.[156]

4.1. Challenges in MFIS Structure of FeFET and Remedies. From the preceding discussions, it is clear that the MFIS device structure is superlative for FeFET devices and is likely for NC-FET device applications. The inclusion of a buffer layer to form the MFIS structure of FeFET improves devices' performance and reliability. The MFIS structure suffers from the following fundamental integration issues, especially for FeFET as NVM applications.[157]

4.1.1. Depolarization Field. The reliability of FeFET, especially the data retention characteristics, are degraded by the inclusion of insulator layer between ferroelectric and semiconductor surface. The data retention implies the aging for which the device can hold the stored digital information. The electrical equivalent circuit of the MFIS structure of FeFET can be imagined as a series combination of the ferroelectric capacitor and dielectric capacitor. A write voltage is applied as a gate voltage to write/store logic 0 or logic 1 in the FeFET devices during the write operation. A small read voltage near the flat band voltage is applied for retention evaluation during the retention test as the supply power is switched off (or, say, the gate terminal is grounded). Since the gate terminal of FeFET is grounded, the ferroelectric capacitor's bottom electrode is short-circuited with the top electrode of the dielectric capacitor. Henceforth, the charge $\pm Q$ appears on both capacitors' electrodes because of the ferroelectric remanent polarization P_r and maintaining charge neutrality at the node amid both capacitors. Therefore, under a short-circuit condition, the charge in a dielectric capacitor is $Q = CV$ due to the charge−voltage relation of the capacitor; consequently, in a ferroelectric capacitor, it becomes $Q = -CV$, which signifies that the electric field direction in ferroelectric and polarization is opposite to each other. This field that opposes the polarization direction is called the depolarizing field and reduces the retention time.[157]

The solution to this problem is to reduce the depolarizing field by reducing the ratio of the dielectric constants of ferroelectric to the buffer layer. In other words, either the buffer layer with high permittivity or ferroelectric film with a low permittivity are required. Also, it must be noted that the leakage current across both the ferroelectric and buffer layers must be considerably low. If not, the charge neutrality condition at the node amid both capacitors can be suppressed, and charges on buffer layer electrodes disappear and subsequently charges vanish on the semiconductor surface. Hence, stored information cannot be read by FeFET's drain current, even if ferroelectric film polarization is retained.[13] Mathematically, the depolarization field (E_{dep}) is expressed as

$$E_{dep} = P_r\left[\varepsilon_f\varepsilon_o\left(\frac{C_{IS}}{C_F} + 1\right)\right]^{-1} \tag{5}$$

$$C_{IS} = \frac{C_{IL}C_S}{C_{IL} + C_S} \tag{6}$$

where P_r, ε_f, ε_0, C_{IL}, C_F, and C_{IS} are the remanent polarization, dielectric constant of ferroelectric, permittivity of free space, the capacitance of interfacial layer between ferroelectric and the semiconductor substrate, capacitance of ferroelectric, and capacitance of series combination of C_{IL} and C_S, respectively. According to eq 5, until C_{IS} becomes infinite, a significant depolarization field exists, reducing the ferroelectric film's polarization. Using eq 6, when $C_{IS} = C_{IL}$, then $C_s = \infty$. On the other hand, C_{IS} is minimum, in strong inversion, i.e., when depletion region thickness becomes maximum (W_{d_max}), and C_s is minimized. Therefore,

$$\frac{C_{IL}C_{S\_min}}{C_{IL} + C_{S\_min}} \le C_{IS} \le C_{IL} \tag{7}$$

$$C_{S\_min} = \frac{\varepsilon_o\varepsilon_S}{W_{d\_max}} = \sqrt{\frac{\varepsilon_o\varepsilon_S q^2 N_a}{4kT\ \ln(N_a/n_i)}} \tag{8}$$

where N_a, n_i, k, and T are the doping concentration in the silicon substrate (p-type), the intrinsic carrier concentration, the Boltzmann constant, and the absolute temperature, respectively. Using eqs 5−8, the depolarization field can be expressed as

$$P\left[\varepsilon_f\varepsilon_o\left(\frac{\varepsilon_{IL}d_f}{\varepsilon_f d_{IL}} + 1\right)\right]^{-1} \le E_{dep} \le P\left[\varepsilon_f\varepsilon_o\left(\frac{C_{IS\_min}}{C_f} + 1\right)\right]^{-1} \tag{9}$$

4.1.2. Voltage Drop Across Buffer Layer. The electrical equivalent circuit of the MFIS structure of FeFET is series combination of ferroelectric and insulator dielectric capacitors. Therefore, any applied gate voltage is divided among both the capacitors, i.e., total voltage (V_t) is equal to the sum of voltage across ferroelectric (V_f) + voltage across insulator (V_i) capacitors. The voltage across both capacitors can be estimated by the following eq 10. According to the charge matching condition, the charge across both capacitors must be equal, i.e.,

$$Q_f = Q_i \Rightarrow C_fV_f = C_iV_i \Rightarrow \frac{\varepsilon_f}{T_f}V_f = \frac{\varepsilon_i}{T_i}V \tag{10}$$

where Q_f, C_f,V_f, ϵ_f, T_f, and Q_i,C_i,V_i, ϵ_i,T_f are the charge, capacitance, voltage, dielectric constant, thickness of ferroelectric and insulator layer, respectively. Since the dielectric constant of ferroelectric (ϵ_f) is much larger than that of insulator (ϵ_i), $C_f \gg C_i$, consequently $V_f \ll V_i$. Thus, most of the gate voltage is applied across the insulator layer. This leads to high electric fields in the insulator compared to ferroelectric, resulting in the insulator layer's breakdown, sometimes even before the ferroelectric gets polarized. The solution to this problem is to minimize the voltage drop across buffer insulator by increasing the ratio of the insulator capacitance, C_i to the ferroelectric capacitance, C_f, i.e., by using thin films of the insulator and ferroelectric materials of comparable dielectric constant.

4.1.3. Extra Processing Steps and Gate Stack Thickness. The MFIS structure of FeFET results in an extra fabrication step to deposit insulator thin film before the ferroelectric and adds to extra gate stack thickness. Thus, a high gate stack thickness may cause cross-coupling capacitance issues among adjacent devices in next-generation ultrascaled device structures. So, a ferroelectric material with high interface quality in direct conformal contact with a semiconductor would be a great solution.

4.1.4. Three-Dimensional Structures. Three-dimensional (3D) architectures need to be introduced to realize high-density products in the consumer market. 3D integration of conventional perovskites (e.g., PZT or SBT) is currently a challenge due to the limited thickness scalability of perovskite ferroelectrics, particularly forming a 3D perovskite capacitor. Samsung

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succeeded in growing columnar PZT on trench sidewalls with good ferroelectric switching behavior, only with larger trench holes (>0.40 μm). Still, the grain growth mechanism in trench holes is needed to be enlightened, and novel methods are needed to grow columnar PZT in smaller trench holes (<0.4 μm).[30,158,159]

4.1.5. Multibit Storage in a Single Memory Cell for NVM. The possibility of multilevel storage in a single cell of NVM is required to improve the storage density and cost per bit. For instance, the current state-of-the-art NAND flash technology utilizes three-bit (i.e., 8 states/level) data storage in a single cell. Therefore, for FeFETs to replace data memories, multibit data storage is needed. Here, we prefer to use the term multibit instead of multilevel, which is generally confusing; e.g., three-bit multilevel storage can be confused with incorrect three levels, while three-bit multibit storage specifies that three bits corresponds to 2^3 = 8 memory states/levels. In principle, ferroelectrics store two states ("0" and "1") corresponding to two saturated polarization states $+P_s$ and $-P_s$. However, one can obtain intermediate polarization values between $+P_s$ and $-P_s$ by altering the up-polarization ($+P_s$) and down-polarization ($-P_s$) domain ratios, as shown in Figure 4. But, it is hard to achieve a controlled intermediate polarization state because of the stochastic, complex polarization nature.[29,160] The conventional method of attaining an intermediate polarization between $-P_s$ and $+P_s$ adjusts the strength (e.g., electric pulse's amplitude and width). However, the method is not consistent for multibit storage because variations in defect distribution and fatigue in ferroelectric materials can cause a considerable variation in ΔP, even for similar applied electrical pulses. Therefore, two reliable polarization states of ferroelectrics are generally preferred. Nevertheless, attaining reliable multibit polarization states would be an outstanding achievement. Mulaosmanovic et al.[161] reported multibit capability in ferroelectric HfO_2. Three storage states are revealed in TiN/Si:HfO_2/SiON/Si, MFIS structure of FeFET that remain distinguishable after 10 h of a retention test at room temperature and showed >10^5 cycles endurance with program pulse of 500 ns. Lee et al.[162] proposed a new method for multibit storage in ferroelectric by current control during polarization switching. The displacement current density (J_D) escorts the polarization switching process. In 1861, Maxwell first introduced J_D in the theory of electromagnetism. J_D is defined as the rate of change of electric polarization and/or field, related as[163]

$$J_D = \frac{\partial P}{\partial t} + \varepsilon_o \frac{\partial E}{\partial t} \tag{11}$$

where ε_0 is the permittivity of free space. During polarization switching, the displacement current density (J_D) originates between the capacitor plates, whose magnitude is equal to the capacitor's wires' conduction current. This approach aims to limit the current outflow generated from J_D, which can control polarization's switching speed. A cycling process was used to write eight different states by adjusting J_D and hysteresis pulse measurements to measure the polarization change. The neighboring states were separated with a margin of ~15 μC/cm^2. It would be fascinating to see how this concept can be realized in real FeFET memory devices and the realization of next-generation 3D architectures. Further, we turn to the ferroelectric device application in section 5.

5. FERROELECTRIC DEVICES

Here, we catalog the operating principle, recent progress, and possible use of emerging ferroelectric materials in devices at all levels of the memory hierarchy, as (i) ferroelectric negative capacitance field effect transistors (NC-FET): 1T structure for low power CMOS logic; (ii) ferroelectric RAM (FeRAM): 1T-1C structure with fast access time, high endurance, moderate data retention, and destructive readout to compete with volatile DRAM; (iii) ferroelectric field effect transistors (FeFET): 1T structure with nondestructive readout, fast access time, moderate endurance and high retention time (>10 years) for NVM have the potential to substitute embedded solid-state drives inside the computer; and (iv) ferroelectric tunnel junctions (FTJ) or ferroelectric resistive random access memory (FR-RAM) with a 3D X-point device structure may work for high-density niche storage applications to interchange low-cost per bit external HDDs and may compete with SSDs as well.

5.1. Negative Capacitance Field Effect Transistors (NC-FETs). The performance and functionality of integrated circuits (ICs) have been directed by the scaling, innovation, and evolution of complementary metal oxide semiconductor (CMOS) technology driven by Moore's Law. However, ever-increasing power dissipation with scaling has brought various CMOS technology challenges. The origin of this excess power dissipation concern of CMOS technology is primarily called "Boltzmann tyranny." This means to obtain a 10-fold increase in drain current (I_D) at 300 K, a minimum increase of K_bT log 10 = 60 mV/dec in gate voltage (V_G) is required. Here K_b and T are the Boltzmann constant and temperature, respectively. Thus, the subthreshold swing's theoretical limit is 60 mV/dec at 300 K. Thus, to achieve an acceptable on−off ratio (generally >10^6) of current, ~1 V needs to be applied to the gate. Lowering the subthreshold swing can lower the power dissipation and the supply voltage. However, the scaling of supply voltage <1 V is at a much slower pace, e.g., according to International Technology Roadmap for Semiconductors (ITRS) 2015, the supply voltage is approaching ~0.8 V,[5] resulting in a reduced self-heating effect.[164] Additionally, microprocessor power density is proportional to load capacitance (C_L), supply voltage (V_{dd}), and the switching frequency (f) is equal to half of the operating frequency.

$$\text{power} = C_L V_{DD}^2 f \tag{12}$$

Since V_{dd} is scaling at a slower pace ~0.8 V, and C_L continuously increases, it results in unmanageable power dissipation. Therefore, a further increase in operating frequency has slowed down to manage the excess power dissipation. This major physical limitation of CMOS technology is addressed by novel devices such as tunnel FETs (TFET),[165] feedback FETs,[166] impact ionization metal oxide semiconductor transistors (IMOS),[167,168] nanoelectromechanical FETs (NEMFETs),[169] NC-FeFET or NC-FET.[133] Among the aforesaid, NC-FET is a promising aspirant due to the feasibility of easy adoption in current high-volume manufacturing of CMOS technology.

The NC effect in ferroelectrics is detailed earlier in section 3.2. In the MFS structure, where the gate oxide of conventional FET is replaced with a ferroelectric material. The total capacitance (C_T) in the conventional FET metal−insulator-semiconductor (MIS) structure is given by

$$C_T = \frac{C_S C_{OX}}{C_S + C_{OX}} \tag{13}$$

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where C_S and C_{OX} are the semiconductor and oxide capacitances, respectively. In the conventional FET, both capacitors (C_S and C_{OX}) are positive. Therefore, C_T is smaller than C_S and C_{OX}, while, in NC-FET, C_S is positive, but C_{OX} is negative. The denominator term decreases, and hence C_T increases (it must be noted that the system's total capacitance is increased and remains positive). As $Q = CV$, enhanced C_T implies a low voltage is required to produce equal charge quantity in both C_S and C_{OX} capacitors, as both C_S and C_{OX} possess the same charge because of series combination. The semiconductor channel current is directly related to charge across C_S, which deduces that a lower voltage is now required to produce the same amount of current.[164] Therefore, I_{on} is achieved at a significantly lower voltage, which results in the steeper rise in current, corresponding to the reduction of the subthreshold swing (S) below 60 mV/dec. Mathematically, S is expressed as

$$S = \frac{\partial V_G}{\partial \log I_D} = \left(\frac{\partial V_G}{\partial \psi_S}\right)\left(\frac{\partial \psi_S}{\partial \log I_D}\right) \tag{14}$$

where Ψ_S is the surface potential on semiconductor surface, the first term is called body factor (m) and the second term depends on the transport mechanism. For conventional FET, first term (m) is "1", and the second term follows the Boltzmann factor giving $S = 2.3\ K_bT/q = 60$ mV/dec. Although, for NC-FET, second term is fixed, i.e., the transport mechanism is same, first term (m) is varied, i.e., $m < 1$, to reduce the overall S, provided $C_{ox} < 0$ and $|C_{ox}| < |C_S|$. Mathematically,

$$m = \frac{\partial V_G}{\partial \psi_S} = 1 + \frac{C_S}{C_{OX}} \tag{15}$$

Hence, NC-FeFETs may be used to reduce the $V_{dd} < 0.5$ V and therefore are a potential candidate in the current and future era of portable low power electronics.

5.1.1. Headway of NC-FETs Technology. In 2010, the first complete experimental demonstration was reported by Rusu et al. in the Au/P(VDF-TrFE)/Al/SiO_2/Si, MFMIS structure for NC-FET, where the center metal (Al) layer was used as an internal node (ψ_s) to calculate the voltage amplification. Along with S-like charge-voltage characteristics, a subthreshold swing of 46−58 mV/dec was reported using an internal electrode.[170] In 2012, Salvatore et al. suggested five critical points for the accurate design of an NC-FET: (i) the ferroelectric voltage drop, (ii) temperature dependence, (iii) induce a peak in the $C-V$ curve of the gate stack, (iv) increase of current in strong inversion, (v) overlap of the subthreshold region of MOS with the NC region of ferroelectric for steep subthreshold swing (S). Herein, the first two points were addressed: through the voltage drop and the temperature dependence. If the temperature is decreased from T_2 to T_1, the capacitance of ferroelectric varies and results in a wider NC region, and the necessary condition $C_{MOS} \leftarrow C_{FE} < C_{OX}$ is no longer fulfilled.[171] The NC effect was observed if the ferroelectric temperature is kept below its Curie temperature (T_C). Irrespective of the above T_C, the ferroelectric transits into the paraelectric phase, and the NC effect generally vanishes.

Moreover, it was experimentally observed that the NC effect vanishes with an increase in temperature up to 75 °C, much lower than the T_C (~110 °C) of P(VDF-TrFE). It was also suggested that an optimum temperature exists at which the subthreshold swing (S) is minimum. Thus, it concludes that T_C of the ferroelectric must be higher than the operating temperature of integrated circuits (ICs), i.e., ~85 °C.[171] A similar temperature dependence of the NC effect was also reported in the $Pb(Zr_{0.2}Ti_{0.8})O_3/SrTiO_3$ bilayer capacitor structure. Thereby, the NC was stabilized for a temperature range above 573 K up to 773 K (close to T_c of ~430 °C for bulk PZT) and not pertinent to the IC technology as the conventional ICs operate at room temperature, often below 85 °C. However, in this case, the NC effect was observed beyond the T_c and supported that lattice matching of the structure imposes strain that results in the enhanced T_c of PZT. It was also suggested that low T_C ferroelectrics might allow the NC effect to be observed at low temperature.[172] Using this idea, later, the negative capacitance effect at room temperature was demonstrated using low T_c $BaTiO_3$ as the ferroelectric in series with $SrTiO_3$ as a paraelectric electrode.[136,173] In ref 136, (i) $Ba_xSr_{1-x}TiO_3$ (BSTO) was used as a ferroelectric, which gives a significant window for tuning the T_c (ranging from shallow temperatures to that of $BaTiO_3 \approx 110$ °C), where $x = 0.8$ was used that provides $T_C \approx 292$ K;[174] (ii) $LaAlO_3$ (LAO) was used instead of a $SrTiO_3$ dielectric because $LaAlO_3$ shows nearly constant permittivity for a wide range of thickness. Using the ferroelectric-dielectric (FE-DE) superlattice stack, the NC region was stabilized around $Q = 0$ at room temperature. In addition to this, Khan et al. also reported the NC region's direct measurement by adding resistance in series to the ferroelectric.[134] In fact, in earlier NC reports, a series capacitor, i.e., gate dielectric in series with the ferroelectric capacitor, was used in the device structure. This provides an easy way to optimize the NC effect in NC-FETs. Recently, Frank et al.[156] proposed an improvement in NC-FET by employing an ultrathin metal layer between the ferroelectric and semiconductor channel, which provides constant capacitance to the ferroelectric layer and stabilizes the NC region to theoretically achieve an S of 2 mV/dec over 11 decades. A similar idea was earlier implemented by McGuire et al. in metal/P(VDF-TrFE)(~200 nm)/metal/Al_2O_3(20 nm)/MoS_2 MFMIS NC-FETs that showed $S \approx 11.7$ mV/dec.[175] Furthermore, the NC effect in short channel FinFETs by externally connecting a ferroelectric capacitor was also reported with low $S \approx 8.5$ mV/dec.[176]

As discussed by now, CMOS-compatible HfO_2 based dielectrics are a new class of ferroelectrics that can be immediately adopted in the current semiconductor industry. In this regard, NC-FET's concept is desired to be explored for HfO_2-based ferroelectrics NC behavior and dependence on the T_c. Recently, NC-FET's steep slope characteristics using $HfZrO_2$ as the ferroelectric were reported by Cheng et al.[177] withan S of 5 mV/dec and by Lee et al. using the antiferroelectric effect of $HfZrO_2$ with an S of 23 mV/dec.[178] Above all, the hysteresis-free NC effect in HfO_2-based devices is suitable for low-power logic applications. Also, switching speed down to 10 ns is demonstrated, which indicates that ferroelectric HfO_2-based NC-FETs are a promising candidate to provide the speed comparable to SRAM of the current memory hierarchy. Such 1T-type MFIS devices with an access time <10 ns are likely to provide the area and cost advantages over the current 6T SRAM of the current memory hierarchy. Apart from CMOS-compatible reports, sub-60 mV/dec NC-FET devices are also shown on integrating ferroelectrics with 2D TMDs. Generally, it is observed that the capacitance matching is easy to achieve in 2D TMDs compared to the CMOS-compatible Si and Ge semiconductors. The recent experimental reports on NC-FETs especially targeted to reduce subthreshold swing "S" are

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summarized in Table 2. However, the results are mostly debated due to the influence of gate leakage current in the subthreshold region and very few data points in the subthreshold region. It is found that the slow measurement of transfer characteristics gives an accurate capacitance matching.[179,180] Nevertheless, to play as a role model, 2D semiconductor materials still have a long way to go, especially high-quality growth on large-area substrates with carrier mobilities greater than state-of-the-art Si and Ge counterparts.

Table 2. Recent Experimental Reports on NC-FETs at Room Temperature

device structure	S_{min} (mV/dec) forward (F)/reverse (R)	hysteresis (V)	ref
p^+-Si/$HfZrO_2$/Al_2O_3/MoS_2	57.6(F)/52.3(R)	0.012	297
Ag_{NW}/P(VDF-TrFE)/HfO_2/MoS_2	42.5	∼1	298
Au/Ti/P(VDF-TrFE)/Al_2O_3/MoS_2	11.7−14.4		175
Al/P(VDF-TrFE)/MoS_2	24.2−51.2	>7	299
p^+-Si/HfAlO/Ni/HfO_2/MoS_2	57	0.017	300
p^+-Si/HZO/Al_2O_3/MoS_2	23	0.024	301
TiN/HZO/TiN/HfO_2/MoS_2	6.07	∼0.37−5.8	179
p^+-Si/HZO/Al_2O_3/MoS_2	37.6(F)/42.2(R)	∼0.027	302
Al/P(VDF-TrFE)/$MoSe_2$	24.3	>20	299
p^+-Si/HZO/Al_2O_3/WSe_2	40.2(F)/57.5(R)	0.18	180
p^+-Si/HZO/Al_2O_3/Ni/HfO_2/WSe_2	41.6(F)/14.4(R)	0.12	180
Au/P(VDF-TrFE)/SiO_2/Si	13	1	303
Au/P(VDF-TrFE)/TiN + nMOSFET	18	3−4	304
TaN/HZO/SiO_x/Si	42(F)/28(R)	<0.1 V	305
TiN/$HfZrO_2$/TiN/TaN/HfO_2/Si	55	<0.1	306
Au/$BiFeO_3$/(La,Sr)MnO_3 + FinFET	8.5−50	4.5−4.8	307
Au/Ti/PZT/LSMO + FinFET	18−83(F)/6.8−19.6 (R)	0.48−1.02	308
Au/P(VDF-TrFE)/TiN + planar MOSFET	45−52	∼0.04	309
TaN/HZO/SiO_x/Si	52	∼0.1	310
Metal/Si:HfO_2/SiO_x/Si	54	∼0.006	311
TaN/HfAlO/SiO_x/Si	40(F)/39(R)	0.1	312
TaN/HfAlO/SiO_2/Si	25	0.020	313
TaN/HZO/TaN/HfO_2/Ge	47(F)/43(R)	0.04	314
TaN/HZO/TaN/HfO_2/GeSn/Ge	95 (F)/40(R)	0.06	314
TaN/HZO/TaN/HfO_2/GeSn	10	0.1	315
TiN/Al_2O_3/HZO/Al_2O_3/GeO_x/Ge	43(F)/49(R)	0.017	316
TiN/HZO/GeO_x/Ge	54	0.1	317
TaN/HZO/TaN/HfO_2/SiO_2/Ge	29	0.11	318

In summary, the prime challenge to realize an NC-FET is to stabilize the NC region of ferroelectrics at room temperature (e.g., by adding series resistance or capacitance) and achieve hysteresis-free steep subthreshold swing (S < 60 mV/dec) of the devices. However, a diverse range of reports for S < 60 mV/dec are available and compared in Table 2. Hence, the MFIS structure using the ferroelectric NC effect seems suitable for low-power portable computing applications. The NC effect in CMOS-compatible HfO_2-based materials is strongly desired for rapid development and commercial NC-FET-based products.

5.2. Ferroelectric Random-Access Memory (FeRAM). The 1T-1C structure type ferroelectric random access memory (FeRAM) devices achieve nonvolatility by sensing and switching the ferroelectric capacitor's polarization state. In 1952, D. A. Buck proposed using ferroelectric materials for information storage.[181] FeRAM is unique due to its fast access time (theoretically <200 ps[18]), low-power consumption, high security, excellent retention and endurance time, and remarkable radiation tolerance, signifying it to be ideal for consumers, IT, military, and space applications.[182] Current commercial applications of FeRAM are restricted to low-density applications (e.g., identity (ID), radio-frequency identification (RFID) and Smart cards, and other embedded applications) mainly because of the critical thickness limit concern and reliability degradation of perovskite ferroelectric materials at the nanoscale.[183] However, it is controversial whether there is a threshold thickness limit for the existence of ferroelectricity in perovskite ferroelectrics.[184,185] For FeRAM to be the strong candidate for future NVRAM, it is necessary to accomplish the next-generation FeRAM technology node's high-density projected goals. Thus, FeRAM requires nanometer-scale thin ferroelectric material with high reliability, free from fatigue, imprint, and statistical variations.

Since the 1990s, FeRAM became commercially available but lost the race against the scaling advantages offered by Flash memories. Thus, since the 2000s, commercial FeRAM products have been stuck at the 90−130 nm technology node because of reliability concerns.[186−188] FeRAM devices are commercially available but offer destructive readout (DRO) operation. DRO means that after every read cycle, the stored information is lost. Therefore, an additional write cycle is needed after every read cycle. Thus, in the 1T-1C structure, the read and the write operations are limited by the ferroelectric material's cycling endurance. Therefore, an endurance of $>10^{15}$ cycles is essential for such devices. This structure of classical FeRAM is similar to the conventional 1T-1C structure of DRAM, where the capacitor dielectric is replaced by ferroelectric material (Figure 1d). Alternate to 1T-1C, the 2T-2C structure is also proposed to improve the sensing margin but increase the cell size.[4,189,190] For the 1T-1C FeRAM structure, the memory state is defined by the nonvolatile polarization state of the ferroelectric capacitor (1C) element. The stored state is accessed by the transistor (1T) element. The bipolar ferroelectric switching is achieved by adding a plate line to the conventional cross-point architecture of word and bit lines similar to DRAM.[22] Thus, both FeRAM and DRAM use similar sensing schemes and face similar scaling challenges. For instance, with a decrease in the lateral area, the absolute (polarization) charge value per bit also decreases. However, to achieve a high data density of DRAM, 3D integration is the possible solution.[191] But, for FeRAM, 3D integration turns out to be a significant issue (as discussed in section 4.1.4). Therefore, 3D integration of the MFM structure ferroelectric capacitors with high reliability, e.g., fatigue and imprint free, is highly desired for FeRAM to replace DRAM applications.

The commercial 1T-1C FeRAM products available at 130 nm technology node have ∼70 nm PZT thickness in a capacitor on plug (COP) architecture, low data densities of ∼4−64 Mbytes, fast access time of 15−45 ns, good endurance of $>10^{12}$ cycles and data retention of >10 years.[186,187] The only problem of low data

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density could be removed with further scaling of ferroelectric thickness, which comes at the cost of reduced device reliability.[192] Additionally, to achieve high memory density, 3D integration is required, where the problem of achieving ferroelectricity on 3D capacitor sidewalls needs to be overcome without compromising device reliability.[193−195] Recently, with the development of CMOS-compatible HfO_2-based ferroelectrics, the FeRAM devices compatible down to 28 nm technology nodes are demonstrated.[196] Nevertheless, FeRAM devices with a fast read/write access time of 10 ns, endurance 10^{15} cycles, retention >10 years, cell size of $6F^2$, and energy 50 fJ/bit are successfully demonstrated, which are a fairly good option for secure and reliable low-density applications.[11]

5.3. Ferroelectric Field Effect Transistors (FeFETs). In 1957, I. M. Rose enlightened the field with the standard concept of FeFETs for integrated circuits.[197] The ferroelectric layer integrated into the transistor's gate stack, i.e., 1T-type structure, is called an FeFET (Figure 1e). Unlike the 1T-1C structure of FeRAM, in FeFET, the transistor serves both as the switching and storage element and hence significantly reduces the on-chip area. Moreover, FeFET offers a nondestructive readout (NDRO) since the transistor's drain current is also controlled by ferroelectric film's polarization direction and is also used to alter the surface conductivity of the semiconductor. Henceforth, the memory states logic "1" and "0". Further, the gate stack of the 1T FeFET structure is generally investigated in three device structures: MFS, MFIS, MFMIS structures (as discussed in section 4). For 1T FeFET devices, the MFIS structure is generally considered to prevent interdiffusion and interface reactions between the semiconductor and ferroelectric in contrast to the MFS structure. Also, there is more retention advantage as compared to the MFMIS structure, where the leakage current spreads to the floating metal and destroys the charge neutrality.

MFIS structure and operation of FeFET are shown in Figure 8, panels a and b, respectively.[198] For a p-type semiconductor

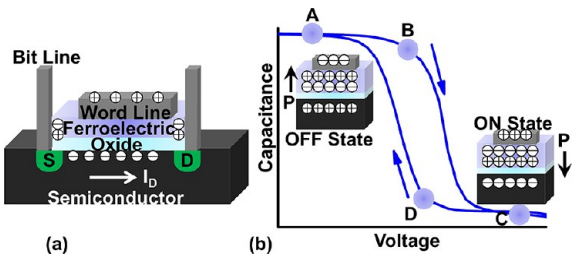

Figure 8. (a) MFIS structure of FeFET and (b) operation in the OFF and ON state.

substrate, when a negative voltage is applied to the gate, the ferroelectric film is polarized, and holes accumulate at the Si surface representing the OFF state (Point A) (as shown in the inset of Figure 8b). Because of the insulator buffer layer's presence, which creates a potential barrier, charges are difficult to inject into the ferroelectric thin film. When gate voltage is reduced to ∼0 V or, say, near flatband condition (Point B), the ferroelectric remains polarized near the remnant polarization state, and therefore few holes remain accumulated at the Si surface, signifying nonvolatile storage of device in the OFF state. Further, on application of a positive gate voltage, the ferroelectric gets polarized in the reverse direction, i.e., polarization switching occurs, which results in an inversion layer of electrons at the Si surface signifying the ON state (Point C) as shown in the inset of Figure 8b. Again when the gate voltage is reduced to ∼0 V (Point D), the ferroelectric remains polarized near the opposite remnant polarization state, and therefore few electrons remain at the Si surface, signifying nonvolatile storage of the device in the ON state.[157] The theoretical memory window (ΔW), i.e., flatband voltage shift during forward and reverse gate voltage sweep, and the ratio of voltage across MFIS capacitors, ferroelectric to the insulator (V_f/V_i) is related as

$$\Delta W = 2d_f E_c \tag{16a}$$

$$\Delta W_{exp} = 2d_f E_c - \Delta V_{ci} + \Delta V_{fatigue} \tag{16b}$$

$$\frac{V_f}{V_i} = \frac{d_f}{d_i}\frac{\varepsilon_i}{\varepsilon_f} \tag{17}$$

where V_f, d_f, ε_f, and V_i, d_i, ε_i are the voltage, thickness, relative permittivity of the ferroelectric, and buffer insulator layer, respectively. From our own experience in the field, the experimental ΔW may vary from the theoretical ΔW. For instance, the experimental memory window (ΔW_{exp}) may be lower than the theoretical value predicted due to charge injection (ΔV_{ci}) or higher than the theoretical value owing to ferroelectric fatigue ($\Delta V_{fatigue}$). Fatigue in the ferroelectric material generally enhances E_c but reduces the P_r of the ferroelectric. Therefore, we propose the above eq 16b to model ΔW_{exp}. However, the experimental variation parameters ΔV_{ci} and $\Delta V_{fatigue}$ are tough to obtain to pre-estimate the accurate experimental memory window. But these can give an approximation of the experimental memory window variation from the theoretical value.

5.3.1. Alternate High-κ Buffer/Insulator Layer for FeFET. In general, the buffer layer requirements are similar to the alternate high-κ oxide for CMOS-based integrated circuit technology. An ideal buffer material for FeFET device application should have the following exceptional properties:[48]

- Reasonably high dielectric constant (κ)
- Good interface with the semiconductor substrate
- Low leakage current density
- Good thermal stability
- Excellent diffusion barrier for ferroelectric

From 1994 onward, various buffer materials ranging from low dielectric constant ($SiO_2 \approx 3.9$) to high dielectric constant ($SrTiO_3 \approx 300$) materials have been extensively investigated for the MFIS structure of FeFET (summarized in Table 3). The motivation to use a buffer/insulator layer of high dielectric constant is that it allows the use of a physical thicker dielectric layer to achieve the same capacitance, eliminating the leakage current issues due to direct tunneling.[199] Lastly, it enhances the retention time of ferroelectric devices and continues the shrinking of device feature size for the next-technology node. However, merely replacing with alternate high-κ dielectrics[199−204] cannot easily solve the problem because of the inverse bandgap relation, especially the ferroelectric buffer layer compatibility, dielectric constant ratio, and many other properties as mentioned above. The dielectric constant must not be too large since it causes fundamental device physics impediments like fringing field-induced barrier lowering type short channel effects.[205]

5.3.2. Topical Advancement in FeFET. In 2002, Kim et al. demonstrated the metal/$SrBi_2Ta_2O_9$/SiN/Si, MFIS structure with 50 ns switching time, $>10^{11}$ fatigue cycles, but with a low

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Table 3. Recent Developments in the MFIS Structure of FeFET[a]

buffer layer	ε_i	ferroelectric/buffer gate stack	memory window	voltage sweep	retention	ref
$SrTiO_3$	~300	SBT(300 nm)/$SrTiO_3$(23 nm)	1.1 V	±7 V	8.6×10^4 s (1 day)	57
TiO_xN_y	N.A.	PZT(20 nm)/TiO_xN_y(6 nm)	1.05 V	±5 V	5×10^3 s (extrapolated 15 years)	69, 70
TiAlO	30	PZT(120 nm)/TiAlO(20 nm)	3.4 V	±10 V	N.A.	71
TiO_2	N.A.	PZT (300 nm)/TiO_2(60 nm)	2.0 V	±6 V	N.A.	72
La_2O_3	~25	PZT(160 nm)/La_2O_3(16 nm)	0.7 V	±8 V	N.A.	73
HfO_2	25	SBT(400 nm)/HfO_2(6 nm)	1.0 V	±5 V	2.6×10^6 s (30 days)	150
		BLT(200 nm)/HfO_2(10 nm)	1.32 V	±5 V	N.A.	66
$LaAlO_3$	21−25	SBT(210 nm)/$LaAlO_3$(25 nm)	3.0 V	±10 V	4.3×10^4 s	58
Ta_2O_5	22	PZT(700 nm)/Ta_2O_5(74 nm)	13 V	±15 V	N.A.	74
HfAlO	20	SBT(420 nm)/HfAlO(12 nm)	1.6 V	−6 to +8 V	2.9×10^6 s (33 days)	59
ZrO_2	20	SBT(210 nm)/ZrO_2(28 nm)	2.6 V	±10 V	N.A.	60
		BLT(300 nm)/ZrO_2(N.A)	2.0 V	±5 V	N.A.	67
Y_2O_3	15	PZT(290 nm)/Y_2O_3(11.8 nm)	1.5 V	±8 V	3×10^3 s	75
Dy_2O_3	14	PZT(250 nm)/Dy_2O_3(20 nm)	0.6 V	±6 V	1×10^4 s	76
PrO_2	12	SBT(400 nm)/PrO_2(20 nm)	0.3 V	±12 V	1×10^4 s	61
HfSiON	~11	SBT(300 nm)/HfSiON(2 nm)	0.8 V	±4 V	8.6×10^4 s (1 day)	62
Al_2O_3	~9	PZT(250 nm)/Al_2O_3(3.8 nm)	0.5 V	±5 V	N.A.	77
SiON	~7	SBT(400 nm)/SiON(20 nm)	0.3 V	−2 to+4 V	6×10^5 s (extrapolated 1 year)	63
		Si:HfO_2(9 nm)/SiON(1.2 nm)	0.8 V	±5 V	extrapolated 10 years	228
Si_3N_4	7	BLT(100 nm)/Si_3N_4(3 nm)	1.2 V	±5 V	~1×10^4 s	68
		PZT(120 nm)/Si_3N_4(2.5 nm)	3.6 V	±10 V	N.A.	78
		SBT(260 nm)/Si_3N_4(6 nm)	~2.0 V	±10 V	2.6×10^5 s	64
SiO_2	3.9	SBT(400 nm)/SiO_2(27 nm)	2.7 V	±6 V	3.0×10^3 s	65
		PZT(120 nm)/SiO_2(2.5 nm)	3.0 V	±10 V	N.A.	78

[a]Reports are ordered in accordance with a dielectric constant of the buffer layer.

retention time of ~2.6 ×10^5 s (3 days) only.[64] Afterward, numerous attempts have been made in past decades to investigate different buffer materials in the MFIS structure. However, no one could improve the electrical properties, especially the desired retention characteristics of MFIS devices. Recently, Hf-based oxides as an insulator buffer layer (e.g., HfO_2 and HfAlO) showed improved electrical properties. In 2004, Aizawa et al. showed Pt/SBT/HfO_2/Si, MFIS FeFET characteristics with a write pulse width of 20 ns and retention time of ~15.9 days at room temperature.[206] The breakthrough in retention characteristics was observed in 2008 when Tang et al. showed Pt/SBT/HfO_2/Si, MFIS devices with a retention of 8 h at room temperature, which remains distinguishable until 10 years extrapolation.[150] This astonishing device performance was due to the excellent quality HfO_2 buffer layer and optimum buffer layer thickness. Thus, with an acceptable switching speed (<20 ns), endurance (>10^{11}), retention (~10 years), and low operating voltage (<5 V), the state-of-the-art SBT/HfO_2-based FeFETs seemed an suitable solution for commercial nonvolatile memories compatible with 130 nm technology nodes. Zhang et al.[207] demonstrated the Pt/SBT/HfAlO/Si, MFIS structure of FeFET in NAND architecture that shows reliable characteristics, especially the high endurance of 10^9 cycles and long retention extrapolated 10 years, and access time ~10 μs. It is whispered that HfO_2-based dielectrics serve as the best buffer layer for MFIS FeFET applications. Table 3 highlights recent developments in the field of MFIS device structure of FeFETs, where memory window much greater than 1 V is possibly due to fatigue (as discussed earlier in Section 2.1). The dielectric constant of the buffer layer plays a vital role in MFIS devices' performance. However, overall device performance does not solely depend on the dielectric constant but also on the ferroelectric/buffer gate stack, leakage, thickness, and quality of oxide that govern the electrical properties such as memory window and retention of MFIS devices. As discussed earlier, increasing the buffer layer's dielectric constant to maintain a reasonable ferroelectric/buffer dielectric constant ratio can improve the MFIS device performance and is beneficial for scaling FeFETs for high-density storage applications. By means of this idea, recently TiO_2-based buffer layers, i.e., TiAlO and TiO_xN_y, have been investigated with a high dielectric constant PZT ferroelectric and proved to be an attractive candidate for a buffer layer in MFIS device applications. However, theoretically, the scalability of PZT/SBT approaches in terms of achievable memory window at very thin films is questionable for scaled-down devices below 20 nm feature sizes. Using eqs 16a and 17, to achieve a reasonable ΔW of 1 V, the typically required thickness for PZT/SBT-based FeRAM systems (with $E_c \approx 0.05$ MV/cm) must be ~100 nm. However, gradually, the PZT/SBT-based system may face reliability problems such as fatigue, which may increase the E_c (decrease P_r) and increase ΔW. The same behavior, i.e., increased E_c, (decreased P_r) is also observed on the scaling down the thickness of ferroelectric films,[25] where the critical thickness limit is also argued.[183−185,208] Thus, PZT/SBT approaches' scalability is a significant challenge that needs to be overcome for next-generation scaled FeRAM devices.[209] Alternatively, a new ferroelectric material system is required, which offers a reasonably high P_r, E_c, and reliability at scaled thicknesses.

5.3.3. TiO_xN_y Buffer Layer for FeFETs. Table 3 shows that TiO_xN_y films have attracted significant attention because of the high dielectric constant, which permits enough voltage across the PZT ferroelectric layer. Apart from this, TiO_xN_y films show improved physical and chemical properties compared to TiO_2 because of excellent diffusion barrier properties and hinders interfacial oxide formation.[69,70] It is also well-known that TiN is an exceptional metal buffer layer adopted by the CMOS industry. So, it is believed that TiO_xN_y possesses the oxide

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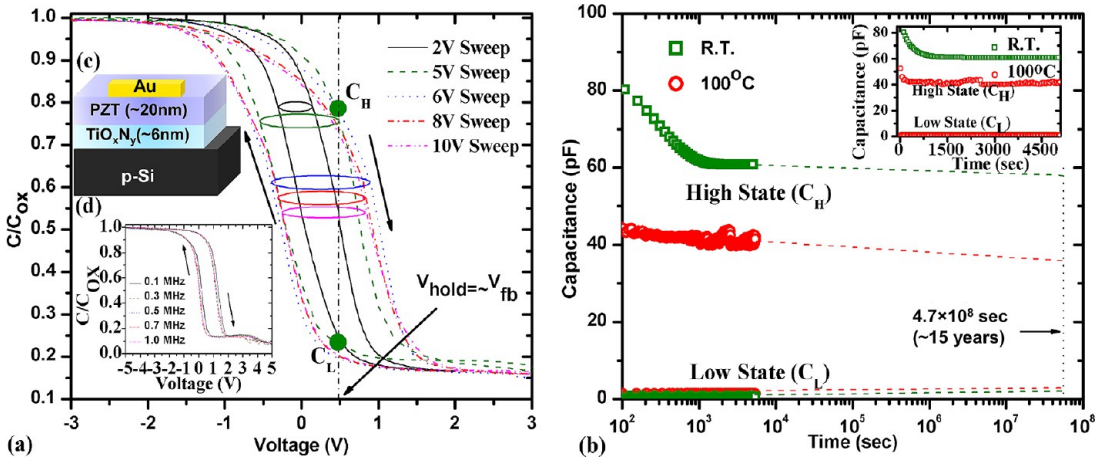

Figure 9. (a) Cyclic $C-V$ characteristics of Au/PZT (20 nm)/TiO_xN_y(6 nm)/Si, MFIS capacitors measured at 1 MHz frequency with variation in sweep voltage. The inset (c) shows Au/PZT (20 nm)/TiO_xN_y(6 nm)/Si, MFIS structure and inset (d) shows cyclic C−V characteristics of Au/PZT (20 nm)/TiO_xN_y(6 nm)/Si, MFIS capacitors measured with variation in frequency. (b) Capacitance−time characteristics of Au/PZT (20 nm)/TiO_xN_y(6 nm)/Si, MFIS capacitors at room temperature (R.T.) and 100 °C extrapolated on a log scale, and the inset shows the measured capacitance−time characteristics. Reproduced from ref 69. Copyright 2015 Elsevier.

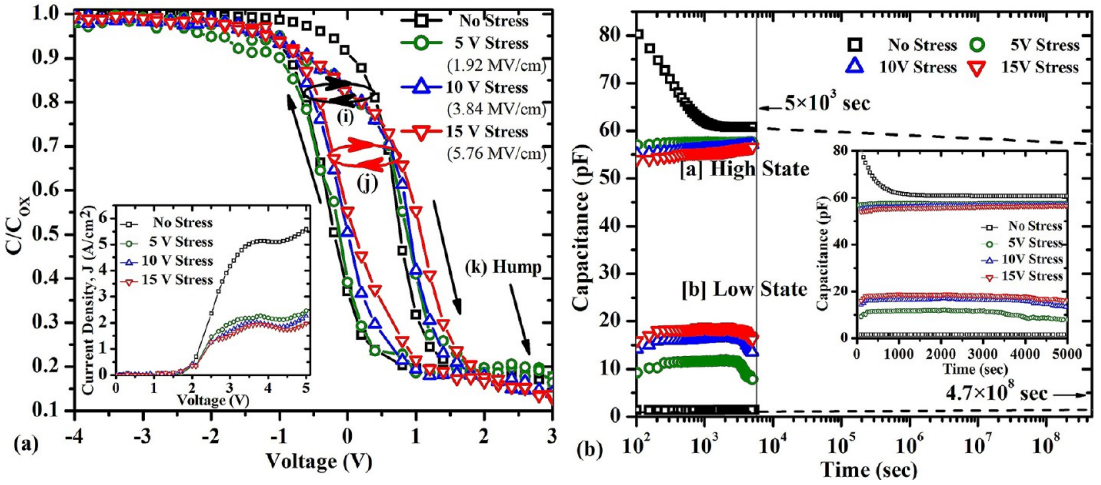

Figure 10. (a) Normalized $C-V$ characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS capacitors at different stress voltages. The inset shows leakage current density for Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS capacitors at different stress voltages, (b) Capacitance−time characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS capacitors at room temperature extrapolated on a log scale, and the inset shows the measured capacitance−time characteristics at different constant voltage stress. Reproduced from ref 70. Copyright 2014 AIP Publishing LLC.

properties of TiO_2 and the barrier properties of TiN. Thus, TiO_xN_y is expected as an exceptional buffer layer candidate for nonvolatile FeFET device applications.

Figure 9a shows the memory characteristics (cyclic $C-V$) of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structure, at 1 MHz with variation in sweep voltage.[69] Here, the flatband voltage (V_{FB}) shift measured from the cyclic dual sweep $C-V$ curves is called the memory window or hysteresis. The dual sweep signifies sweep from negative (accumulation) to positive (inversion) voltage (forward sweep), pursued by positive (inversion) to negative (accumulation) voltage sweep (reverse sweep). The memory window of ∼0.42 V was estimated at a sweep voltage of ±2 V. The memory window increases to ∼1.25 V at ±6 V sweep voltage. This substantial enhancement in the memory window with gate voltage variation is attributed to a rise in $PbZr_{0.52}Ti_{0.48}O_3$ polarization. However, the memory window reduces from 1.2 V @ ± 6 V to 1.10 V @ ± 10 V, possibly due to charge injection from the buffer layer at the high electric field, which is expected to oppose the ferroelectric polarization. Here, it is required to mention that, in our earlier report,[69] the theoretical memory window was calculated by assuming E_c of PZT ≈ 1/5 times the electric field across the ferroelectric layer (E_F), using eq 16. But recent investigations,[209] have shown that the maximum achievable memory window for a PZT-based system with a typical E_c of 50 kV/cm restricts its thickness to 100 nm to achieve a memory window of ∼1 V. Therefore, the experimental memory window of ∼1 V obtained in Au/PZT (20 nm)/TiO_xN_y(6 nm)/Si, MFIS capacitors may be due to increased E_c due to a reduction in PZT thickness or fatigue in the ferroelectric thin film. Fatigue is a common problem in ferroelectric thin films that increases the E_c (increases the memory window) and decreases the P_r (decreases the sensing margin) of a ferroelectric. However, the problem of fatigue may not be of concern unless the P_r becomes so small that the sensing circuit is unable to sense both the logic "1" and logic "0" memory states. The inset (c) of Figure 9a shows the MFIS structure of fabricated FeRAM devices, and inset (d) shows the cyclic $C-V$ characteristics of Au/PZT (20 nm)/TiO_xN_y(6 nm)/Si, MFIS

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structures measured with the variation of frequency for the validation of the memory window or hysteresis due to polarization. This rules out the possibility of hysteresis due to space charge rearrangement in the lattice, mobile ionic charges, and interfacial polarization. Figure 9b shows the retention behaviors of Au/PZT (20 nm)/TiO_xN_y(6 nm)/Si, MFIS structures acquired using a capacitance−time ($C-T$) method at 300 K. In this procedural exploration, a "'write'" voltage pulse of 100 ms duration and pulse height of +5 V program voltage for C_L (low capacitance state), −5 V (program voltage) for C_H (high capacitance state) were applied to MFIS devices. Here, the read voltage must be carefully considered close to the flatband voltage for the retention test. The capacitance maxima and minima must be significantly distinguishable at the same read voltage, as shown (with green circles) in Figure 9a. Ideally, if the $C-V$ curves show a sharp transition, then at a read voltage, C_H and C_L would be nearly equal to accumulation capacitance C_{acc} and inversion capacitance C_{inv}, respectively. Here, the high (C_H) and low (C_L) capacitance values are measured separately as a function of aging, keeping the bias voltage fixed close to flat band voltage (~0.5 V). Primarily, C_H decays exponentially and losses ~25% of high state capacitance value (i.e., $((C_i - C_f)/C_i) \times 100\% = ((80-60)/80) \times 100 = \sim 25\%$) within a few seconds followed by nearly linear decay with time as shown in the inset of Figure 9b, where C_i and C_f are the initial (t = 100 s) and final (t = 5000 s) measured capacitance during retention test. The C_H and C_L difference (i.e., $\Delta C = C_H - C_L$) is distinguishable for 1.5 h, even if extrapolated up to 15 years, suitable for next-generation FeFET devices. Since the actual integrated circuits operate at high temperatures, retention analysis at ~100 °C is performed.[210] A decrease in C_H was perceived on high-temperature aging, but the C_H and C_L values remain distinguishable for 1.5 h, even on 15 years extrapolation.[69]

In addition to thermal stress, electrical stress plays a vital role in real-world device applications. Thus, constant voltage stress (CVS) was applied to Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS devices, and electrical characteristics were recorded as shown in Figure 10. Here variation in V_{fb} of ~0.25 V was noticed under CVS up to 15 V, as shown in the inset (i, j) of Figure 10, attributed to the existence of a substantial number of TiO_xN_y/Si interface defects. The cyclic C−V curves at inset (i, j) of Figure 10a revealed memory window (ΔW) variation of ~0.05 V with the stress voltage increase from 0 to 15 V, attributed to trapping and detrapping at the TiO_xN_y/Si system.[211] Although intrinsic trapping sites in the TiO_xN_y/Si system are not strong, the charge numbers detrapped are enough to cause the slight V_{fb} shift. Therefore, the memory window reduction after CVS indicates reduced traps at the Si/TiO_xN_y system. Further, during reverse $C-V$ sweep, an exciting hump (inset (k)) also revealed strong detrapping of TiO_xN_y/Si system's intrinsic trap charges, which vanishes after CVS. It specifies that the TiO_xN_y/Si system's traps reduce with an increase in CVS. Further, the leakage characteristics (inset of Figure 10a) revealed a ~3.63 $\mu A/cm^2$ reduction in leakage current on the application of CVS of 15 V, confirming the decrease in intrinsic trapping sites in TiO_xN_y of the TiO_xN_y/Si system. The possible reason for the improvement in leakage characteristics with CVS may be the clogging of neutral defects that offer resistance to current conduction or result in deep traps such that electrons are no longer available for conduction.[212] The data retention characteristics of Au/PZT (20 nm)/TiO_xN_y(6 nm)/Si, MFIS devices with variation in CVS (Figure 10b) also confirmed 15 years data retention. It was observed that the slope of high state C_H becomes positive and low state and C_L becomes negative; i.e., the difference in high and low states (ΔC) increases under constant voltage stress, resulting in improvement of the retention time of MFIS capacitors.[70]

In summary, the MFIS structure using the TiON buffer layer are promising for FeFET applications. We observed a minimum write time of ~200 ns, endurance ~10^8 cycles, and retention of ~15 years in the same device. To increase the access time <200 ns, a smaller buffer layer down to 4 nm was also tried, but it resulted in low retention and bad characteristics. Therefore, the results presented here were optimum for the PZT/TiON gate stack. In the future, the TiON-based buffer layer can be investigated for high endurance SBT ferroelectrics, and complete nonvolatile memory characteristics demonstration including speed, retention, and endurance are required. It is also argued that the $C-V$ curves' nonlinearity can generate the impression of slowing down or even saturating retention loss if the inversion or accumulation region is reached. Therefore, for a more accurate retention test, the FeFETs can be fabricated and V_{fb} plotted with time. Nevertheless, a ferroelectric material system is required, which offers a reasonably high E_c. A solution to this problem is resolved by a HfO_2-based ferroelectric material system with a high E_c of ~1 MV/cm as discussed in the subsequent section.

5.3.4. Ferroelectric HfO_2-Based FeFETs. HfO_2 is adopted in the semiconductor industry as a gate dielectric due to its high dielectric constant (~17−43), wide band gap (~5.3−5.7 eV), and high band offset (>1 eV).[213] In 2007, Böscke et al. at Qimonda first discovered the ferroelectric properties in HfO_2-based thin films, followed by series of investigations by the Waser group in Aachen, NaMLab, Fraunhofer CNT, and a first report published in 2011.[88] The unanticipated ferroelectric properties in HfO_2 are believed to be due to the formation of the polar orthorhombic (oIII) $Pca2_1$ phase, which is not found in the general HfO_2 phase diagram.[44,214−216] The capability to engineer ferroelectricity in the CMOS industry compatible HfO_2 and doped HfO_2 materials (Figure 11),[22] which show ferroelectricity at <10 nm thickness,[217] has attracted the scientific community to permit its use as a gate dielectric in FeFET devices. Notably, because of high E_c (~1 MV/cm) in

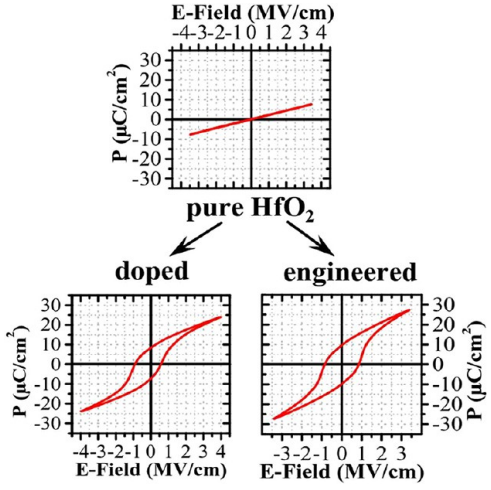

Figure 11. Paraelectric characteristics of pure HfO_2 $P-E$ characteristics converted to ferroelectric $P-E$ hysteresis in Si-doped HfO_2 (3.6 mol % Si in HfO_2) or engineered HfO_2 (e.g., TiN/HfO_2/TiN). Reproduced from ref 22. Copyright 2015 The Electrochemical Society.

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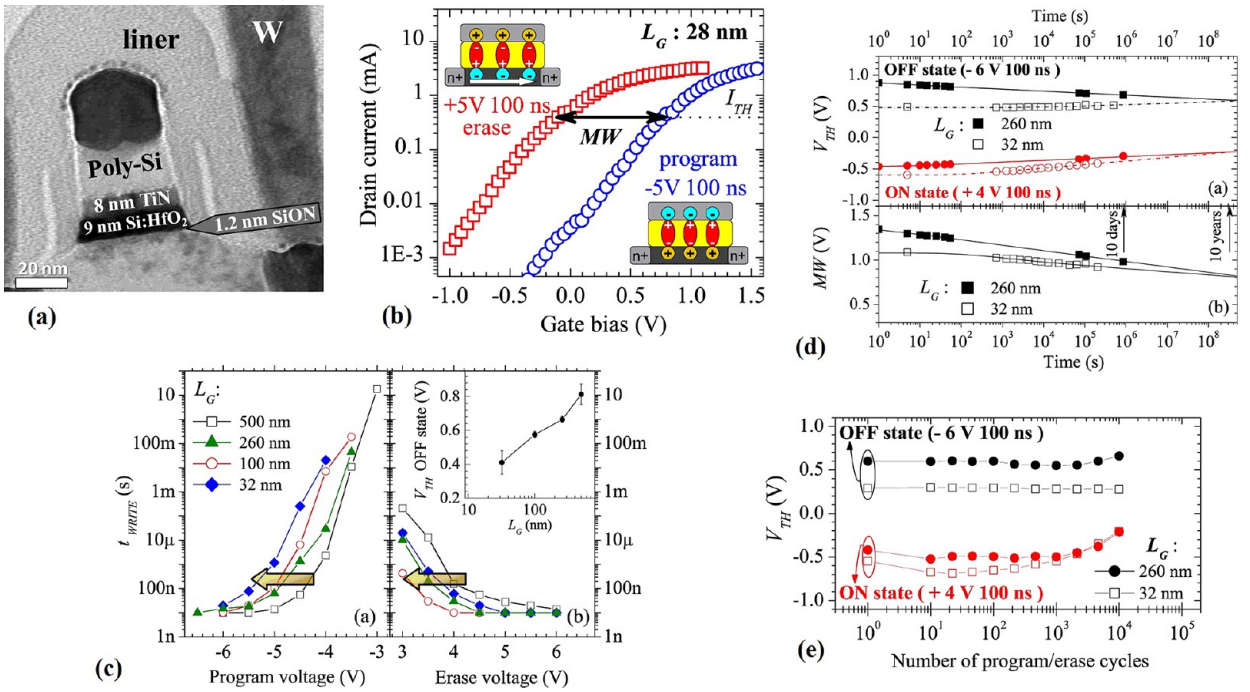

Figure 12. (a) TEM cross-section image and (b) I_D-V_G memory characteristics of Si:HfO_2 (32 nm)-based MFIS FeFET devices. The effect of scaling on (c) switching speed, (d) retention characteristics, and (e) endurance characteristics of 32 nm Si:HfO_2-based MFIS FeFET device. Reproduced from ref 228. Copyright 2014 IEEE.

HfO_2-based ferroelectrics that directly scale, the minimum adaptable theoretical ferroelectric thickness to ~5 nm using eq 16 achieves a memory window of ~1 V. As well, the nonvolatile retention is quite easily achieved as compared to PZT/SBT-based systems.[209] For instance, two major mechanisms are proposed to be responsible for retention loss that dominates in different time regimes: (i) initial fast decay stage: depolarization field (E_{dep}) responsible for the initial fast decay; (ii) later slow decay stage: gate leakage and trapping responsible for later slow decay in longer time. From the $P-E$ loop of a ferroelectric layer, if $E_{dep} > E_c$, then E_{dep} can cause significant retention loss; if $E_{dep} \leq E_c$, then slight polarization can flip. Therefore, the E_{dep}/E_c ratio determines the polarization decay rate during the early stage. The E_c of HfO_2-based ferroelectrics is much larger than SBT/PZT counterparts, which points to a smaller E_{dep}/E_c ratio and therefore low retention loss during the initial fast decay stage. After the initial fast decay stage due to E_{dep}, ferroelectric polarization saturates down to a value in proportion to E_c in the MFM structure.[218,219] Further, the P_r in the ferroelectric layer induces charge exchange from gate or Si, based on polarization direction[49] and causes charge trapping that reduces the polarization effect. The charge trapping based decay is slow due to a longer time constant (as compared to decay due to E_{dep}), and the memory window degradation is in proportion to trap density N_t.[218,220,221] Thus, the trap density in HfO_2-based ferroelectrics (~3×10^{11} cm^{-2}),[95] which is significantly lower than PZT/SBT counterparts (~4×10^{12} to ~5×10^{13} cm^{-2}),[75,218,222,223] is also a cause of better retention in HfO_2 FeFETs. Additionally, it is believed that a lower dielectric constant of HfO_2-based ferroelectric (as compared to SBT/PZT) reduces the fringing field at the gate edge for scaled FeFETs that may be beneficial for long retention memory devices.[224]

The orthorhombic (oIII) phase in HfO_2 is observed in (i) engineered HfO_2: encapsulating between TiN electrodes, small grain size;[45] (ii) doped HfO_2: with Si/Al/Y/Gd/Zr/La/Sr/N dopants[22,51,87−93,225] and the $P-E$ characteristics for both cases are shown in Figure 11.[7] The ab initio simulations found that the stability of this oIII-phase in HfO_2 lies in a narrow energy range of generally assumed polymorphism.[226] On the basis of various experimental and simulations results, it is established that the oIII-phase is formed at essential process parameters: (i) small average grain size (D_{ave}); (ii) large tensile stress along the c-axis of the tetragonal (t)-phase; (iii) capping layer to avoid monoclinic (m)-phase formation due to crystallization annealing and optimization of the ozone dose; (iv) suitable t-phase grains orientation compatible with the polar direction and asymmetric strain before phase transition to the oIII phase; (v) dopants (e.g., Si/Al/Y/Gd/Zr/La/Sr) with suitable doping concentrations, that may change surface energy and internal stress state.[44,227] After considerable research efforts, ferroelectric Si:HfO_2 with 4.4 mol % Si, is reported with best results and found compatible with 28 nm CMOS technology node.[228] Figure 12a shows the cross-section TEM image of poly-Si/TiN(8 nm)/Si:HfO_2(9 nm)/SiON (1.2 nm)/Si, MFIS structure of FeFET with 32 nm gate length fabricated using 28 nm CMOS technology. The electrical characteristics shown in Figure 12 were reported by taking averaged response from multiple memory cells, i.e., containing a parallel arrangement of many transistors. Figure 12b shows the I_D-V_G memory characteristics of poly-Si/TiN (8 nm)/Si:HfO_2 (9 nm)/SiON (1.2 nm)/Si, MFIS structure of FeFET programmed and erased by a 100 ns pulse of −5 V and +5 V, respectively, showing a memory window of 0.8 V. Moreover, the devices exhibited a nonzero memory window at 10 ns switching speed (Figure 12c), and data retention measured for 10 days and extrapolated to 10 years (Figure 12d) along with a switching endurance of 10^4 cycles (Figure 12e).

Apart from undoped and doped HfO_2 ferroelectrics, the $Hf_xZr_{1-x}O_2$[229,230] and HfO_2/ZrO_2 nanolaminates[231] are also a

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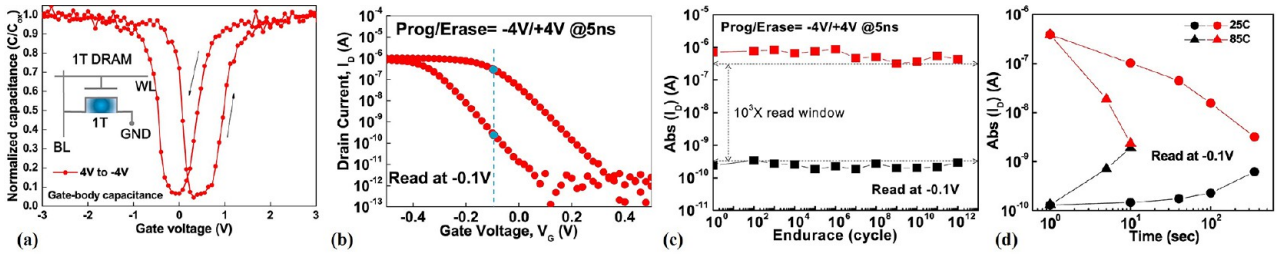

Figure 13. (a) Measured $C-V$ characteristics (inset shows the schematic plot of 1T- DRAM), (b) $I_D - V_G$ after −4 V/+4 V@5 ns P/E write pulse and read @ −0.1 V, (c) endurance characteristics, and (d) retention characteristics of TaN/ZrHfO (30 nm)/ SiO_2(3 nm)/Si, MFIS structure. Reproduced from ref 233. Copyright 2014 IEEE.

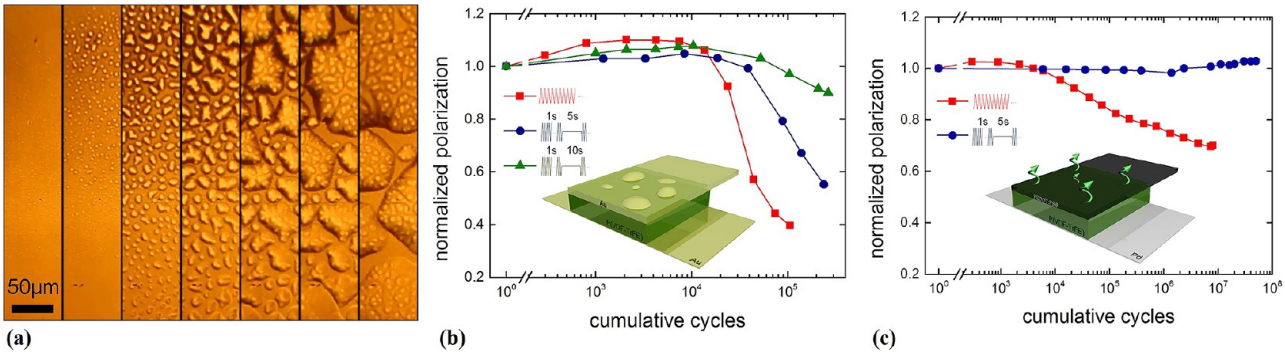

Figure 14. (a) Optical micrographs of the Au top electrode taken on the same spot in the Au/P(VDF-TrFE)(500 nm)/Au system during fatigue measurement. Endurance characteristics of P(VDF-TrFE) capacitors with (b) Au top electrodes and (c) PEDOT: PSS top electrodes. Here, normalized polarization is shown in relation to number of cycles of 40 V/100 Hz bipolar triangular pulse [red curve] and when the continuous cycling was interrupted every second with 5 s [blue curve] and 10 s [green curve] waiting time.[85]

potential candidate for CMOS-compatible ferroelectric materials. Initially, ferroelectricity in $Hf_xZr_{1-x}O_2$ was reported by Muller et al. with P_r of 16 $\mu C/cm^2$ and a high E_c of 1 MV/cm.[229] It was observed that $Hf_{0.5}Zr_{0.5}O_2$ composition is best for ferroelectric behavior.[232] Thus, $Hf_{0.5}Zr_{0.5}O_2$ has become a widely used CMOS-compatible ferroelectric material. Cheng et al. recently demonstrated a TaN/$Zr_{0.5}Hf_{0.5}O_2$ (30 nm)/SiO_2 (3 nm)/Si, MFIS structure.[233] The ferroelectric hysteresis loop (flat band voltage shift) was reported at +4 V to −4 V sweep, as shown in Figure 13a. Additionally, the devices operated at a high speed of 5 ns (Figure 13b) and endured up to 10^{12} switching cycles (Figure 13c), appealing to the suitability of the device to replace traditional DRAM in the current memory hierarchy. The high endurance of 10^{12} cycles for $Hf_{0.5}Zr_{0.5}O_2$ significantly removes the bottleneck of HfO_2-based 1T-FeFETs and also endorsed the existing commercial viability. However an endurance test up to 10^{15} cycles using a faster pulse generator still needs to be explored to meet the full potential and replace existing 1T-1C DRAM. However, the retention time less than 10^3 s of TaN/ZrHfO (30 nm)/ SiO_2 (3 nm)/Si, MFIS FeFET is acceptable for DRAM but not for next-generation NVRAM. On the other hand, for HfO_2/ZrO_2 nanolaminates, Weeks et al. observed that the orthorhombic phase is sensitive to deposition temperature and independent of layer thickness. However, it would be interesting to see the higher performance of HfO_2/ZrO_2 nanolaminates' integrated FeFETs, especially the endurance and retention characteristics in the near future.[231]

There is a common understanding among various researchers that the retention of $Hf_{0.5}Zr_{0.5}O_2$-based FeFET devices can be achieved by improving the buffer layer and buffer layer/semiconductor interface in MFIS systems. In summary, CMOS-compatible and green HfO_2 based ferroelectrics are promising for next-generation nonvolatile FeFETs. Although, there is a trade-off between retention and endurance. Therefore, on the basis of the device characteristics, it can be predicted to fit the memory hierarchy's specific level, for example, high endurance and medium retention for DRAM and medium endurance and long retention for NVM applications. In the future, it is expected to see FeFETs compete with state-of-the-art planar SSDs ~15 nm technology, $4F^2$ with three bits per cell, or 3D NAND with 128 stacked layers of storage, although presently the concept of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$-based 1T-type FeFETs seems a good alternate for DRAM,[233] as it can provide an area advantage, i.e., one element (1T) instead of two elements (1T-1C). However, the possibility of 3D integration and endurance needs to be confirmed up to 10^{15} cycles. Alternatively, FeFET devices with a fast read/write access time of 100 ns, endurance ~10^5 cycles, retention >10 years, cell size 6−10F^2, and energy <1 fJ/bit are competitive for NVM applications.[11]

However, for FeFETs to be a universal memory, achieving 10 years of data retention and ~10^{15} endurance cycles in the same cell remains an ambitious research topic. We expect that optimizing the ferroelectric material with different dopants, electrode materials, or processing conditions may push the endurance to the demanding 10^{15} cycles in 1T-FeFET. Also, high retention without compromising the endurance may be achieved with the relatively thick high-κ buffer layer. Of course, there is a trade-off between endurance, retention, and device speed, which may be optimized with the FeFET device structure's design constraints for a particular application. Correspondingly, optimum memory architecture and sensing schemes are also needed.

5.3.5. Organic PVDF-Based Flexible FeFETs. In 2004, Schroeder et al. fabricated and demonstrated the first organic

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Table 4. FeFETs with Two-Dimensional Channel Materials (2D FeFET)

structure	memory window (V) at (@) sweep voltage (V)	retention time (s)	endurance (cycles)	I_{on}/I_{off}	write/erase speed	ref
Au/P(VDF-TrFE)/MoS_2	15 V@ ± 20 V	60		~10^7	1 s	319
Al/P(VDF-TrFE)/$MoSe_2$	24 V@ ± 40 V	>2 × 10^3	10^4	~10^3−10^5	50 μs/2 ms	320
Au/P(VDF-TrFE)/In_2O_3−NW	33 V@ ± 50 V	5 × 10^4	400	>10^6	1 s	321
Al/P(VDF-TrFE)/ZnO	10 V@ ± 20 V	10^4		~10^3	>50 ms/>50 ms	322
Al/P(VDF-TrFE)/pentacene		10^4		40	>50 ms/ > 50 ms	322
Al/P(VDF-TrFE)/TIPS-PEN		>5 × 10^4		>10^3		323
Au/P(VDF-TrFE)/MEH-PPV		>6 × 10^5	10^3	>10^4	~0.3−0.5 ms	86
MXD6/pentacene	~20 V@ ± 20 V	~20% loss after 3 h		200		234

memory FeFET using nylon poly(m-xylylene adipamide) (MXD6) as a ferroelectric and pentacene as a semiconductor material. The memory window of 20 V @ ± 20 V sweep and retention loss of ~20% was observed after 3 h.[234] In 2005, Naber et al. reported a high-performance Au/P(VDF-TrFE)/MEH-PPV organic FeFETs, with programming time (>0.1 ms), retention (10^4 s), and endurance (10^3 cycles).[86] For organic ferroelectric memories, apart from uniform ferroelectric thin films (as discussed in section 2.3), fatigue is also a significant challenge because the spontaneous polarization is reduced to ~50% in fewer than 10^6 cycles. Endurance is reported to be dependent on input pulse amplitude and frequency.[235] In 2011, Khan et al. observed that poly(3,4-ethylenedioxythiophene): poly(styrene sulfonic acid) [PEDOT:PSS] electrodes are superior as compared to metal (Pt) electrodes; especially in terms of improved endurance >10^8 cycles. Here, the enhanced endurance with PEDOT:PSS electrodes was attributed to a reduction of charge injection in P(VDF-TrFE), which might be due to less carrier concentration of the polymer compared to metal electrodes, resulting in a lower trap charge density.[236] There was no well-established evidence for lower trap charges in the PEDOT:PSS/P(VDF-TrFE)/PEDOT:PSS system. Furthermore, Li et al. also observed that PVDF-based capacitors are generally shorted with metal electrodes and hence reported PEDOT:PSS electrodes to be the possible solution.[106]

Recently, Zhao et al. presented that the top electrode's delamination is a reason for fatigue, as shown by the optical micrographs of Figure 14a. It was proposed that the accumulation of gases induced during the P(VDF-TrFE) phase decomposition, expelled from beneath the top electrode, is the origin of fatigue. Figure 14b shows the endurance characteristics of Au/P(VDF-TrFE)/Au, capacitors with a variation of input 40 V/100 Hz bipolar triangular pulse cycles [red curve]. After that when the continuous cycling was interrupted with 5 s [blue curve] and 10 s [Green curve] waiting time as shown in the inset of Figure 14b. It was noticed that during switching, gas generated due to P(VDF-TrFE) phase decomposition diffuses out of the capacitor during the delay, does not accumulate at the interface, and results in improved endurance. Figure 14c shows the same endurance test on PEDOT:PSS/P(VDF-TrFE)/Au, capacitors with variation in input pulse cycles. Here, PEDOT:PSS organic electrodes with a higher gas diffusion coefficient than Au, were used and significantly improved endurance characteristics were observed. Fatigue occurs after 10^4 cycles for continuous bipolar triangular pulsing (40 V/100 Hz) and microvoids on PEDOT−PSS's surface. However, with a delay of 5 s, the fatigue-free capacitor was realized with endurance >10^8 cycles, as shown in Figure 14c [blue curve]. Moreover, Au electrodes on top of PEDOT:PSS were also investigated, and the observed endurance was similar to Au/P(VDF-TrFE)/Au systems. Recently, Kim et al. demonstrated a fully transparent and flexible graphene/P(VDF-TrFE)/poly[bis(4-phenyl)(2,4,6-trimethylphenyl)-amine] [PTAA], 1T-MFS FeFET, with ±60 V, 50 ms switching pulse and much low endurance of ~125 cycles.[82] Likewise, Kim et al. and Sugano et al. reported the P(VDF-TrFE)-based FeFETs on a flexible substrate that showed minimal variation in electrical properties when subjected to bending stress.[237,238] Thin Film Electronics ASA, Norway, carries out the commercial activity in this field, using organic ferroelectric thin films printed electronics.[239,240]

In summary, the solution to uniform PVDF thin films is (i) control over moisture contents during the deposition of PVDF, (ii) high-temperature processing, (iii) use of copolymers: P(VDF-TrFE), PVDF−PMMA, and PVDF−GO. Notably, for device applications, PEDOT:PSS electrodes are desired for acceptable endurance characteristics (>10^8 cycles). The organic materials have limited thermal stability. Therefore, these cannot be integrated into CMOS technology but are suitable for low-cost, flexible/printed electronics. All organic PVDF-based FeFETs are still under investigation, which shows performance comparable to their inorganic counterparts.

5.3.6. FeFETs with Two-Dimensional Channel Materials (2D FeFET). The two-dimensional (2D) materials, e.g., graphene, transition metal dichalcogenides (TMDs), silicene, and phosphorene[241] have attracted the scientific community's wide attention because of the potential to extend the integrated circuit technology to sub-nanometer scales. Among these, TMDs have immense potential to be the semiconductor component in next-generation FETs because of their bandgap in the range of 1−2 eV and atomically thin layers due to weak van der Waals interactions amid corresponding bulk material layers that have shown minimal surface roughness and low density of dangling bonds.[242,243] Recent progress in 2D materials suggests that they might be one pathway for next-generation nanoelectronics devices.[244−247]

There is plenty of space for research and development on integrating two-dimensional channel materials along with ferroelectric materials (gate dielectric) and low resistance contacts, particularly in low-power flexible electronic applications. In this regard, a few reports are summarized in Table 4 to give a glimpse of the present status of integrating ferroelectric materials along with two-dimensional materials. Here, it is evident from Table 4 that the performance of 2D FeFETs is still lagging behind the inorganic counterparts (shown earlier in Table 3), mainly regarding reliability characteristics like endurance and retention. It would be interesting to see how the advancements in 2D TMDs bring high-performance 2D FeFETs for state-of-the-art nanoelectronics in the near future. In addition to device-related challenges, the fabrication process of

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2D TMDs needs to be significantly improved in the future, especially, the large-area uniform growth of 2D, chemical purity, stoichiometry, thickness (number of layers), yield, environmental stability in the desired semiconducting phase for next-generation nanoelectronics.

5.4. Ferroelectric Tunnel Junctions (FTJ). In 1971, Esaki et al. proposed the initial concept of ferroelectric tunnel junctions (FTJ).[248] FTJ is a trilayer metal-ferroelectric-metal (MFM) structure that consists of an ultrathin ferroelectric layer sandwiched among two conductive electrodes (Figure 15),

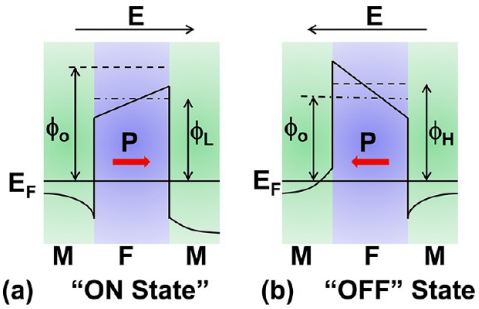

Figure 15. Ferroelectric tunnel junctions for cross-point architecture NVM (a) ON state, and (b) OFF state.[249]

where E_F is the Fermi level of top electrodes.[249] When no electric field is applied, the ferroelectric is unpolarized, and a square potential energy barrier of height φ_o (dashed line) exists between the electrons in the two metal electrodes. According to basic quantum mechanics, the wave function of electron leaks through a potential barrier provided the barrier is adequately thin and low. The tunnel transmittance depends exponentially on the square root of the barrier height.[250] When a negative voltage (−V) is applied to top (right) electrode, the ferroelectric polarizes, and the height of the potential energy barrier decreases to φ_L (Figure 15a). It reduces the tunneling resistance and increases the tunneling current to give the "ON" state.

Similarly, the application of a positive voltage (+V) to the top (right) electrode (Figure 15b) results in ferroelectric polarization in the opposite direction, and the potential energy barrier height increases to φ_H. It increases the tunneling resistance and decreases the tunneling current to give the "OFF" state. This phenomenon in which the ferroelectric layer's tunneling resistance varies based on external electric field application is called the tunnel electroresistance (TER) effect. The resistances ratio in the OFF and ON states, i.e., R_{OFF}/R_{ON} (resistance ratio), are defined as the TER effect's efficiency (η). Therefore, the devices that operate on the TER principle are also called ferroresistive memories. Alternatively, the tunnel electroresistance (TER) ratio $= \frac{J_{ON} - J_{OFF}}{J_{OFF}} \times 100\%$ and $\frac{J_{ON}}{J_{OFF}}$ ratio for FTJs has been significantly improved in the past decade. A significant improvement has been achieved in replacing one of the metal electrodes with a heavily doped semiconductor understood due to electrical modulation in height and width of a tunnel barrier in the MFS structure. Thus, apart from the MFM structure, the concept of FTJs is also feasible to be applied for the MFS structure, as shown in Figure 16.[251] When a positive voltage is applied to metal (Figure 16a), the ferroelectric polarization directs to the semiconductor and results in electrons' accumulation on the semiconductor surface. The accumulated semiconductor surface behaves like a metal layer, and the screening effect acts analogous to that in the MFM structure of

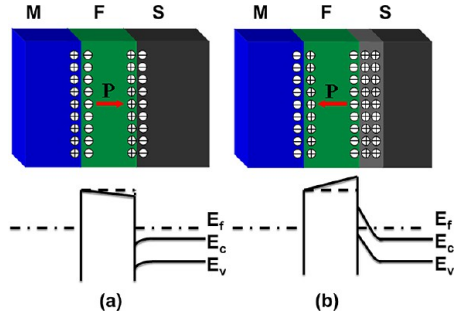

Figure 16. Ferroelectric tunnel junctions using the MFS structure and corresponding band diagram for the (a) low resistance state and (b) high resistance state. Here, the semiconductor electrode is preferred for an enhanced TER effect due to modulation of tunneling barrier height and width.[251]

FTJs. However, this is partial screening generally, and a depolarization field E_{dep} that opposes the polarization develops in the ferroelectric barrier.[252] Therefore, E_{dep} reduces the barrier height resulting in higher tunneling transmittance[252−254] (i.e., low resistance, high current, "ON" state). As shown in Figure 16b, when a negative voltage is applied to metal, the ferroelectric polarization is reversed and points to the metal. The depletion of electrons on the semiconductor surface results in immobile ionized donors (holes).[129,255] In the depleted state, the immobile screening charges spread over the space charge region and are defined by the doping profile.[256] The preliminary screening again produces E_{dep}, although this time, it enhances the barrier height.[252−254] Thus, the electron tunneling has to face an additional barrier in the depleted space charge region due to induced band bending.[256] This extra barrier results in significantly reduced tunneling transmittance (i.e., high resistance, low current, "OFF" state).

Furthermore, FTJs offer the advantage of being a nonvolatile, nondestructive readout and high density due to the MFM structure in the cross-point (X-point) architecture, and low-voltage operation. The primary challenge for FTJs' commercial potential is room temperature polarization switching and stability at ultrathin thicknesses.[185,257] A common argument is that ferroelectricity ceases beyond a critical thickness due to depolarization fields or finite-size effects.[208] It is also challenging to get $P-E$ characteristics at ultralow thicknesses (<10 nm) due to higher leakage currents. Moreover, ferroelectrics are also piezoelectric in nature, and therefore reverse piezoelectric effects can cause modification in ferroelectric thickness. However, this usually occurs at very high voltages,[253] whereas FTJs generally operate at low voltages, preventing the ferroelectric state's destabilization. In the past decade, renewed interest has emerged due to significant advances in deposition techniques, better control over the ferroelectricity at ultralow thicknesses, and advanced nanoscopic characterization techniques.

5.4.1. Requirements and Challenges for the Development of FTJs. The benchmarks that are necessary for high-performance FTJs to be a potential contender for future high-density nonvolatile memories are listed as follows:

- High TER ratio (higher the better, up to 10^7 is reported).
- Scaling (<200 nm), typically cell size <$4F^2$, competes with high-density storage memory competitors, where F is the feature size.
- High data retention (>10 years) for long-term storage.
- High endurance (>10^8 cycles).
- Low write energy (<100 fJ/bit).

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Table 5. Recent Experimental Reports on FTJs

T.E.	ferroelectric	B.E.	substrate	$\eta = R_{OFF}/R_{ON}$	scalability	retention (s)	endurance (cycles)	ref
Ag	$PbZr_{0.52}Ti_{0.48}O_3$ (4 nm)	$La_{0.8}Sr_{0.2}MnO_3$	STO	~10^7	0.6 μm			324
Pt	$BaTiO_3$ (3.4 nm)	$SrTiO_3$:Nb		>10^4	30 μm	10^5 (extrp. 10 years)	>10^3	251
Co	T-$BiFeO_3$(4.5 nm)	$Ca_{0.96}Ce_{0.04}MnO_3$	$YAlO_3$	>10^4	0.18 μm	68 h	>2000	269
MoS_2	$BaTiO_3$(2.4−4.8 nm)	$SrRuO_3$	STO	~10^4		48 h		325
Cu	$PbZr_{0.2}Ti_{0.8}O_3$(9 nm)	$La_{0.7}Sr_{0.3}MnO_3$	$SrTiO_3$	>1500	0.22 μm	6000		266
Co	$BaTiO_3$ (1.6 nm)	$La_{0.7}Sr_{0.3}MnO_3$	$NdGaO_3$	1000	5 μm	100		326
Co	$BaTiO_3$ (2 nm)	$La_{0.7}Sr_{0.3}MnO_3$	$NdGaO_3$	>300	0.35 μm			263
Co	$PbZr_{0.2}Ti_{0.8}O_3$ (1.2−1.6 nm)	$La_{0.7}Sr_{0.3}MnO_3$	$SrTiO_3$	300	0.22 μm			327
Cr	$BaTiO_3$(3.2 nm)	$La_{0.7}Sr_{0.3}MnO_3$	STO/Si	212	105 nm^2		10^4	279
STO	BTO (2.4 nm)	SRO	STO	~125	75 nm			280
Pt	$BaTiO_3$ (2 nm)	$La_{0.7}Sr_{0.3}MnO_3$	STO/Si	>100	5 μm	10^5 (extrp. 10 years)	>10^5	282
Co	$BaTiO_3$ (2 nm)	$La_{0.7}Sr_{0.3}MnO_3$	$NdGaO_3$	>100	0.05 nm		900	328
Ag	$BaTiO_3$ (3 nm)	$SrRuO_3$	$DyScO_3$	>100	20 nm			267
$La_{0.5}Ca_{0.5}MnO_3$	$BaTiO_3$ (3 nm)	$La_{0.7}Sr_{0.3}MnO_3$	$SrTiO_3$	100 @5K	15 μm			273
Cr	$BaTiO_3$ (3 nm)	Pt	MgO	~30	0.80 μm			268
Pt	$Hf_{0.5}Zr_{0.5}O_2$ (~2.8 nm)	Pt	N.A.	~20	300 μm			329
Pt	$Hf_{0.5}Zr_{0.5}O_2$ (~2.8 nm)	TiN	Si	~15	300 μm	>8 h	>10^3	330
W	PVDF (8 nm)	Au	Si	>10	0.36 μm			277
Pt/$La_{0.67}Sr_{0.33}MnO_3$/ $La_{0.5}Sr_{0.5}MnO_3$	$BaTiO_3$ (0.8 nm) @ 10K	$SrTiO_3$:Nb		~4	5 μm	6000	500	276
Ag	$BaTiO_3$	$SrTiO_3$:Nb		200−3000	70 μm (50 nm)	>10^4	>10^8	278

- Thermal stability (>200−400 °C) compatible with the back-end-of-line (BEOL) CMOS processing
- Compatibility with high-volume manufacturing (HVM) CMOS technology
- Multibit storage by incorporating a ferroelectric tunnel barrier into the traditional magnetic tunnel junctions (MTJ) to develop two-bit (four levels) memory devices.

Although FTJs are in a nascent phase, many standard investigations and tests are desired to benchmark their nonvolatile memory potential. Epitaxy high-quality, single-crystal films are only reported to give high performance to date. High-quality CMOS-compatible ultrathin ferroelectric films are required to develop and commercialize high-performance FTJs.

5.4.2. Advancement in FTJs. In 2003, Contreras et al. reported resistive switching in the MFM structure at room temperature.[258] However, the initial experimental demonstrations of TER came in 2009.[259−261] Garcia et al. reported ferroelectricity in highly strained $BaTiO_3$ films down to 1 nm thickness using (peak force microscopy) PFM at room temperature (RT). The efficiency (η) of ~100 was reported, which corresponds to a giant TER effect of 10 000% at RT, high speed (10 ns), low operating voltage (3 V), and read voltage of 100 mV. Moreover, low program energy ~10 fJ/bit was shown in scaled 50 nm devices, which is better than the typical nJ to pJ range of existing flash and emerging memories.[249,259] Gruverman et al. also reported ultrathin $BaTiO_3$ films for FTJs with additional local $I-V$ curves fitted with direct tunneling models.[261] Maksymovych et al. showed the local DC piezoresponse of ferroelectric ($PbZr_{0.2}Ti_{0.8}O_3$ (30 nm)) using a conductive atomic force microscope (AFM) tip. From the measured $I-V$ curves, a considerable current change was attributed to the ferroelectric switching.[260] Furthermore, Garcia et al. commented that for such thick ferroelectric film (30 nm), Fowler−Nordheim (F−N) tunneling comprises electron transport via hopping or other mechanisms in the ferroelectric thin films. However, the Schottky barrier resistance appears predominant.[262] In 2010, Pantel et al. reported three possible transport mechanisms that govern the current flow in ferroelectric ultrathin films of FTJs. (i) Direct tunneling dominates at low voltage (low TER); (ii) F−N tunneling is prominent at high voltage; and (iii) thermionic emission at higher barrier thicknesses (high TER).[254] Likewise, Chanthbouala et al.[263] reported Co/$BaTiO_3$/$La_{0.7}Sr_{0.3}MnO_3$, ferroelectric memristor, whose resistance varied by application of 20 ns voltage pulse. This kind of memristive behavior emulates synapses plasticity and has potential in neuromorphic architecture.[264] In 2011, Gao et al.[265] revealed the atomic resolution role of defects in ferroelectric switching using in situ transmission electron microscopy (TEM). It attributes that the intrinsic electric field present at the interface of the metal/ferroelectric system establishes the nucleation sites, the ferroelectric domains growth, mobility, and the orientation of the domain walls. Simultaneously, a feeble pinning force is exerted on the motion of domain wall due to dislocations. Pantel et al. reported Cu/$PbZr_{0.2}Ti_{0.8}O_3$ (9 nm)/$La_{0.7}Sr_{0.3}MnO_3$, MFM FTJs with an efficiency (η) of 1500, high ON current of 10 A/cm^2, and thermionic emission as a dominant transport mechanism.[266] In 2012, Gao et al. demonstrated Au−Co/$BaTiO_3$(2 nm)/$La_{0.7}Sr_{0.3}MnO_3$, MFM FTJs via local PFM characterizations, η of 15 to 220, speed 100 μs to 10 ns, scalability with 20 nm wide FTJs, and write energy ~100 fJ/bit. The endurance ~900 cycles were only demonstrated because of tip drift and loss of electrical contact.[267] A breakthrough in the TER effect was reported in 2013 by Wen et al. where a Pt/$BaTiO_3$/Nb:$SrTiO_3$, MFS

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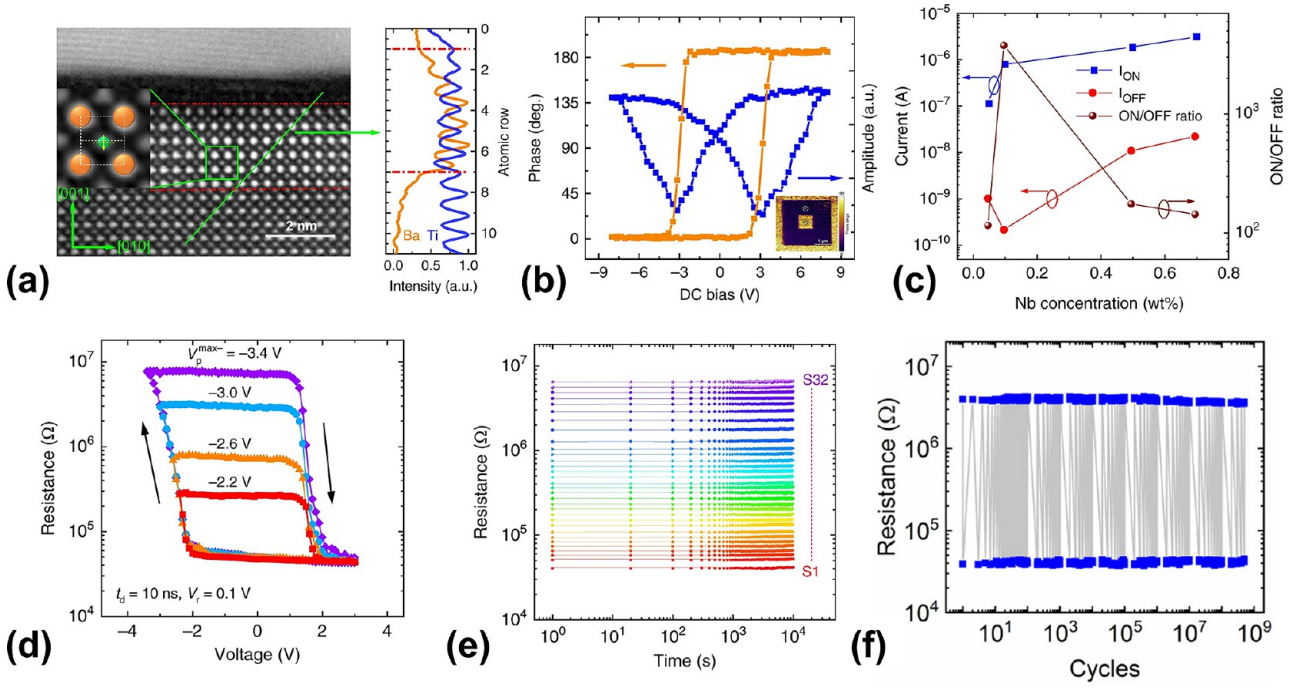

Figure 17. Ag/$BaTiO_3$/Nb:$SrTiO_3$ FTJs using the MFS structure, where the semiconductor electrode is used for an enhanced TER effect due to modulation of the tunneling barrier height and width. (a) The HAADF-STEM images (inset shows the displacement of Ti ion (green sphere) in BTO (where orange sphere denotes Ba ions)), and the corresponding line scan results using core-level EELS. (b) The PFM hysteresis loops where phase and amplitude signals are in orange and blue color, respectively. The inset of (b) shows the PFM phase image acquired after applying a write voltage of −6 V on 3 × 3 μm^2 area and +6 V in center 1 × 1 μm^2 area using a conductive tip. (c) The ON/OFF ratios with variation in Nb concentrations at 0.1 V read voltage. (d) The resistance−voltage hysteresis characteristics measured at a read voltage of 0.1 V with variation in peak voltage V_p and with pulse duration of 10 ns. (e) Resistance retention characteristics for 32 resistance states, i.e., five-bit multibit storage. (f) Endurance characteristics.[278]

structure was explored. The idea was to replace one electrode in conventional FTJ with a heavily doped semiconductor (Nb:$SrTiO_3$). It showed η of ∼10^4 at RT, which is two orders higher magnitude than conventional FTJ with MFM structures. Apart from this, a retention time measured up to 10^5 s, extrapolated to 10 years, and an endurance of >10^3 cycles was demonstrated.[251] In recent times, TER has been evidenced in numerous ferroelectric complex oxides (e.g., $BaTiO_3$, $PbTiO_3$, or $BiFeO_3$, etc.) at RT and summarized in Table 5.[262] In 2013, Zenkevich et al. gathered information from a metal/ferroelectric interface by hard X-ray photoemission experiments and determined the Pt/BTO and Co/BTO barrier heights. The calculated barrier heights were used to fit the $I-V$ curves measured at RT for Cr/BTO/Pt, MFM FTJs, and η of 30 was understood as a tunnel barrier potential profile modulation in a direct tunneling regime.[268] A giant TER effect (η of ∼10 000) for 180 nm scaled Co/$BiFeO_3$/$Ca_{0.96}Ce_{0.04}MnO_3$ FTJs was reported by Yamada et al.[269] Here, $BiFeO_3$ ultrathin films deposited on $YAlO_3$ substrates are predicted to stabilize the T-Phase of $BiFeO_3$ and show giant tetragonality expected to have large spontaneous ferroelectric polarization.[270−272] Yin et al.[273] and Jiang et al.[274] demonstrated enhanced TER ratio (nearly two orders of magnitude) by insertion of metal−insulator transitionmanganite, e.g., insertion of $La_{0.5}Ca_{0.5}MnO_3$ in a $La_{0.7}Sr_{0.3}MnO_3$/$BaTiO_3$/$La_{0.5}Ca_{0.5}MnO_3$/$La_{0.7}Sr_{0.3}MnO_3$ structure.[273] In 2015, Boyn et al.[275] investigated the impact of top electrodes such as W, Co, Ni, and Ir on the band profile in super tetragonal $BiFeO_3$-based FTJs. It was found that the metals with large work functions result in a high metal/ferroelectric barrier height and high OFF/ON ratios (η). However, a higher η resulted in deteriorated switching characteristics (i.e., switching voltage distributions become broad) due to a large built-in electric field. Likewise, Li et al.[276] demonstrated high TER (∼400%) with the addition of heterojunctions and without changing the primary switching properties for ultrathin $BaTiO_3$ (∼0.8 nm)-based FTJs at room temperature. However, retention (10^3 s) and endurance (500 cycles) are much lower than the requirements for state-of-the-art FTJs (section 5.4.1). Apart from this, a figure of merit factor RA, i.e., the product of resistance (R_{ON}) and area (A) was introduced. The addition of extra layers in the MFM structure results in improved TER but at a high RA factor cost. For example, Pt/BTO(7uc)/Nb:$SrTiO_3$, MFM FTJs has RA = 5 MΩ μm^2, which is much larger than 10 Ω μm^2 required for impedance matching of the transistor (generally in order of kilo-ohms). Thus, reduction in thickness of electrodes is also required. Tian et al.[277] proposed that interfacial effects like dead layer, polarization modified layers, and interface chemical terminations are not critical for organic homopolymer PVDF-based MFM FTJs. An overwhelming report on multibit storage capability up to five-bits (32 states) per cell has been recently demonstrated by Ma et al.[278] for an Ag/$BaTiO_3$/Nb:$SrTiO_3$ FTJ (Figure 17) with a high operating speed up to 600 ps and 10 ns that maintains up to 358 K broadening the pathway for FTJs. Figure 17a shows the Ag/$BaTiO_3$/Nb(7%):$SrTiO_3$ MFS FTJs high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) images and the corresponding line scan results using core-level electron energy-loss spectroscopy (EELS). An epitaxial film of ∼2.4 nm (∼6 unit cells) $BaTiO_3$ is estimated. The ferroelectricity in $BaTiO_3$ ultrathin films is confirmed from the PFM hysteresis loops (Figure 17b). Further, the effect of variation in the Nb concentration on TER

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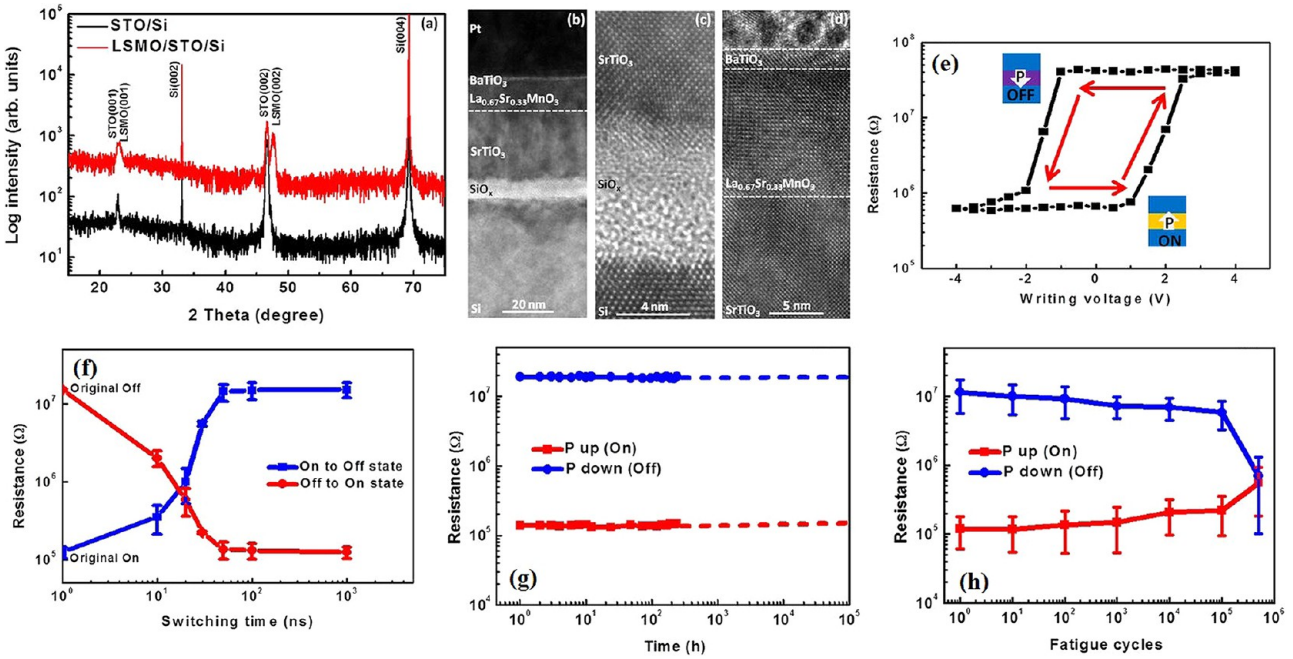

Figure 18. (a) XRD patterns of STO/Si and LSMO/STO/Si structures. HRTEM images (b) Pt/BTO/LSMO/STO/Si structure, (c) STO/Si structure showing an interfacial SiO_x amorphous layer, and (d) Pt/BTO/LSMO/STO, structure. (e) Resistance−voltage ($R-V$) characteristics of the FTJ with 2 nm BTO, (f) switching speed analysis (~50 ns), (g) retention analysis, and (h) endurance characteristics (>10^5 cycles).[282]

ratio is also presented (Figure 17c), which revealed a high TER ratio of 3000 for Nb(0.1%):$SrTiO_3$ concentration, which reduces to ~100−200 for 0.7% Nb. It is also claimed that a higher carrier concentration semiconductor electrode and lower work function metal electrode are required to enhance the operation speed for the MFS-FTJ. There is a trade-off between the operating and TER ratios because a lower concentration of semiconductor electrodes showed higher TER. Figure 17d shows the resistance−voltage hysteresis characteristics measured at a read voltage of 0.1 V that revealed a lower voltage of −2.2 to −3.4 V is required for a pulse duration of 10 ns, while a higher voltage of up to −12 to −18 V was required for a pulse duration of 600 ps. Next, the five-bit (32 states) multibit resistance retention characteristics presented in Figure 17e showed a difference larger than 10% among adjacent states. The resistance retention is also tested for a temperature of 358 K for reliability perspective and practical memory application. Finally, the switching endurance is also reasonable up to 10^8−10^9 cycles (Figure 17f). Of course, the proof-of-concept FTJs device's results look pretty impressive, with five-bit multibit storage in a single cell, even with 10 ns write speed, high endurance >10^8 cycles, and good retention measured until 10^4 s. The resistance states seem to look distinguishable even if extrapolated to 10 years (not shown though), revealing the potential to be the next nonvolatile memory, replacing SSDs and HDDs. But for the ambition to replace RAM (DRAM/SRAM), the endurance needs to be pushed >10^{15} cycles for these FTJs. In the future, it would be interesting to see similar kinds of results in the CMOS-compatible high-volume manufacturing process and also how well these can compete with state-of-the-art 128 layered stacked Flash technology.

In fact, for rapid development and commercialization of practical applications of FTJs, their integration with CMOS technology is required. An attempt made by Li et al.[279] to integrate FTJs on silicon substrates and ferroelectricity was depicted using the conductive-AFM technique with endurance measured up to 10^4 switching cycles. However, essential memory properties such as speed and retention are absent. Likewise, Abuwasib et al. depicted sub-100 nm FTJs integrated into the CMOS process with $R_{on}/R_{off} \approx 125$, but retention, endurance, and speed of FTJs need to be investigated.[280] Chernikova et al.[281] demonstrated ferroelectricity in HZO ultrathin films (~2.5 nm) using PFM and depict its possibility for FTJs, but essential memory characteristics are missing, e.g., retention and endurance. This may open the door to the implementation of FTJs in CMOS. However, a critical investigation may be needed to demonstrate this in the future. For example, in FTJs on silicon (or semiconducting electrode), the space charge in a semiconductor can be switched from accumulation to inversion by polarization switching, which gives a tremendous TER effect due to effective barrier width variation.[251] Therefore, cautious band engineering of the MFS structure is essential, especially the top metal's effective work function, control of carrier type, the doping level of semiconductor, and any possible dipole formation in the interfacial SiO_x layer.[281] Likewise, Guo et al.[282] demonstrated Pt/$BaTiO_3$(BTO)/$La_{0.67}Sr_{0.33}MnO_3$(LSMO), MFM FTJs grown epitaxially on STO/Si for complete nonvolatile memory analysis. Here, memory characteristics are observed with variation in $BaTiO_3$ thickness from 1.5−4 nm. FTJs with 2 nm BTO thickness exhibited a high TER of 15800% with I_{ON} and I_{OFF} of 1.28 μA and 8.03 nA, respectively. Figure 18a shows the XRD spectra of reported STO/Si and LSMO/STO/Si structures, suggesting decent epitaxial growth of perovskite films on silicon. Figure 18b−d shows HR-TEM images of various interfaces of Pt/BTO(2 nm)/LSMO(12.3 nm)/STO-(28 nm)/Si structure, where an interfacial amorphous SiO_x (~8−9 nm) was observed between STO and silicon. Possible reasons for this interfacial SiO_x was given to be due to oxygen diffusion (i) during STO template growth or (ii) through the STO layer during high-temperature (~650 °C) LSMO and BTO depositions. The nonvolatile resistance-voltage character-

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Table 6. Comparison of Ferroelectric Memories with State-of-the-Art Commercial and Emerging Memories[11,331,287a]

memory/property	cell area (F^2)	multibit	voltage (V)	read/write speed	retention	endurance (cycles)	energy
SRAM	>100	1	<1	∼1 ns		$>10^{16}$	
DRAM	6	1	<1	∼10 ns	∼64 ms	$>10^{16}$	pJ/bit
NOR flash	10	2	>10	∼50 ns/10 μs−1 ms	>10 years	$>10^{5}$	10 nJ/bit
NAND flash	≪4 (3D)	3	>10	∼10 μs/100 μs−1 ms	>10 years	$>10^{4}$	1 nJ/bit
FeRAM	6	1	<3 V	<10 ns	10 years	10^{15}	50 fJ/bit
FeFET[233] (endurance mode)		1	4	∼5 ns	<10 s	$>10^{12}$	∼1−10 fJ
FeFET (retention mode)		1	∼1.5	100 ns	>10 years	$>10^{5}$	<1fJ/bit
FTJs[278]	*	1−5	2−18 V	600 ps -10 ns	>10 years	$>10^{8}$	∼0.5fJ/bit
STT-MRAM	6−50	1	<1.5 V	<10 ns	>10 years	$>10^{15}$	∼2 pJ
PCRAM	4−30*	2	<3 V	∼50 ns	>10 years	$>10^{9}$	∼3 pJ
RRAM	4−12*	2	<3 V	<10 ns	>10 years	$>10^{6}$−10^{12}	∼50 pJ

[a]Note: Here F is the lithography Feature size. *3D Integration possible with FTJs, RRAM, and PCRAM to achieve cell area ≪4F^2

istics for Pt/BTO(2 nm) /LSMO(12.3 nm) /STO(28 nm)/Si structure are shown in Figure 18e. The hysteretic variation in tunneling resistance has been observed with a coercive field analogous to ∼2 V. The high (low) resistance corresponding to positive (negative) voltage has been described as the variation in the width of the tunnel barrier because of depletion (accumulation) of holes in bottom LSMO electrodes. The switching speed is ∼ >50 ns as observed from Figure 18f, taken after a write pulse of ±3 V with a variation in pulse width from 1 μs to 10 ns. Figure 18g shows the retention characteristics obtained by measuring tunnel junctions' resistance with aging up to 1 week and TER maintained over 10 000% even if extrapolated to 10 years. Further, endurance characteristics obtained by writing bipolar switching pulse ±3 V and 0.05 ms are shown in Figure 18h. Here, the devices are set to ON/OFF states after each switching cycle followed by the $I-V$ measurements, to examine the resistance state, whereas the FTJs are switchable after 10^5 cycles but with a reduced TER ratio. However, with further cycling, the FTJs cannot function, maybe due to BTO thin films domain wall pinning.[283]

In summary, FTJs have immense potential for future ultradense nonvolatile memories. Scalability has been demonstrated down to 20 nm wide FTJs.[267] However, ferroelectric domain size sets the fundamental scaling limit, which can scale up to a few nanometers in ultrathin ferroelectric films.[276] High speeds down to 600 ps,[278] a high TER ratio > 10^4,[269] a high retention time measured up to 10^5 s,[251] and endurance $>10^8$ cycles are demonstrated.[278] However, the data retention time of >10 years and high endurance $>10^8$ cycles are expected in the same cell. The five-bit multibit storage and minimum reported write energy is ∼0.5 fJ/bit,[278] far better than competing memory technologies. In the future, CMOS-compatible high-performance FTJs, with good thermal stability and reliability are required to be explored. Also, multibit data storage can be explored using magnetic electrodes and ferroelectric barriers, often called multiferroic tunnel junctions (MFTJ).[284] MFTJ is a four-state resistance device that consists of two ferroelectric polarization states of the ferroelectric barrier and two magnetization alignment states of magnetic electrodes.[285] Moreover, the selector less FTJ crossbars are also proposed using analog−voltage−amplitude vector-matrix multiplication that exploits constant conductive states related to a device nonlinearity factor and achieves an energy efficiency >100 tera operations per second per watt.[286]

Finally, we summarize ferroelectric memory devices' general properties compared with state-of-the-art memory devices in Table 6.[11,287] From the comparison in Table 6, generally, there is a perception that better parameters relate to better memory. Therefore, the memory with the best parameters can compete in the market, which is not practical based on the economics and the historical reduction of memory technology's cost with scaling (Figure 1b). Therefore, on the basis of the memory hierarchy requirements shown earlier in Figure 1a and Table 6, the ferroelectric memories have to compete with a particular level in the memory hierarchy. In other words, for the high-density storage class level, long data retention of >10 years and cost are the most critical factors. Here cost directly relates to cell area or the possibility of 3D integration, while reasonable speed of <100−500 ns would be acceptable. Therefore, a possible future alternate here is FeFET (retention mode) for the short-term and FTJs (3D) long term. On the other hand, to replace RAM (SRAM and DRAM), high access speed <10 ns and endurance $>10^{15}$ cycles are critical parameters, while the reasonable cost would be acceptable. Thus, good possible alternates at this level are 1T-1C FeRAM for the short-term and 1T-FeFET (endurance mode) for the long-term.

Apart from single memory cells, to develop memory with high-bit density, it is desired to investigate the array architecture of memory with minimum area. Generally, the widely investigated cell array architectures for NVM are AND, NAND, and NOR architectures.[22] Mueller et al.[288] reported that the AND architecture $V_{DD}/3$ operational scheme provides disturb-free operation. A critical investigation is needed to compare different architectures and determine which architecture is best for FeFET memory arrays. Until now, NAND Flash architecture is believed to be the best for multibit storage nonvolatile memory applications.

6. CONCLUSIONS AND FUTURE PERSPECTIVES

In summary, these studies derive the current research and development status toward next-generation logic and memory devices using the integration of ferroelectric materials. In general, from an area−power−speed perspective, the ferroelectric materials integrated as a gate dielectric in FeFETs can achieve high switching speed (theoretically ps), nondestructive 1T (low area) structure, and low-power operation. We present the integration of ferroelectric materials in different devices and structures expected to compete with existing solutions in the current memory hierarchy.

As per our projection, ferroelectric materials integrated into different device structures/configurations can compete with existing solutions (we propose FeFETs operating in different modes), such as

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(i) In NC mode: ferroelectric gated 1T-type NC FeFETs using the NC effect in ferroelectrics have a strong potential to replace next-generation cutting-edge sub-5 nm technology node low-power CMOS logic devices typically with a supply voltage below 0.5 V. NC FeFETs can serve as a 1T element for 14T CPU registers and 6T SRAM. Moreover, the NC effect is not restricted to FeFETs. Instead, it can be applied to general two-state systems detached by an intrinsic barrier (stored energy), e.g., piezoelectric gate barrier transistors, tunneling relays, NEMS devices, and HEMT.[136,143−148]

(ii) In endurance mode: the 1T-1C type FeRAM for low-density or 1T-type FeFETs for high density can provide fast access time (<10 ns), high endurance (>10^{12} cycles), and average retention time (few ms) that seem suitable to replace DRAM. Here endurance improvement of up to 10^{15} cycles is required for 1T FeFET. Alternatively, possible 3D integration is required for 1T-1C FeRAM to compete with DRAM.

(iii) In retention mode: the 1T-type FeFETs with fast access time (<100 ns), moderate endurance (>10^{6} cycles), and high retention time (>10 years) may compete with Flash. However, slightly improved endurance >10^{8} cycles, multibit storage (2−3 bit per cell), and possible 3D integration are needed to be demonstrated to overpower state-of-the-art Flash technology.

(iv) In X-point mode: FTJs, where ferroelectric materials are employed in 3D cross (X)-point architecture, may work for high-density niche storage applications to replace low-cost per bit external storage devices (HDDs). The five-bit multibit storage in a single cell, even with 10 ns write speed, high endurance >10^{8} cycles, and good retention,[278] can be a pretty good product to replace HDDs. However, possible CMOS compatibility of FTJs may open new embedded applications.

Numerous state-of-the-art systematic investigations are required to fulfill the dream of commercialization for aforesaid ferroelectric devices, for instance, working out the correct array architecture, finding the accurate programming/sensing schemes, reliability of end product related to ferroelectric imprint, fatigue, and statistical variations. Besides this, 2D and organic ferroelectrics are other exciting routes to follow for low-cost and flexible devices. The ferroelectric materials are not only restricted to information storage and computing applications in this era of Internet and portable devices but also for deep-space applications because of the radiation tolerance of ferroelectrics and many more.

FTJs are emerging as ideal systems to investigate polarization switching mechanisms and high-frequency nanoscale ferroelectrics dynamics, a virtually unexplored area.[262] Besides, discoveries of 2D electron gases in complex metal oxide heterointerfaces[289] may open opportunities to couple ferroelectrics[290] with the 2DEG and produce a memory effect that is less sensitive to temperature. In the long term, FTJs have massive potential as memristive devices for neuromorphic architectures.[263] FTJs connected to artificial neural networks can exhibit bioinspired rules-based unsupervised learning.[264,291] Multiferroic tunnel junctions, in which FTJs are combined with magnetic electrodes, have tremendous potential to offer, especially multibit data storage and low-power nonvolatile electric-field-controllable spintronics-based devices, i.e., the nascent field of spin−orbitronics.[292] Despite the rapid recent progress, the area of ferroelectric devices (especially NC-FET and FTJs) is at the dawn and has enormous potential for deeper understanding, research, and development both from fundamental and technological viewpoints.

AUTHOR INFORMATION

Corresponding Author

Satinder K. Sharma − *School of Computing and Electrical Engineering, Indian Institute of Technology (IIT) - Mandi, Mandi, Himachal Pradesh 175075, India;* orcid.org/0000-0001-9313-5550; Email: satinder@iitmandi.ac.in

Author

Robin Khosla − *Institut für Halbleitertechnik (IHT), Universität Stuttgart, Stuttgart 70569, Germany; Department of Electronics and Communications Engineering, National Institute of Technology (NIT), Silchar, Assam 788010, India*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsaelm.0c00851

Notes

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