Design and Jitter Modeling of Energy Efficient High Speed Hybrid ADC

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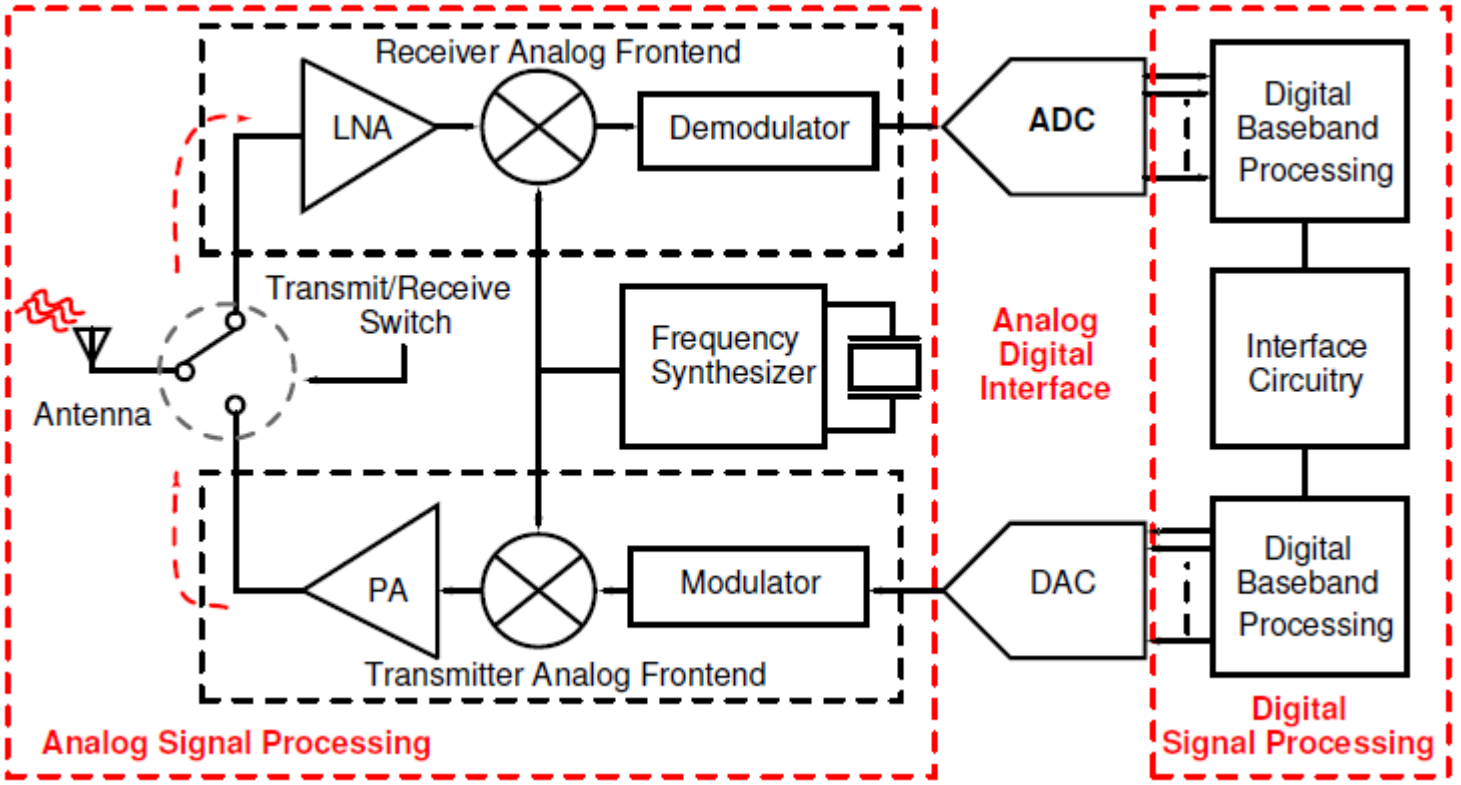
Transceiver



- Converts analog signals into digital bits.
- Syncronization by frequency synthesizer.
- Quantization by comparator circuitry.
- Code conversion by digital logic circuitry.

Selection of ADC

- The analog-to-digital converter (ADC) topology is chosen carefully to achieve the desired trade off between
  - Number of bits,
  - Sampling rate and
  - Power consumption
- Flash ADC
- SAR ADC
- Pipelined ADC
- Hybrid ADC

Literature Survey

- Conversion energy of ADC is reduced by half every 2 years. [1]
- Speed of conversion increases by two folds every 4 years.
- 20 GS/s ADC with a power discipation of 1.2 W. [2]
- Ethernet standard IEEE 802.3bj [3]
  - 100 GS/s (4 X interleaved 25 GS/s)
  - 5–6 Effective Number of Bits (ENOB)
- Long range standard OTU-4
  - 100 GS/s (2 X interleaved 50 GS/s)
  - 5–6 Effective Number of Bits (ENOB)

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[1] Murmann, "Trends in low power digitally assisted A/D conversion", IEICE Trans. Electron, Jun. 2008.

[2] P. Schvan,et.al, "A 24 GS/s 6 b ADC in 90 nm CMOS," ISSCC Dig. Tech. Papers, 2008.

[3] L.Kull, et.al "A 3.1 mW 8b 1.2 GS/s single-channel asynchronous SAR ADC with alternating comparator for enhanced speed in 32 nm SOI CMOS ",IEEE JSSC, Dec. 2013

Literature Survey

- Time interleaving and multi–bit processing can lead to better efficiency. [4]
- Time-interleaved (TI) ADCs are popular architectures that satisfy multi GS/s and high-resolution requirements [5]
- SAR ADCs are superior in aspects of power efficiency and are highly scalable to an advanced CMOS technology [6]
- Time-interleaved SAR ADC designed for 5 GS/s with 10 bits of resolution consumes 76 mW of power [7]

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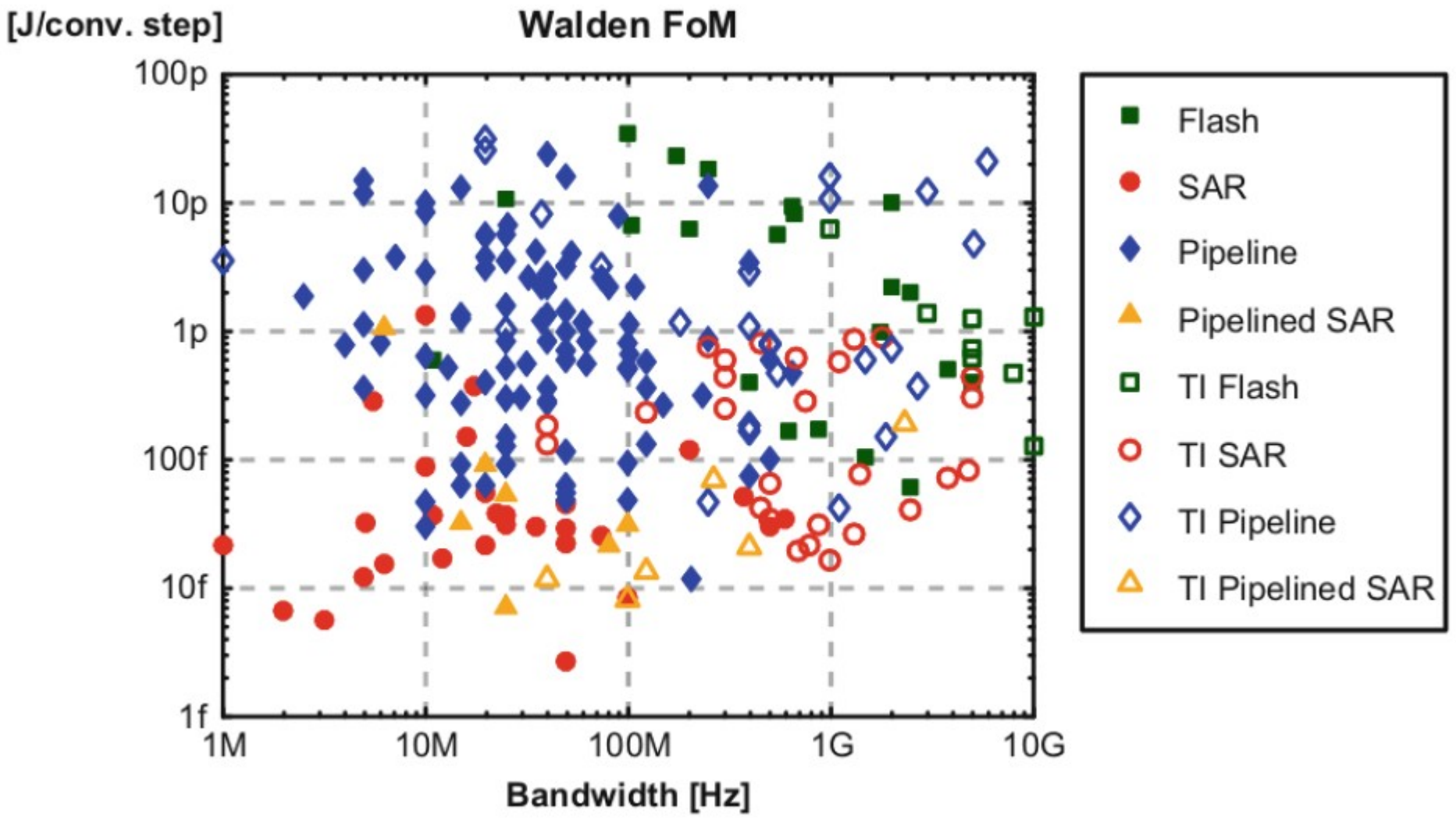
[4] C.H. Chan"A 5.5 mW 6b 5 GS/s 4xinterleaved 3b/cycle SAR ADC in 65 nm CMOS",ISSCC, Mar. 2015.

[5] K. Doris, et.al, "A 480 mW 2.6 GS/s 10b time-interleaved ADC with 48.5 dB SNDR up to Nyquist in 65 nm CMOS," IEEE JSSC, Dec. 2011

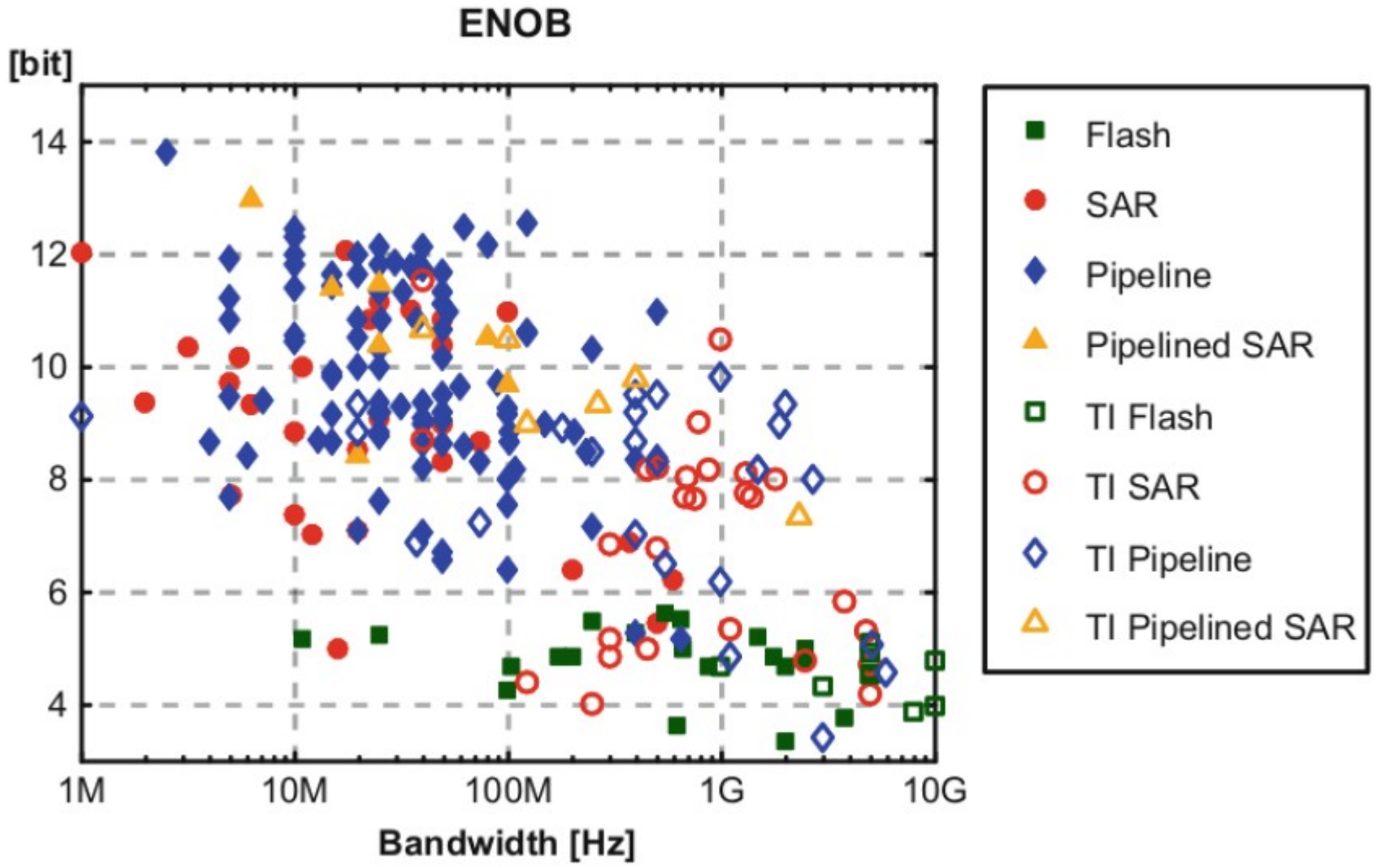
[6] M. Inerfield et al., "An 11.5-ENOB 100-MS/s 8mW dual-reference SAR ADC in 28nm CMOS," in Symp. VLSI Circuits (VLSI), Jun. 2014.

[7] J. Fang et.al"A 5-GS/s 10b 76-mW time interleaved SAR ADC in 28 nm CMOS"IEEE TCAS-I, Jul. 2017.

FOM: ISSCC 1997-2016



ENOB: ISSCC 1997-2016



Background

- Analog-to-digital converters (ADC) play an important role in the design of radio frequency (RF) transceiver architectures [8]
- Hybrid ADC architectures exhibit excellent performance for analog and mixed signal (AMS) systems.
- Successive Approximation Register (SAR) ADC
  - Lower power consumption for higher resolution (N).
  - Medium speed ADC
  - Conversion Speed = N clock cycles
- Flash ADC
  - Higher bandwidth
  - Higher power consumption
  - Conversion speed = 1 clock cycle

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[8] S. Kundu, et.al, "A 1.2 V 2.64 GS/s 8-bit 39 mW skew-tolerant time-interleaved SAR ADC in 40 nm digital LP CMOS for 60 GHz WLAN," in IEEE CICC, Sep. 2014, pp. 1–4.

Aerial view

- Broad bandwidth techniques
  - Time interleaving [9]
  - Alternating comparator [10]
  - Multi-channel ADC techniques [11]
- Non–ideal effects
  - Offset Cancellation
  - Kickback noise reduction

[9] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," IEEE JSSC, vol. 42, no. 4, pp.739–747, Apr. 2007.

[10] L. Kull, et.al "A 3.1 mw 8b 1.2 GS/s single-channel Asynchronous SAR ADC with Alternate Comparators for Enhanced speed in 32 nm Digital SOI CMOS," IEEE JSSC, vol. 48, no. 12, pp. 3049–3058, Dec. 2013.

[11] Z. Cao, et.al, "A 32 mW 1.25 GS/s 6-b 2b/step SAR ADC in 0.13µm CMOS," IEEE JSSC, vol. 44, no. 3, pp. 862–873, Mar. 2009.

Flash Architecture

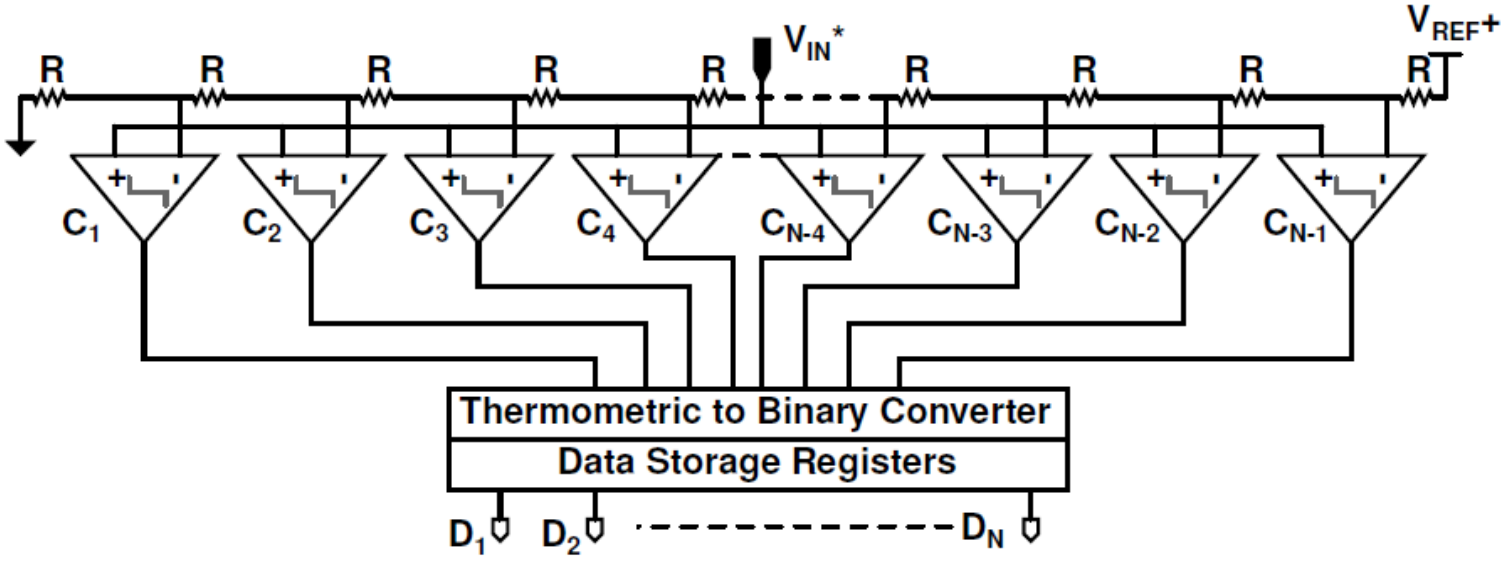


Figure: Block diagram of a flash analog-to-digital converter [12]

- Increased bandwidth
- Higher power consumption
- Conversion cycles = 1 clock cycle
- Parallel processing architecture
- 2^N-1 comparators
- Comparator offset variation

[12] P.E. Allen, D.R. Holberg, CMOS Analog Circuit Design. Oxford Series in Electrical and Computer Engineering, Oxford University Press, 2002, ISBN: 9780195116441.

SAR Architecture

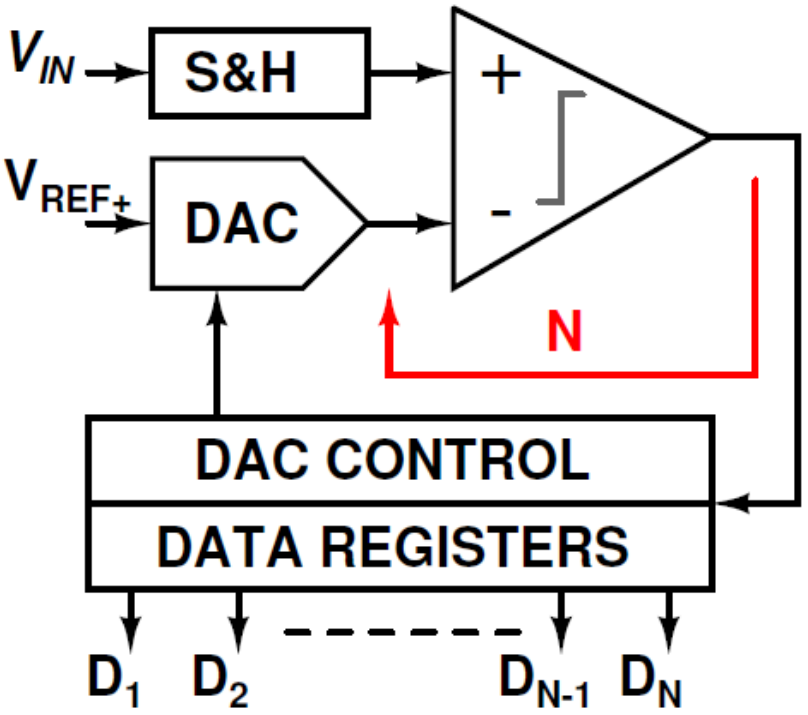


Figure: Block diagram of a successive approximation register ADC [13]

- Serial processing ADC
- Lower power consumption for higher resolution
- Medium speed ADC ($\leq$ 100 MHz)
- Conversion cycles = N clock cycles
- Hardware efficient
- Binary search algorithm

[13] R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, second ed.,Wiley-IEEE Press, 2004, ISBN: 047170055X.

Hybrid ADC: Flash and SAR

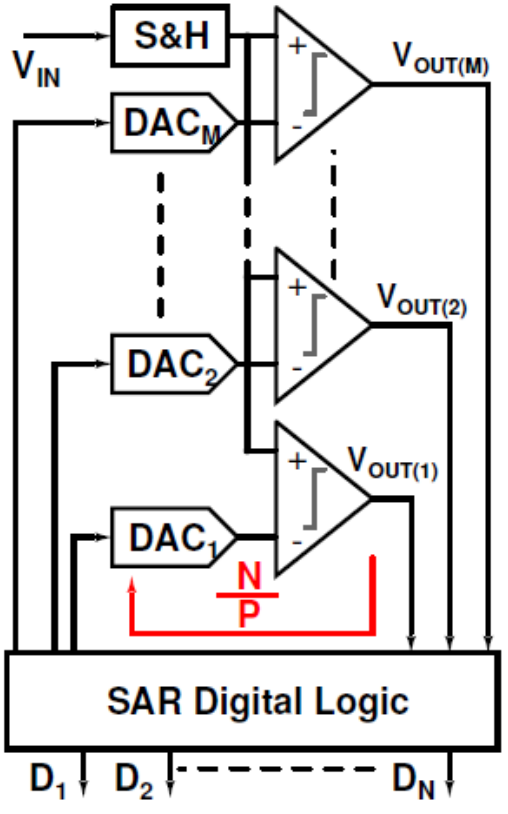


Figure: Block diagram of a hybrid flash-SAR ADC [14]

- Binary search algorithm with parallel conversion of partial bits.
- Each cycle produces P bits.
- The search space is divided into M+1 ($2^P = M+1$).
- Conversion cycles = $\frac{N}{P}$ clock cycles.
- 2^P-1 comparators and DACs.
- Bits per cycle is a trade-off between area and speed.

[14] Seyed Alireza Zahrai and M. Onabajo, "A low-power hybrid ADC architecture for high-speed medium-resolution applications," 2015 IEEE 58th International Midwest Symposium on Circuits and Systems, Aug. 2015, pp. 1-4.

Hybrid Architecture [15]

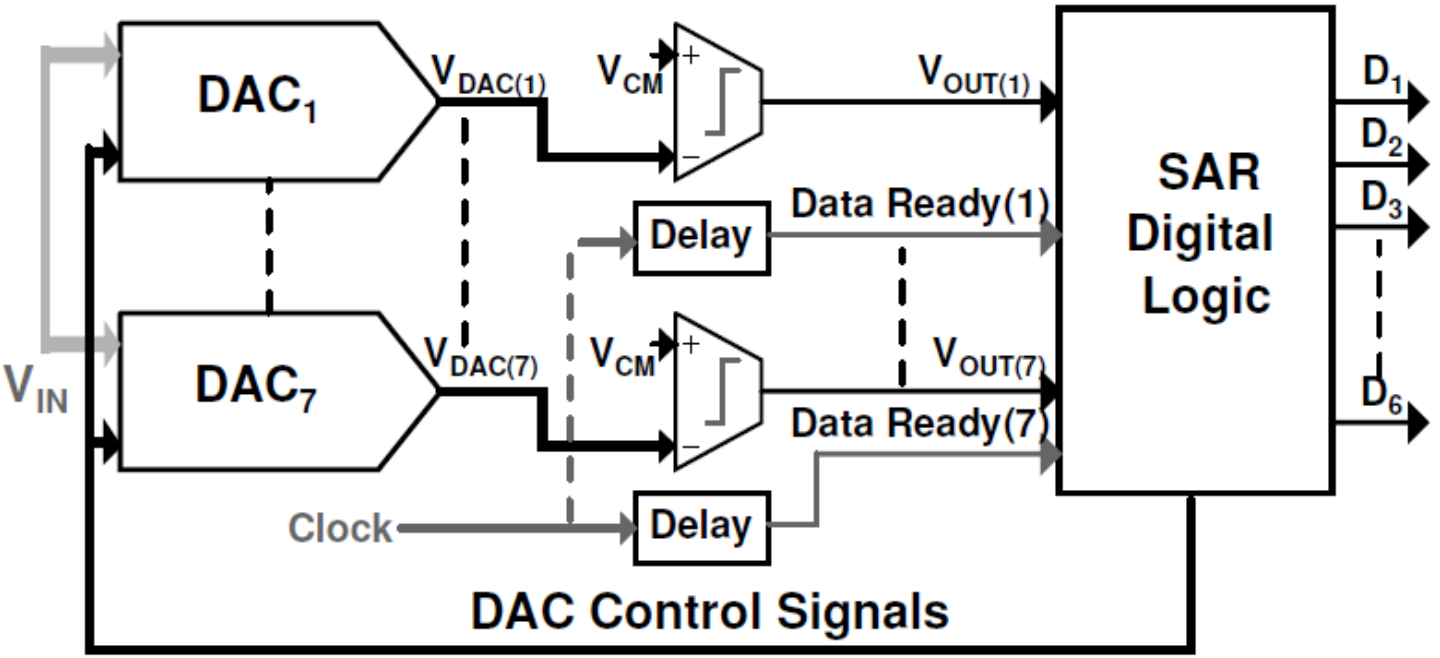


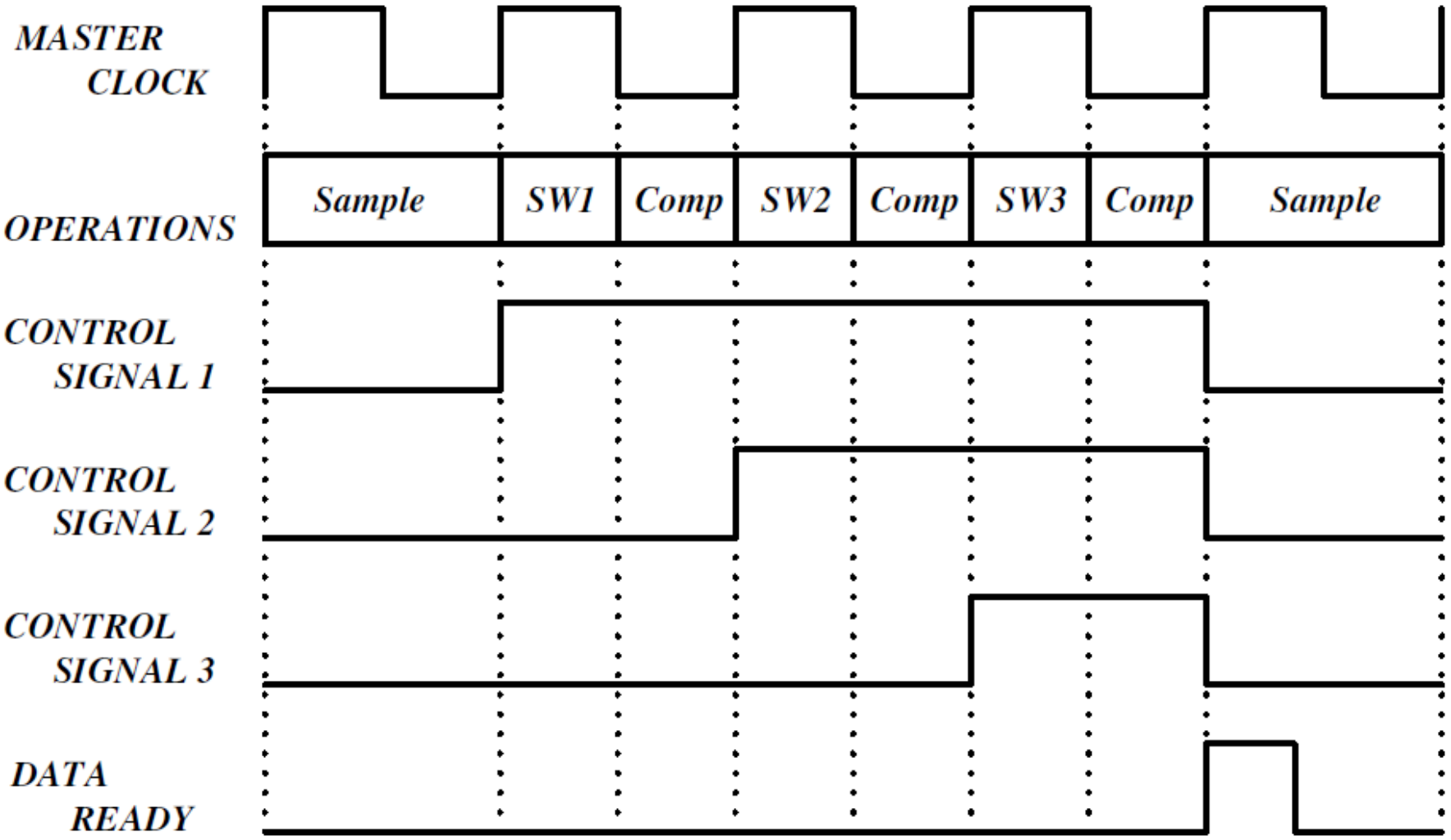
Figure: The block-diagram of a 3-bit per stage, 6-bit flash-SAR ADC.

[15] Dinesh Kumar B. et. al, "Design of Hybrid Flash-SAR ADC using an Inverter based Comparator in 28 nm CMOS", in Elseiver Microelectronics Journal, Volume 95, Jan. 2020, 104666, ISSN 0026-2692.

Salient Features

- A serial SAR ADC combined with a parallel flash ADC.
- The flash ADC achieves faster operation.
- The SAR ADC achieves efficient energy conversion.
- DACs and comparators forms the flash architecture.
- SAR digital logic forms the SAR loop.
- Conversion cycle is reduced by $(N/m) + 1$.
- A 2-bit/cycle architecture is adopted.

Timing Diagram



SW: Switching operation *Comp: Comparision*

Design Specifications

Table: Specifications of the hybrid flash-SAR ADC

Power Supply	0.9 V
Technology Node	28 nm CMOS
Architecture	Hybrid
Speed	1 GS/s
Algorithm	3 bit/cycle
Resolution	6 bits
Power	2.33 mW
FOM [11]	47.7 fJ/conv

[11] $\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times F_s}$,

Specifications

- Comparator
  - Bandwidth = 4 GHz,
  - Resolution = 14 mV,
  - Decision time = 94 ps.
- Digital logic
  - Clock Control,
  - DAC Control,
  - Thermometric to binary encoder,
  - Memory unit.
- Segmented split capacitor DAC
  - Resolution = 14 mV,
  - Speed = 4 GHz,
  - Unit capacitance = 8 fF,
  - Settling time = 20 ps.

Inverter based Comparator

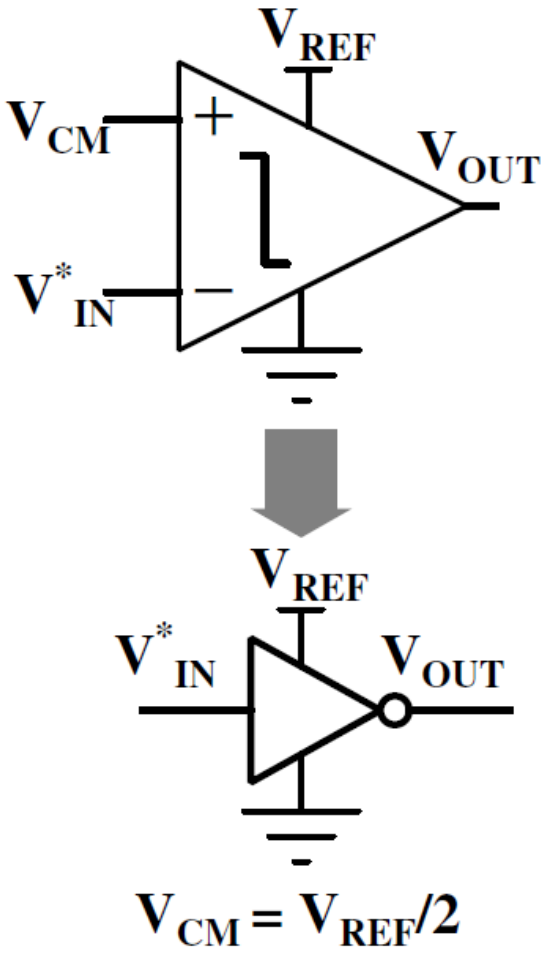


Figure: Idea of inverter based comparator.

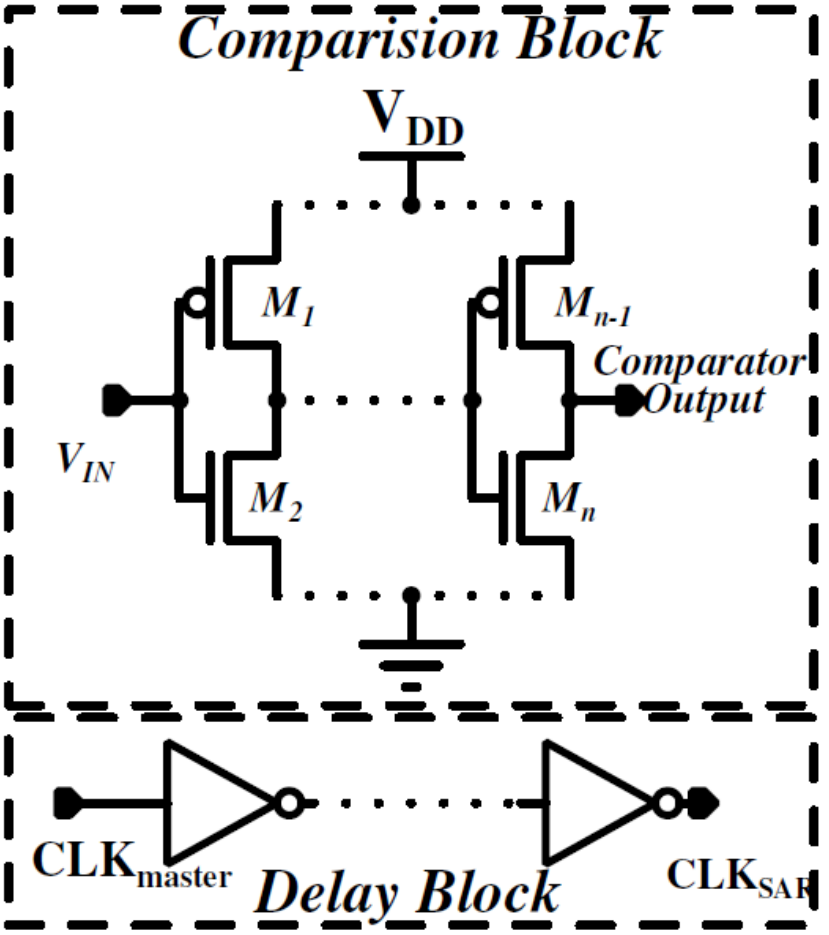


Figure: The schematic of inverter based comparator.

Common Mode Feedback (CMFB)

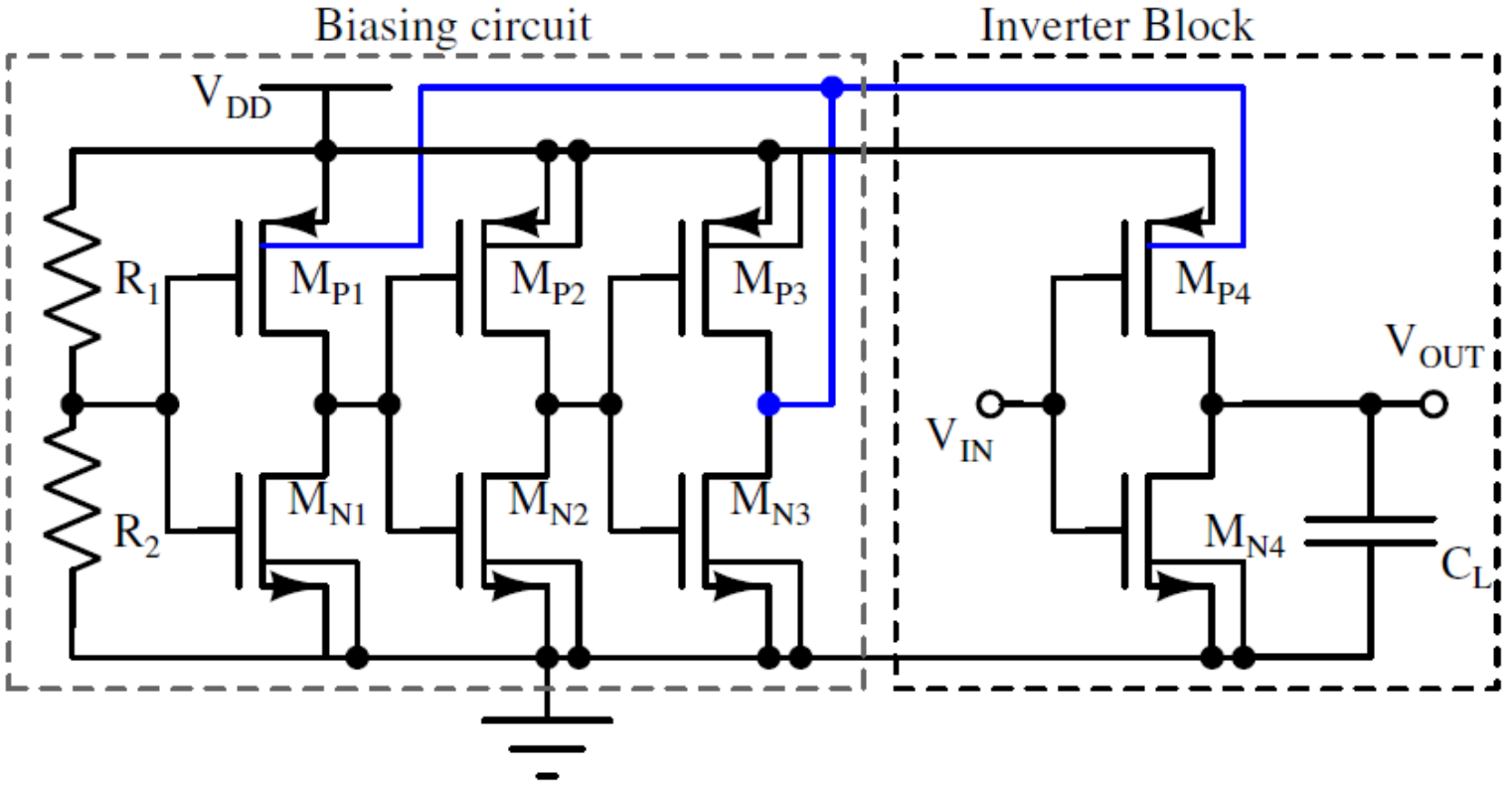
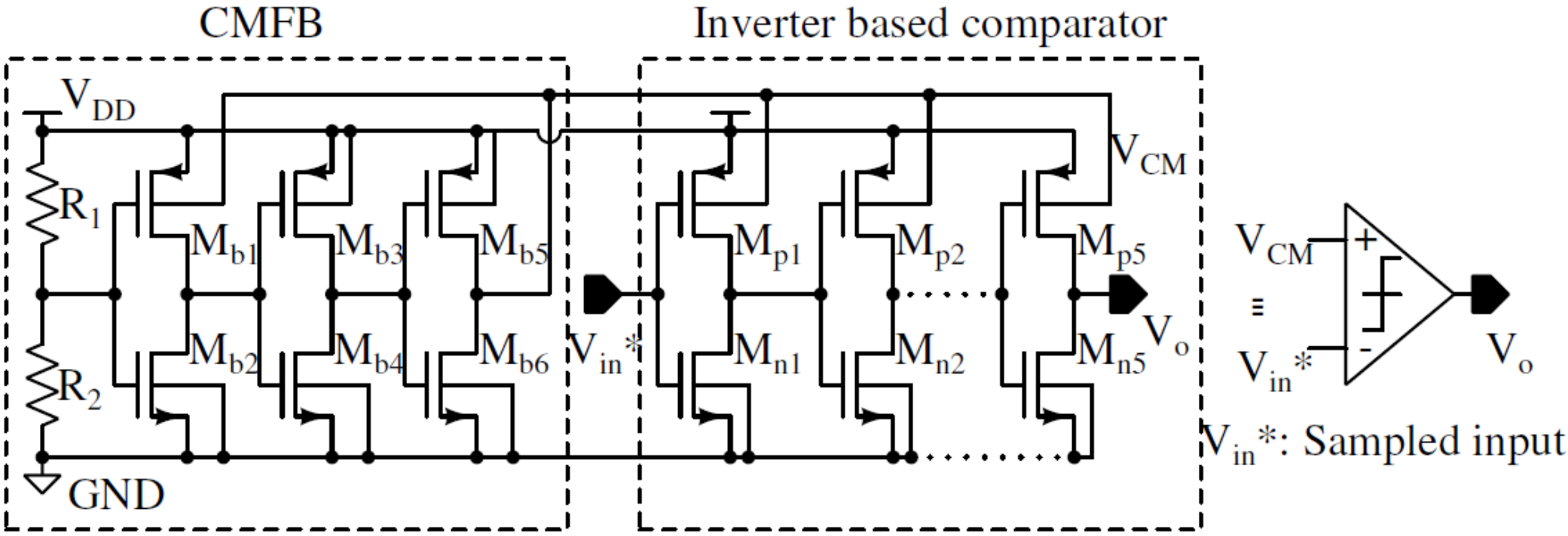


Figure: VCM compensated single stage inverter based comparator [16].

[16] H. Shrimali and S. Chatterjee, "11 GHz UGBW Op-amp with feed-forward compensation technique", in IEEE ISCAS, May 2011

Proposed Inverter based Comparator



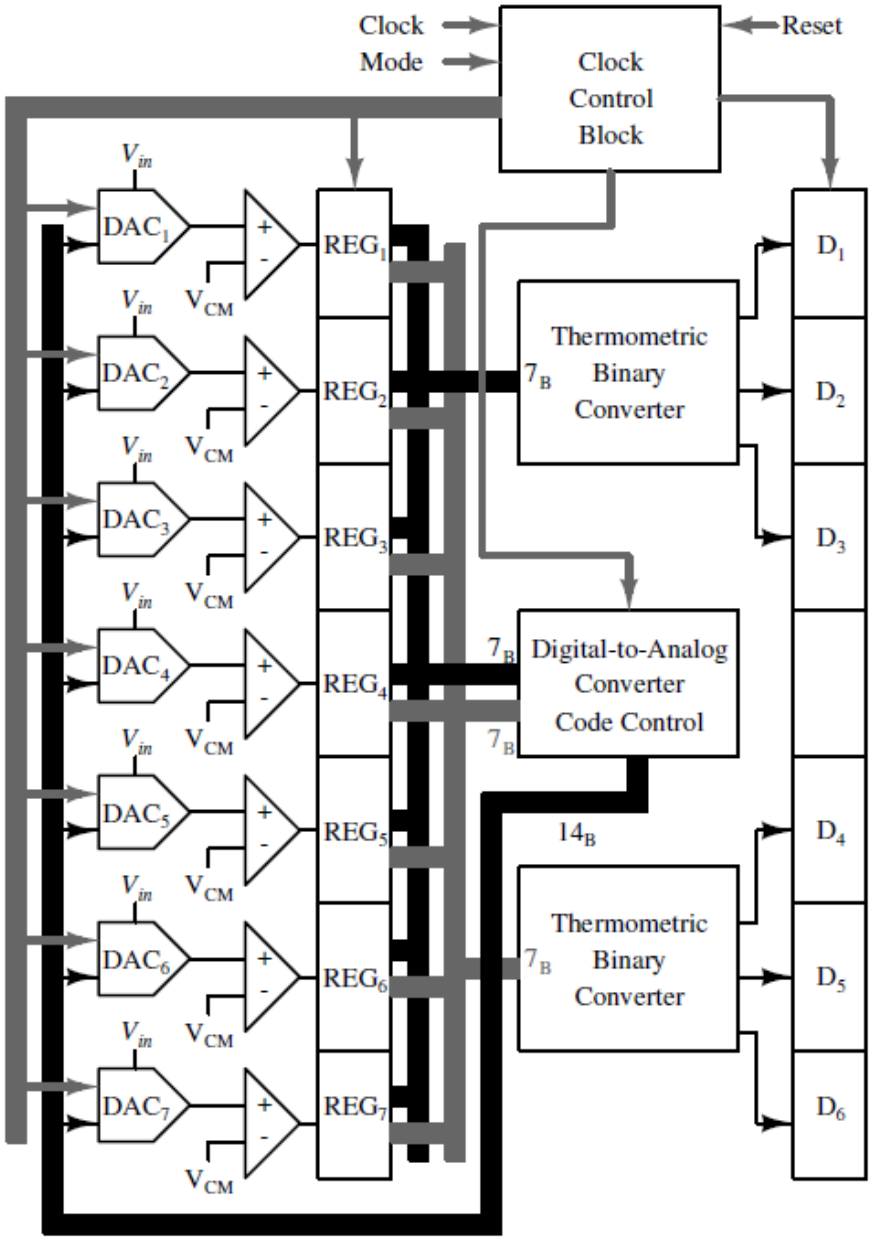
Inverter based Comparator

- An inverter can be used as a comparator, when
  - Swithching Threshold $= V_{CM}$.
- Common–mode–feddback (CMFB) circuitry for fixing the V_{CM} [16] across PVT variations.
- Input offset voltage requirements can be achieved with a chain of inverters in cascade [17]
- The δ delay for data ready is created using chain of inverters.

[16] H. Shrimali and S. Chatterjee, "11 GHz UGBW Op-amp with feedforward compensation technique," in IEEE ISCAS, May 2011, pp. 17– 20.

[17] I. Sutherland, et.al, Logical Effort: Designing Fast CMOS Circuits. San Francisco, CA, USA: Morgan Kaufmann Publishers Inc., 1999.

Power Aware 3bit/cycle ADC



Charge Scaled DAC (CDAC)

- The CDAC converts the digital input to an analog voltage.
- The CDAC decides the
  - Integral Non Linearity (INL)
  - Differential Non Linearity (DNL)
  - Signal to Noise Ratio (SNR)
- Inherent sample and hold circuit
- No static power consumption
- Bottom plate sampling to avoid parasitic effects
- Capacitance spread of DAC increases with number of bits
- Lower switch resistance

CDAC Architectures

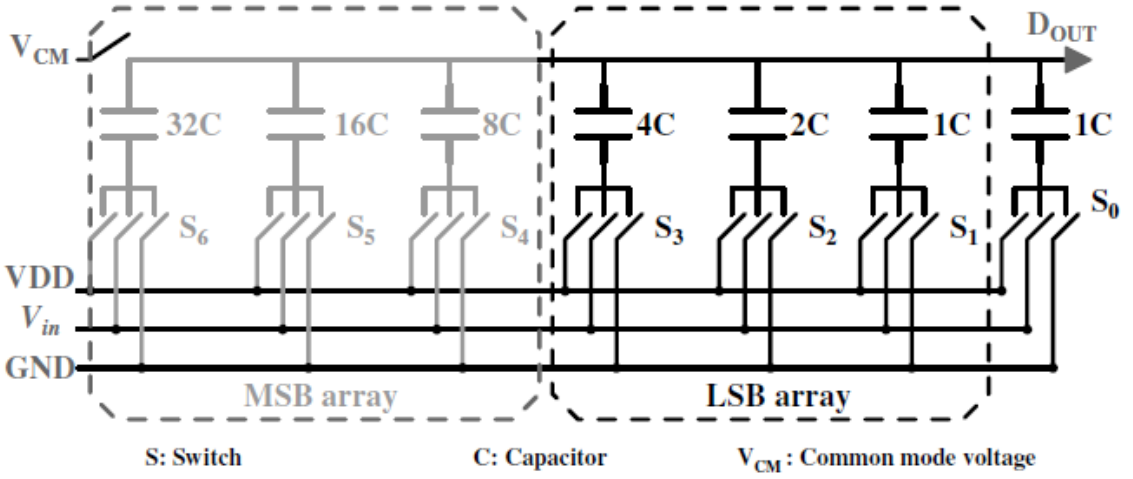


Figure: Conventional CDAC architecture.

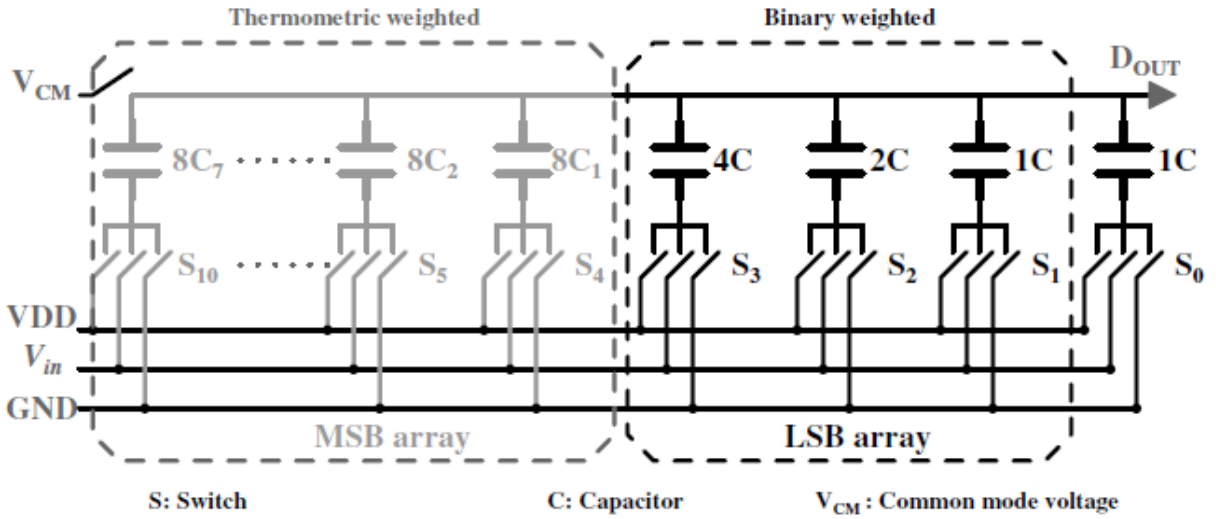


Figure: Segmented CDAC.

Proposed CDAC

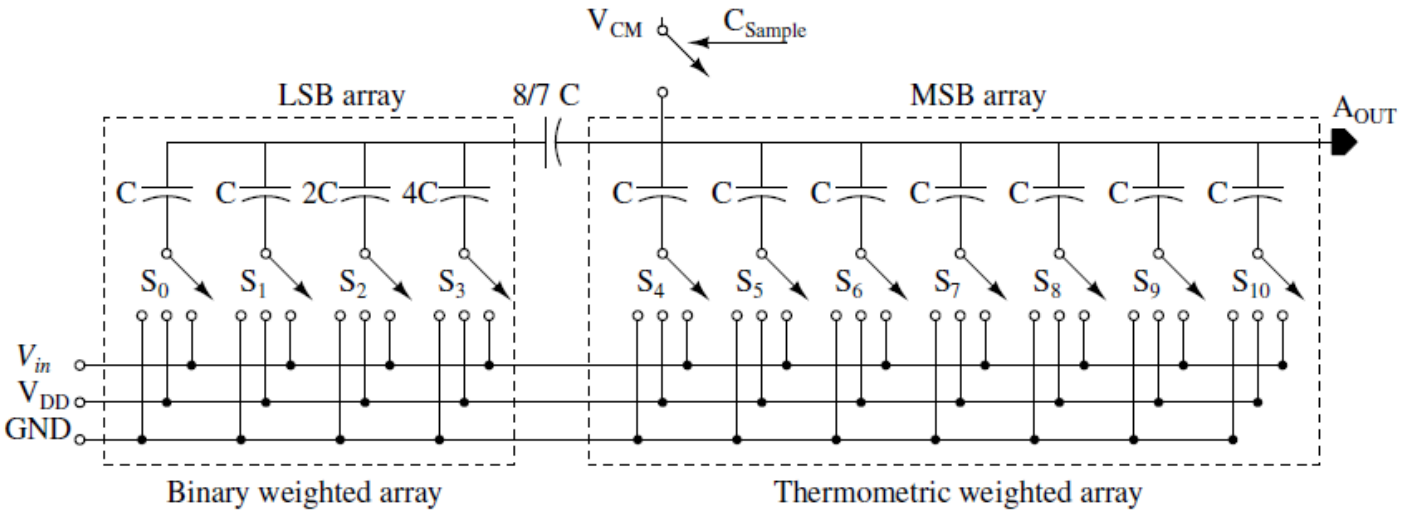
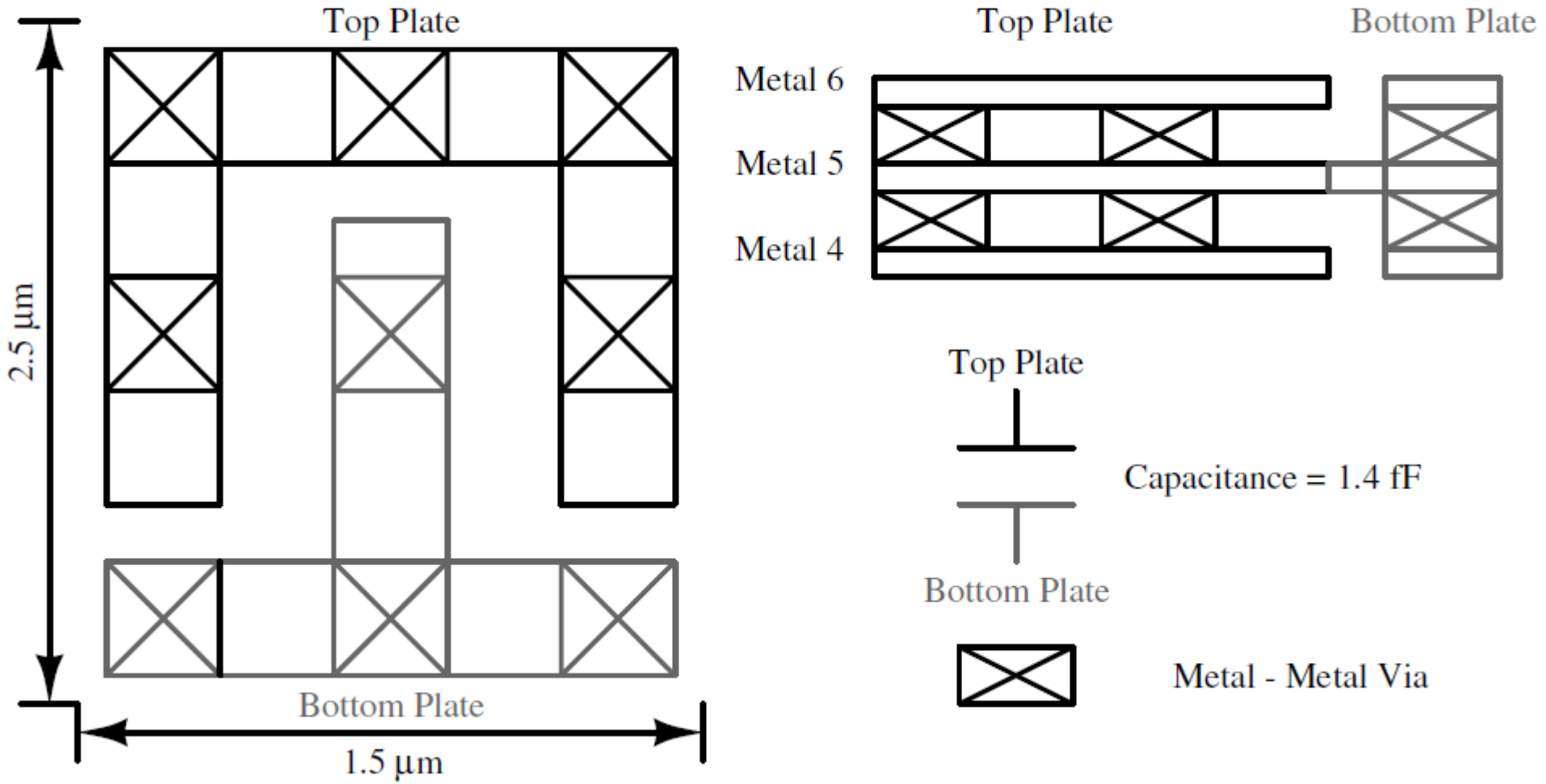


Figure: Implemented segmented split-capacitor array CDAC.

- 87% reduction in area
- Reduced capacitance spread
- Increased speed
- Requires only simple switch circuit.

Custom Capacitance: UMC130



Results (28nm CMOS)

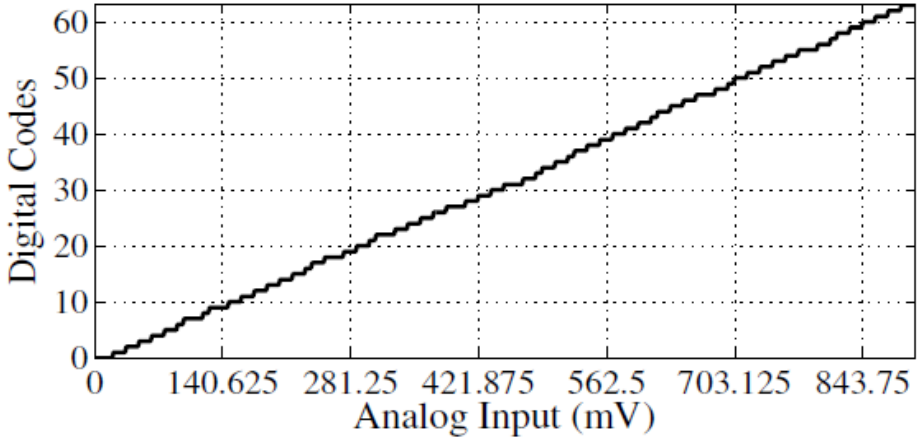


Figure: I/O characteristics for ADC.

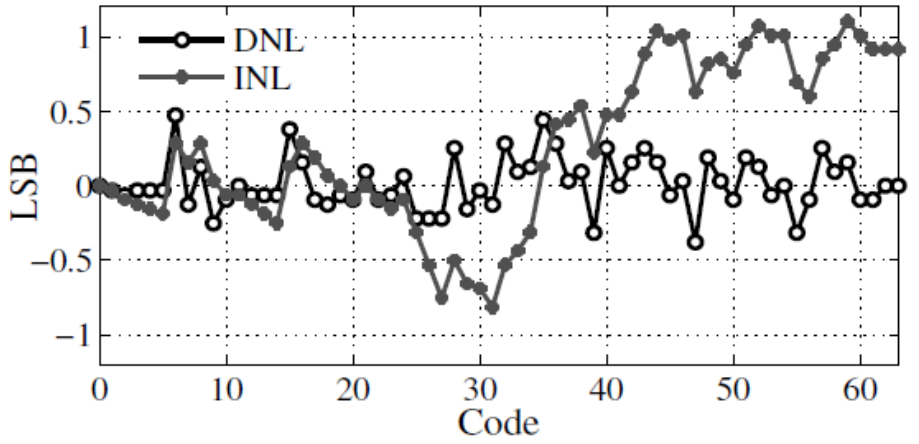


Figure: INL/DNL plots for the ADC.

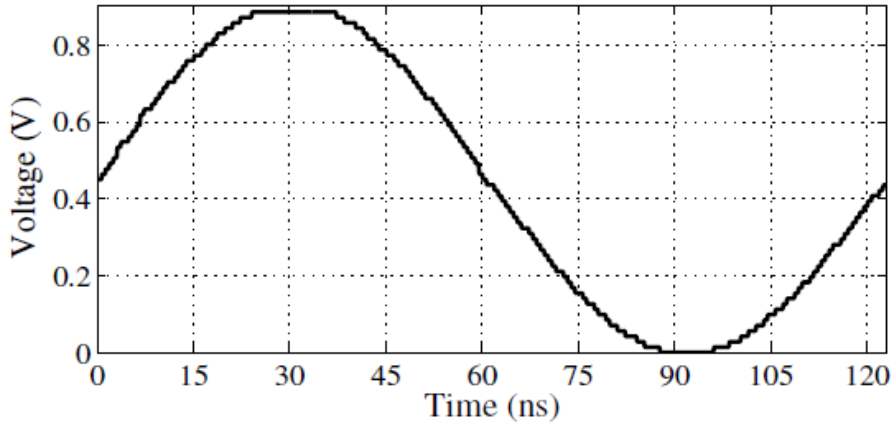


Figure: Transient response of the ADC.

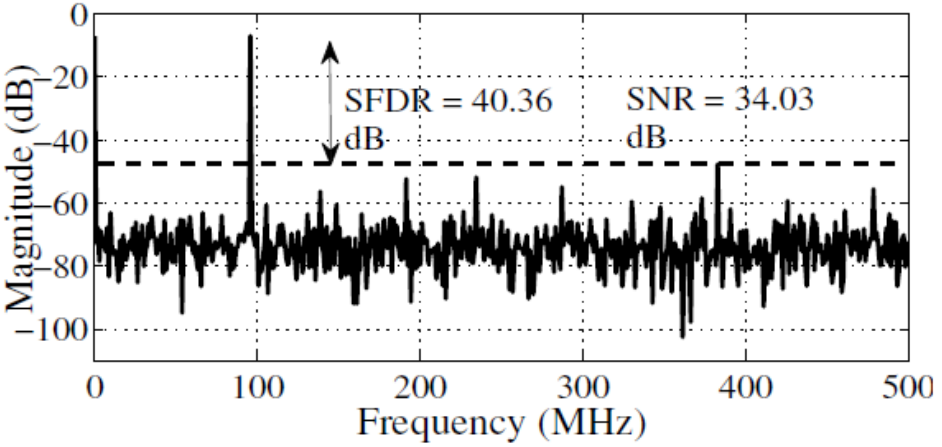


Figure: 1024-point FFT

Results (28nm CMOS)

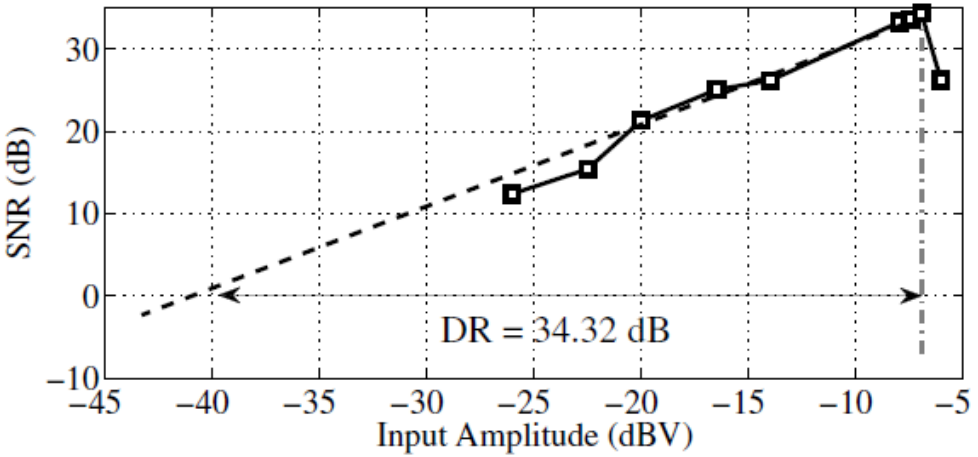


Figure: Variation of the SNR with input signal amplitude for a 1 MHz sinusoid.

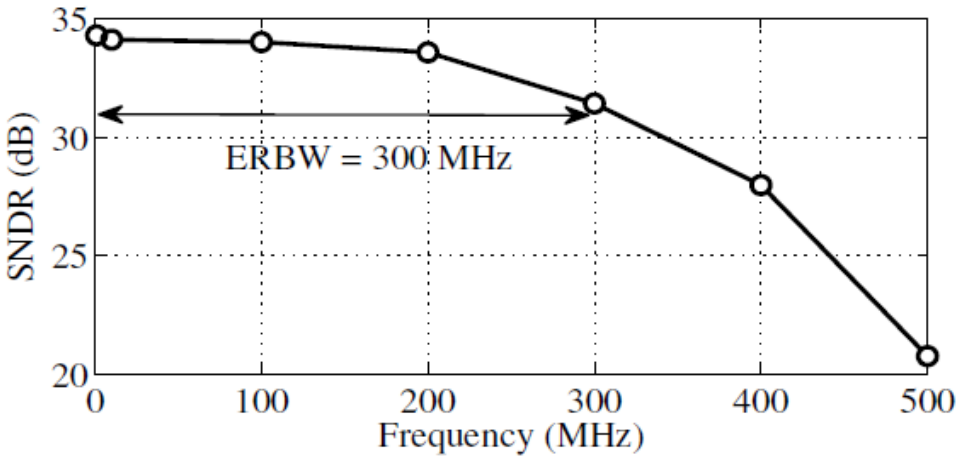


Figure: Variation of SNDR with input signal frequency.

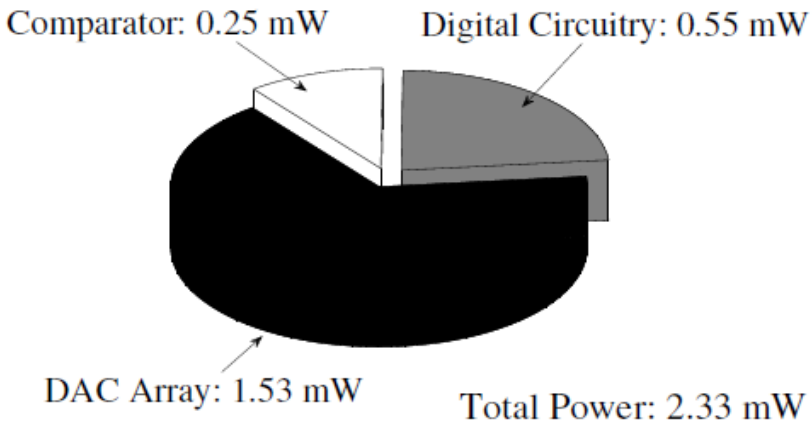


Figure: Power consumption of various sub-blocks of the ADC.

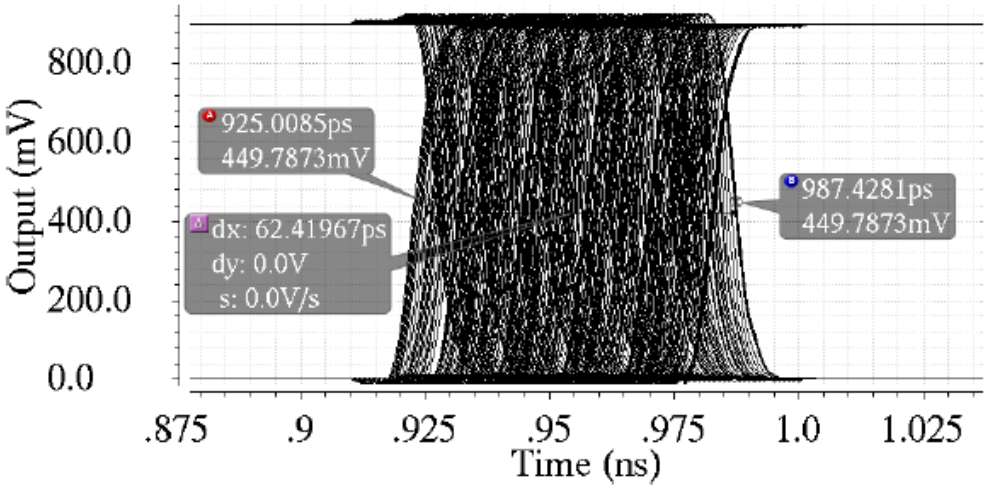


Figure: Eye diagram of the MSB with PRBS of 10 ns bit period.

Results (28nm CMOS)

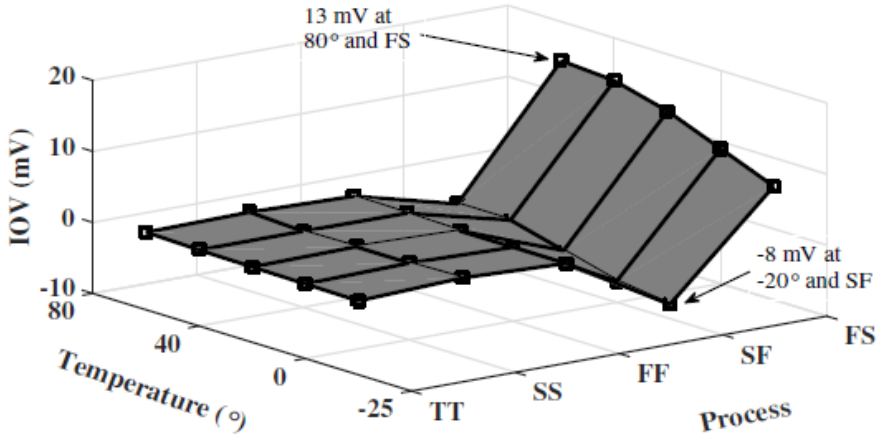


Figure: Variation of input offset voltage (IOV) with process and temperature corners.

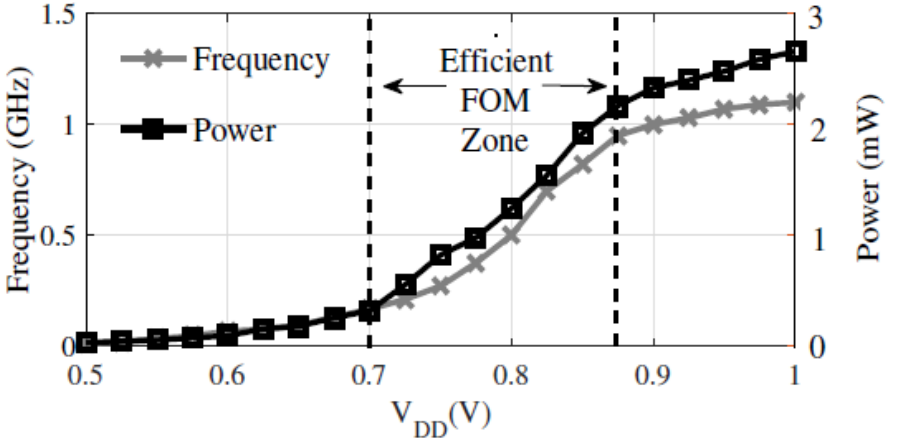


Figure: The speed and power behavior with respect to varying V_{DD}.

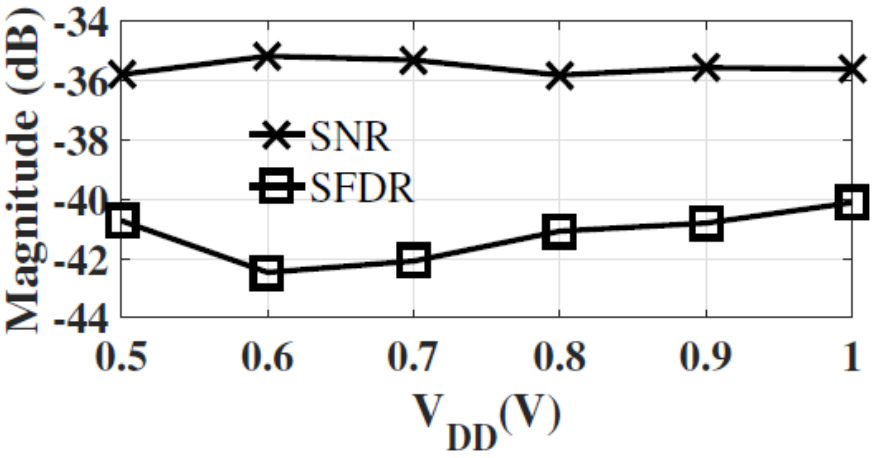


Figure: The SNR and SFDR variations with respect to V_{DD}.

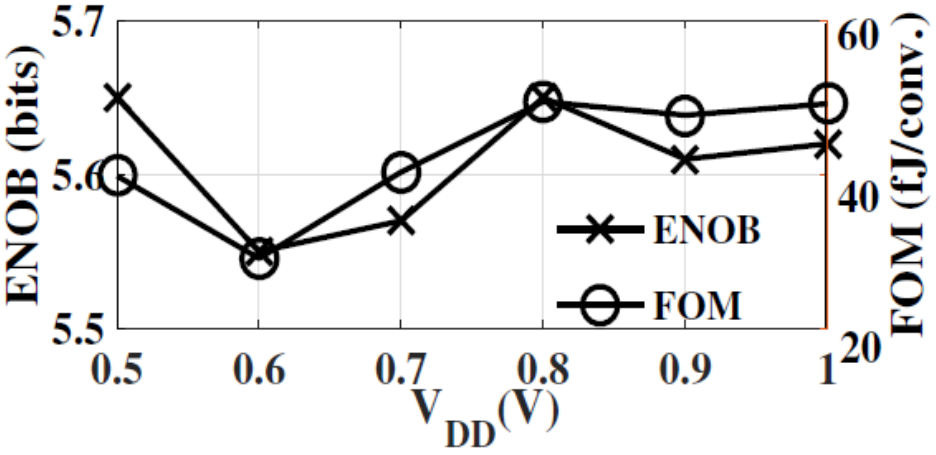


Figure: The ENOB and FOM variations with respect to V_{DD}.

Comparison

Table: Comparison with the state-of-the-art works.

	Technology (nm)	V_{DD} (V)	Architecture	ENOB (Bits)	F_s (GHz)	SNDR (dB)	Power (mW)	Conversion cycles	FOM (fJ/conv)[a]
18 *	55	1.2	SAR	5.6	1.6	35.4	5	7	64
19 *	65	–	2b/cy SAR	5.9	0.32	37.20	9.81	4	479
20 *	180	1.8	SAR	5.87	0.30	36.02	0.64	7	36.47
21 *	180	1.8	FLASH	3.6	0.40	23	0.95	1	190
This work	28	0.9	3b/cy SAR	5.61	1	35.56	2.33	3	47.7
This work	28	0.6	3b/cy SAR	5.55	0.06	35.18	0.01	3	29.56

[a] FOM $= \frac{\text{Power}}{2^{\text{ENOB}} \times F_s}$, * Simulation results.

18 Y. H. Chung and W. S. Rih, "A 6-bit 1.6-GS/s domino-SAR ADC in 55nm CMOS," in ISOCC, Nov. 2017, pp. 216–217.

19 W. Xu, Q. Wei, L. Luo, and H. Yang, "A 6-bit 320-MS/s 2-bit/cycle SAR ADC with tri-level charge redistribution," in IEEE ASID, Sep. 2015, pp.71–75.

20 A. Bekal, et.al, "Sixbit, reusable comparator stage-based asynchronous binary-search SAR ADC using smart switching network," IET Circuits, Devices Systems, vol. 12, no. 1, pp. 124–131, 2018.

21 H. Molaei and K. Hajsadeghi, "A low-power comparator-reduced flash ADC using dynamic comparators," in IEEE ICECS, Dec. 2017, pp. 5–8

Summary: Design

- Supply voltage scalability characteristics.
- Biasing circuitry for fixing V_{CM} across PVT variations.
- Optimum unit capacitor selection for segmented split capacitor DAC.
- Desired sampling rate for efficient FOM.

Jitter Perspectives

- The demand for low power, high speed and robust circuits is increasing in the current scenario.
- Power consumption and speed specifications are crucial for high speed mixed signal systems [22]
- Maintaining the signal integrity (SI) and power integrity (PI) are the major bottlenecks
- The primary sources of jitter are
  - Power supply noise (PSN),
  - Substrate noise,
  - Process variations,
  - Crosstalk,
  - Electromagnetic interference (EMI), *etc* [23]

[22] J. Fang, S. Thirunakkarasu, X. Yu, F. Silva-Rivas, C. Zhang, F. Singor and J. Abraham, A 5 GS/s 10-b 76 mW time-interleaved SAR ADC in 28 nm CMOS, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 7, pp. 16731683, Jul. 2017

[23] K. Oh and X. Yuan, HighSpeed Signaling: Jitter Modeling, Analysis and Budgeting. Prentice Hall, 2011.

VCM compensated Comparator

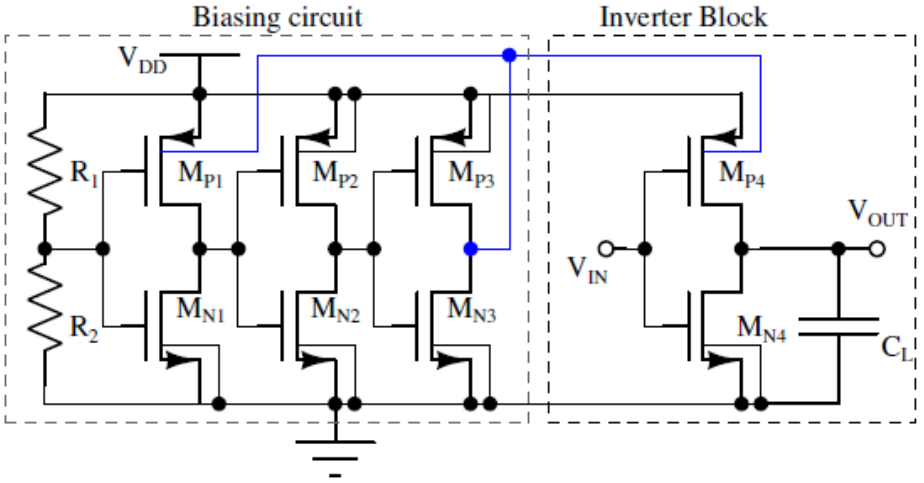


Figure: VCM compensated inverter based comparator with W/L ratios are $M_{N1} = M_{N4} = (0.3\mu m/0.09\mu m)$, $M_{P1} = M_{P4} = (0.51\mu m/0.09\mu m)$, $M_{N2} = M_{N3}$=$(0.1\mu m/0.03\mu m)$, $M_{P2} = M_{P3} = (0.17\mu m/0.03\mu m)$.

The output of the comparator (V_{OUT}) is decided by the switching threshold voltage V_{sw} and is given as:

$$V_{sw} = V_{DD} \frac{r_{ON_N}}{r_{ON_N} + r_{ON_P}}; \quad (1)$$

Small Signal Model

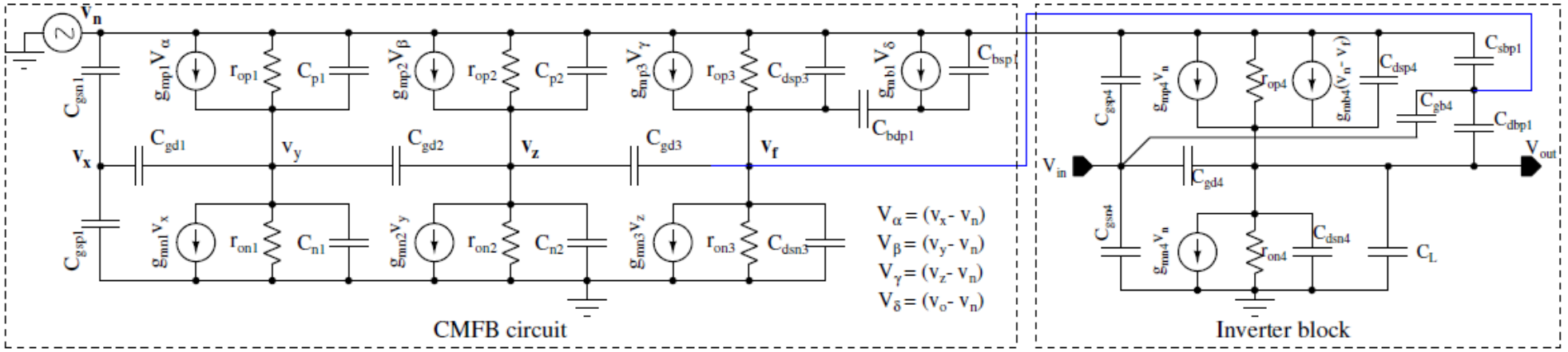


Figure: Small signal model for the VCM compensated inverter based comparator (Fig. 1) in presence of power supply fluctuations.

- The fluctuations in the power supply is transferred to the body of the pMOS transistors and further give rise to PSIJ for the inverter based comparator.
- The admittance matrix method [24] is one of the useful method to solve circuits with large number of nodes.

[24] J. Vlach, V. Ji, and K. Singhal, Computer methods for circuit analysis and design. Springer, 1983.

Transfer Function

The transfer function of a system is defined as [25]

$$\frac{v_f}{v_n} = [C(sI - A)^{-1}B + D]; \tag{2}$$

where,

- v_f is the power-supply,
- v_n is the substrate bounces,
- A is the transfer matrix,
- B is the input matrix,
- C is the output matrix,
- I is the identical matrix and
- D is the transmission matrix.

[25] K. Ogata and Y. Yang, Modern control engineering. Prentice hall India, 2002

Admittance Matrix Method

- Transfer matrix A is written by analysing all the incoming and outgoing currents at each node of CMFB circuit.

$$A = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} & Y_{15} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} & Y_{25} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} & Y_{35} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} & Y_{45} \\ Y_{51} & Y_{52} & Y_{53} & Y_{54} & Y_{55} \end{bmatrix},$$

- B Matrix is the input current with respect to the output,

$$B = \begin{bmatrix} g_{mp1}\left(\frac{R_2}{R_1+R_2} - 1\right) + sC_{gd1} \\ \kappa_2 + g_{mp2} + sC_{gd2} \\ \kappa_3 + g_{mp3} + sC_{gd3} \\ \kappa_4 + g_{mb1} + sC_{db1} \\ -g_{mp1} - g_{mp2} - g_{mp3} - g_{mb1} - \\ \kappa_1 - \kappa_2 - \kappa_3 - \kappa_4 \end{bmatrix},$$

- C matrix is due to the current at the output due to input,
  $C = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix}$,

D is a null matrix as ther is no feed forward element from input to output in CMFB circuit.

EMPSIJ Method

1. Transfer function realisation using admittance matrix method

$$\frac{v_f}{v_n} = [C(sI - A)^{-1}B + D]; \tag{3}$$

where A is the transfer matrix, B is the input matrix, C is the output matrix, I is the identical matrix and, D is the transmission matrix

2. EMPSIJ [26] method for power supply induced jitter estimation

$$J_r = \text{TIE} = \frac{\Delta V_{out}}{\gamma}; \tag{4}$$

where, γ is the slope of rising or falling edge of the comparator output at nominal supply voltage (V_{DD}).

[26] J. N. Tripathi, R. Achar, and R. Malik, "Efficient modeling of power supply induced jitter in voltage-mode drivers (EMPSIJ)" , IEEE Transactions on Components, Packaging and Manufacturing Technology, Oct 2017.

Power Supply Induced Jitter

The output of the comparator due to noise can be expressed as:

$$\Delta V_{out} = \frac{(g_{mp4} + g_{mb4} + g_{dsp4})\mathrm{v_n} + (sC_{dbp4} - g_{mb4})\mathrm{v_f}}{g_{dsp4} + g_{dsn4} + s(C_{gd4} + C_{dbp4} + C_{dsn4} + C_L)}; \quad (5)$$

where, $g_{dsp4} = {r_{op4}}^{-1}$ and $g_{dsn4} = {r_{on4}}^{-1}$.
The closed-form expression for PSIJ can be formulated using:

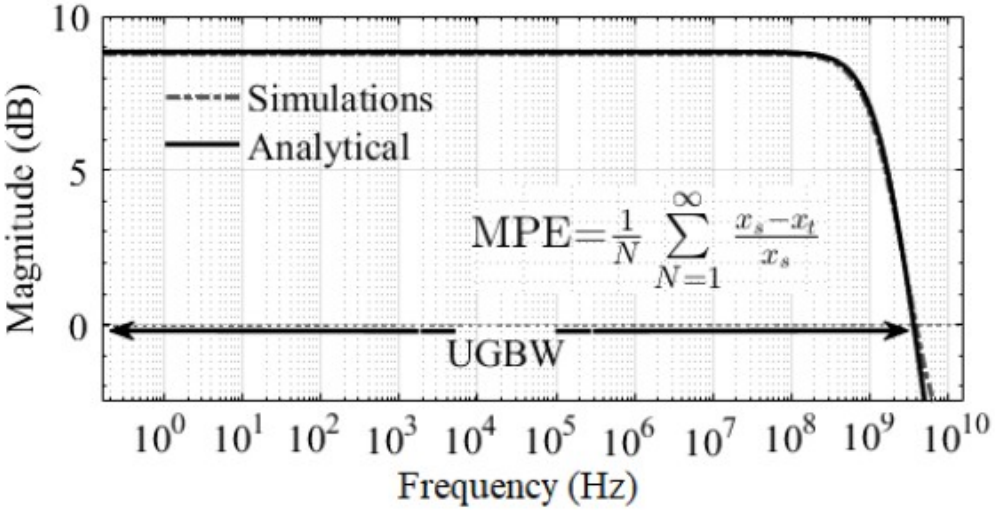
$$J_r = \frac{(g_{mp4} + g_{mb4} + g_{dsp4})\mathrm{v_n} + (sC_{dbp4} - g_{mb4})\mathrm{v_f}}{\gamma(g_{dsp4} + g_{dsn4} + s(C_{gd4} + C_{dbp4} + C_{dsn4} + C_L))}; \quad (6)$$

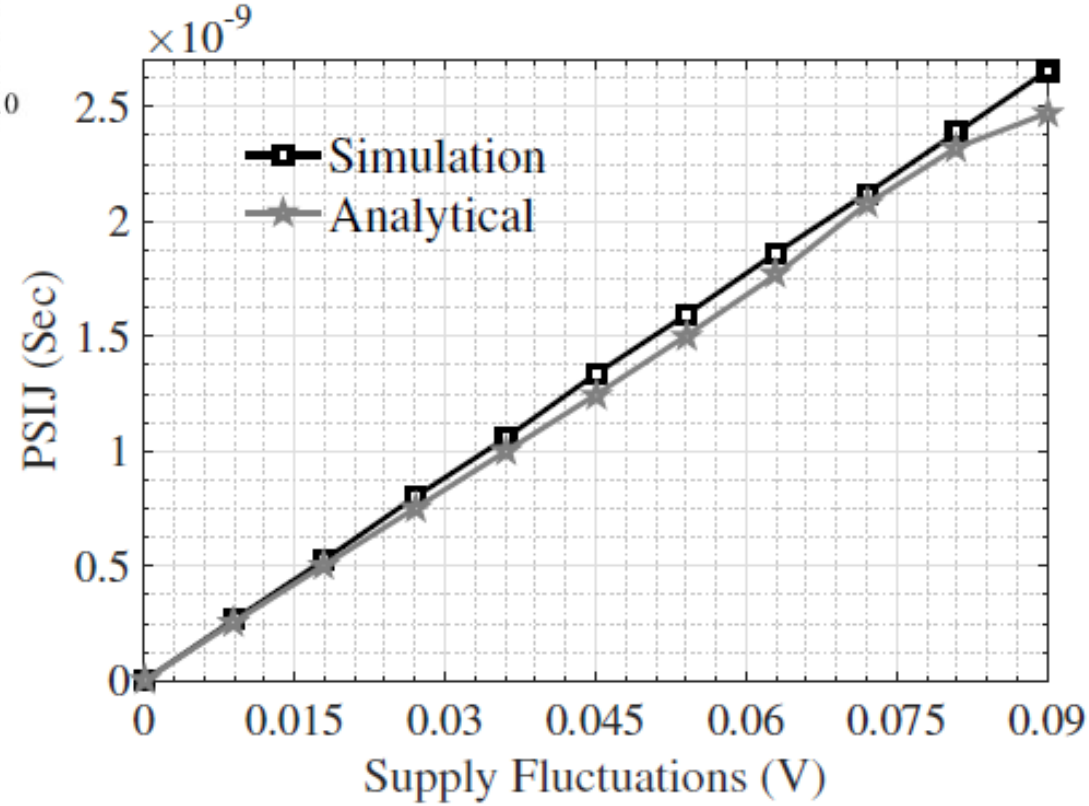
where, $C_{gd4} = C_{gdn4} + C_{gdp4}$.
Next, the peak-to-peak value of PSIJ can be calculated using the following relationship:

$$\mathrm{PSIJ} = \max\{J_r^k\}_{k=1}^{n} - \min\{J_r^k\}_{k=1}^{n}\ , \quad (7)$$

where J_r^k is the TIE at k^{th} rising or falling edge.

Results


10
5
0
Magnitude (dB)
Simulations
Analytical
MPE=$\frac{1}{N}\sum_{N=1}^{\infty}\frac{x_s-x_t}{x_s}$
UGBW
10^0 10^1 10^2 10^3 10^4 10^5 10^6 10^7 10^8 10^9 10^{10}
Frequency (Hz)


$\times 10^{-9}$
2.5
2
1.5
1
0.5
0
PSIJ (Sec)
Simulation
Analytical
0
0.015
0.03
0.045
0.06
0.075
0.09
Supply Fluctuations (V)

Summary: Model

- The proposed model is in agreement with simulation results.
- Impact of jitter is observed in presence of substrate noise.
- PSIJ shows linear increment and can affect SNR.
- Model can be extended for ground noise.
- Method can be extended for analog and digital circuits.

Key References

- **Journal**
  1. Dinesh Kumar B, Sumit K. Pandey, Navneet Gupta and Hitesh Shrimali "Design of Hybrid Flash-SAR ADC using an Inverter based Comparator in 28 nm CMOS", Microelectronics Journal .
- **Conference**
  1. Dinesh Kumar B, Navneet Gupta, Hitesh Shrimali "A 6-bit, 29.56 fJ/conv-step, Voltage Scalable Flash-SAR Hybrid ADC in 28 nm CMOS", in IEEE ISCAS, May 2019.
  2. Dinesh Kumar B, et.al "Analysis of Timing Error due to Supply and Substrate Noise in an Inverter based High-Speed Comparator",in IEEE ISCAS, May 2019.

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सत्यमेव जयते

Goverment Of India

Thank you!