**PRIYANSHU GUPTA**
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## Academic Details

Pursuing PhD in VLSI at School of Computing and Electrical Engineering, IIT Mandi from January 2024

| Examination | Specialization | School/University | Passing Year | CGPA/Percentage |
|---|---|---|---|---|
| M. Tech | Electronics & Communication Engineering | NIT Jalandhar | 2022 | 7.68 |
| B. Tech | Electronics & Communication Engineering | AKTU, Lucknow | 2019 | 67.68 |
| Intermediate | Science | Guru Nanak V M Inter College Hargaon | 2014 | 70.20 |
| Matriculation | Science | Guru Nanak V M Inter College Hargaon | 2012 | 66.67 |

## Current Research Work

**Tittle –** Efficient VLSI Architecture of Training DNN for Edge Applications

## Technical Skills

- Verilog
- Digital Electronics

## Programming Skills

- C programming, python

## Software Used

- Vivado, Xilinx ISE, Cadence Virtuoso,

## Academic Projects & Seminar Projects

**Tittle:-** **IRIS Recognition Biometric System Using machine Learning : (M.Tech Project)**
**Platform:-** Python and using software Anaconda (Spyder) and Goggle Colab **Duration :** 6 Months
**Description:-** Iris recognition biometric system is a CNN-based security problem that identifies persons the introduction of acquisition devices and computers that are ultra-advanced and biometric technology, individuals unique physical and behavioral or physiological biometric method features such as the iris, fingerprint, the face, the retina, the veins, and the hand geometry, and DNA of the behavioral human gait, trademark, and other features keys were identified as the most secure method of authentication and identification scenario of information security. Biometrics is a means of uniquely identifying people based on one or more behavioral patterns or fundamental physical characteristics.
**Keyword's:-** Iris Recognition, segmentation, VGG16 model, NAS-Net model, machine Learning, Convolutional Neural Network.
**Tittle:-** **Comparator Design on FPGA Using Verilog (M.Tech Seminar)** **Duration :** 1months
**Platform:-** Using Xilinx ISE
**Description:-** In this project, a simple 2-bit comparator is designed and implemented in verilog HDL. Truth table, K-Map and minimized equations fpor the comparator are presented. The Verilog code of the comparator is simulated by Model Sim and the simulation waveform is presented.
**Tittle:-** **Traffic Light Controller (B.Tech Project)**
**Platform:-** Using software Xilinx ISE and Verilog RTL Coding with test bench **Duration :** 3 Week
**Description:-** Design traffic light controller using verilog FSM coding and verify with test bench developed the RTL code for each of the sub-blocks used in the block level architechture of the Traffic Light Controller. 'A sensor on the farm is to detect if there to allow the vehicles and change the traffic light to allow the vehicles to cross the highway. Otherwise, highway light is always green since it has higher priority than the farm.

## Achievement in Technical Activities

- VLSI SOC DESIGN using Verilog HDL Trainee at Maven Silicon
- Udemy - Verilog HDL, VLSI Hardware Design Comprehensive Masterclass
- GATE Qualified – 2019, 2024

## Strengths

- Self-Motivated, Positive thinker, Hardworking.

## Hobbies

- Badminton, Travelling and Photography.