The Capacitively Coupled Chopper Stabilized Amplifier with a DTPA based Demodulator

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***Abstract*—This paper presents a chopper stabilized amplifier with a discrete time parametric amplifier (DTPA) based signal demodulator. The DTPA demodulator enables signal amplification while down converting the chopped signal to baseband frequency. The low frequency noise and chopping ripples are cancelled during the track-and-hold process involved in the parametric amplification. The design is implemented in a standard 180 nm CMOS technology and the layout occupies 0.12 mm^2 of area. The post layout simulation results confirm the gain augmentation of 9 dB from the DTPA demodulator. The proposed amplifier consumes 1.02 μA DC current from a 1.5 V supply. The achieved input noise spectral density of 147 nV/$\sqrt{}$Hz gives a noise efficiency factor of 5.4 over 400 Hz bandwidth. Furthermore, the design shows satisfactory performance for -20°C to 80°C temperature range and $\pm$10 % of supply voltage variation at various process corner combinations of transistors. The worst case result is found at slow corner for -20°C with 1.35 V supply and the corner shows 47 dB of gain and 425 nV/$\sqrt{}$Hz of input noise spectral density.**

I. Introduction

The low noise instrumentation amplifier (LNIA) is an important building block of personalized health care monitoring and biomedical data acquisition systems [1]–[3]. The LNIA is also used in low bandwidth measurement systems such as electronic read-out of thermocouple, strain gauge and piezoelectric sensors [4], [5].

Auto-zeroing and chopper stabilization techniques are generally employed to reduce noise in low frequency data acquisition systems [6]. Design trade-offs for these two techniques are well known [6], [7]. The input chopping technique is generally preferred over the auto-zeroing because, the later requires large area to fulfil the $\frac{KT}{C}$ noise constraint coming from the auto-zeroing capacitor. However, to mitigate the effects of impediments from the design trade-offs, amplifiers which incorporate a holding function in the signal demodulator are reported in the literature [7]–[9]. In [8], a track-and-hold (T/H) based demodulator is presented whereas [7] uses a correlated double sampling block for demodulation.

In this work, a discrete time parametric amplifier (DTPA) based demodulation scheme is proposed. This technique provides gain during demodulation of the chopped signal to baseband. Moreover, the augmented gain from the DTPA reduces the effect of noise, when referred back to the amplifier's input. The output ripples and low frequency noise are cancelled without requiring a rigorous low pass filtering.

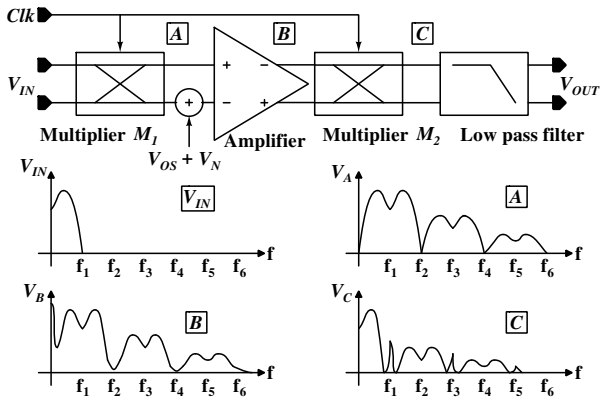

Fig. 1. Concept of conventional chopper stabilized amplifier and frequency spectrum at the relevant locations.

II. Chopper Stabilization and Discrete Time Parametric Amplification

As shown in Fig. 1, the chopper technique avoids the low frequency $1/f$ noise by transposing the input signal to a higher frequency [6]. The modulated input is then amplified, demodulated back to the baseband and passed through a low pass filter. The spectra of signals shown in Fig. 1 explain the process involved in the chopper stabilized amplification. During demodulation of the signal, low frequency noise of the amplifier is up-modulated. The up-modulated noise is then filtered out and input signal is recovered at the output of low pass filter.

Fig 2 shows the working principle of a DTPA where amplification is achieved by varying the gate-body capacitance of a MOS capacitor (MOSCAP) [10]–[12]. A three-terminal variable MOSCAP is realized by shorting drain and source terminals. The amplification process consists of three phases: track, hold and boost. During the track phase, the source-drain terminal is connected to 0 V and the gate terminal tracks the input signal. In the hold phase, the input switch is turned off but the source-drain terminal remains at zero potential. During the boost phase, the gate terminal remains floating but the source-drain terminal is connected to V_{DD}. Eventually, the effective gate-body capacitance becomes less than the gate-channel capacitance. Here, since the gate is floating, the gate charge is constant. According to the charge conservation principle, the gate-body voltage increases to

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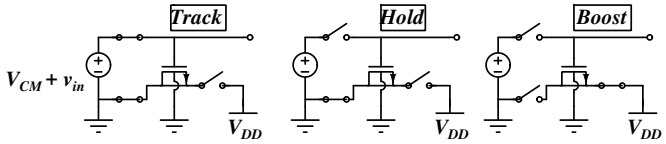

Fig. 2. Principle of a NMOS discrete time parametric amplifier: Track, Hold and Boost phases.

counteract reduction in the capacitance. Hence, amplification of the held voltage is obtained during the boost phase.

III. The Proposed Chopper – DTPA Amplifier

Fig. 3 shows the block diagram of proposed chopper stabilized amplifier with a DTPA demodulator. Only one output path is shown here for simplicity. The Chopper – DTPA amplifier comprises of a chopper modulator clocked by C_{CLK} signal, an amplifier, a DTPA demodulator controlled by D_{CLK} signal and a buffer–filter. As shown in Fig. 3, the hold and boost functions are embedded in the demodulator by replacing multiplier M_2 of Fig. 1 with two DTPA circuits and two controlling switches. The duty cycle of D_{CLK} is made less than the duty cycle of C_{CLK}. This clocking scheme avoids the spikes by sampling the signal when switching transients are exhausted.

During the phase when $SFC_1 = 1$, the input is tracked on the MOSCAP. When SFC_1 goes to logic 0, $DTPA_1$ is switched to boost phase. The bubble on the switch in Fig. 3 indicates inverted operation. The bubbled switch conducts when gate voltage is zero. When SFC_2 becomes logic 1 in the next half cycle of C_{CLK}, the boosted output is fed to the input of buffer-filter. In the first C_{CLK} half cycle, if $DTPA_1$ is in the track mode, then $DTPA_2$ (working in the boost phase) is connected to the buffer-filter input and vice-versa for the next C_{CLK} half cycle. Since the amplified chopped signals change sign after each $\frac{T_{CHOP}}{2}$, the DTPA demodulator recovers the original signal in the form of stair case waveform. If C_{gp} is a parasitic capacitance associated with the gate of MOSCAP and C_{ox} is the gate-oxide capacitance, then the boost factor, $\frac{C_{ox}+C_{gp}}{C_{gb}+C_{gp}}$ corresponds to the gain provided by the DTPA while demodulating the input signal.

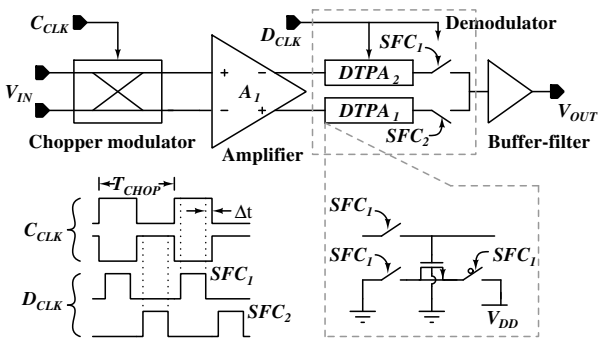

Fig. 3. Chopper stabilized amplifier with DTPA demodulator, switching scheme and clock timing diagram.

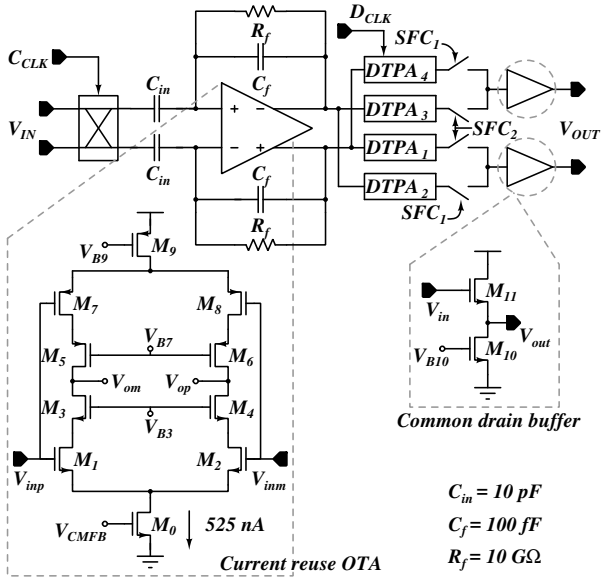

Fig. 4. Circuit implementation of the Chopper – DTPA amplifier (Bias and CMFB circuitry are not shown here).

IV. The Circuit Implementation

Fig. 4 shows the complete architecture of fully differential chopper – DTPA amplifier. Four DTPA circuits are used to recover both positive and negative signals at the output. The amplifier A_1 in Fig. 3 is designed to be a capacitively coupled amplifier where the closed loop gain is defined by ratio of the input capacitance to the feedback capacitance.

As shown in Fig. 4, the core operational transconductance amplifier (OTA) is realised using a telescopic cascode topology. A current reuse technique is implemented by utilizing both pMOS and nMOS as input transistors [13], [14]. Use of complementary input pair transistors increases the transconductance of the OTA, thereby enhancing the bandwidth and improving the noise performance. Assuming $g_{m3} \cdot r_{o3}$ and $g_{m5} \cdot r_{o5}$ to be > 1, the output thermal noise current of the current reused OTA can be approximated as:

$$i_{o,n}^2 \approx \frac{16KT}{3}(g_{m1} + g_{m7}), \tag{1}$$

where, g_{mi} and r_{oi} are the transconductance and the output resistance of the i^{th} transistor, K is the Boltzmann constant and T is the temperature. Using Eq. 1, the input-referred thermal noise voltage of the OTA can be calculated as:

$$v_{n,th}^2 = \frac{16KT}{3(g_{m1} + g_{m7})} \cdot \Delta f. \tag{2}$$

Similar analysis for flicker noise yields input-referred $1/f$ noise voltage to be

$$v_{n,1/f}^2 = \frac{2}{C_{ox}\Delta f(g_{m1} + g_{m7})^2}\left(\frac{K_n g_{m1}^2}{(WL)_1} + \frac{K_p g_{m7}^2}{(WL)_7}\right), \tag{3}$$

where, K_n and K_p represent the flicker noise constants of nMOS and pMOS respectively and C_{ox} is the gate-oxide capacitance. If we assume $g_{m1} = g_{m7}$, then current-reuse

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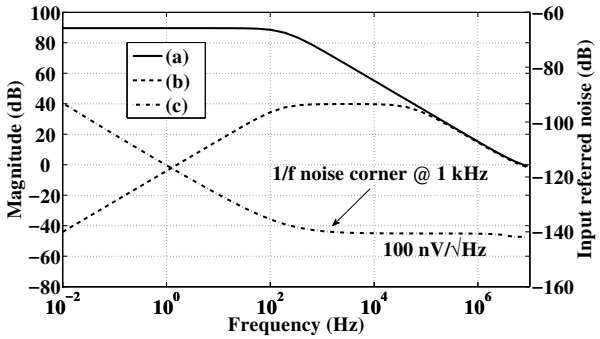

Fig. 5. AC magnitude and noise analysis: (a) open loop gain of the current reuse OTA, (b) closed loop gain of the AC coupled amplifier in Fig. 4, (c) input referred noise density of the OTA.

technique effectively reduces the input-referred noise by a factor of 0.707 while consuming same current.

Noise Analysis of the DTPA Demodulator: Ideally, the parametric amplification is a noise free process. In a way, a stand-alone DTPA achieves amplification without degrading the signal-to-noise-ratio (SNR) [10]. However, the T/H process inherently involved in the DPTA demodulator introduces switching noise. The noise power spectral density (PSD) transfer function of a T/H circuit can be found for a frequency range of interest: $0 < f < \frac{f_{CHOP}}{2}$ [8]. The PSD for an input spectrum bandwidth B is given by:

$$\left[\frac{\eta_o}{\eta_i}\right]_{f<\frac{f_{CHOP}}{2}} = d^2\left[1+2\sum_{n-1}^{h} sinc^2(n\cdot d)\right] + (1-d^2)(1+2h)sinc^2\left[(1-d)\frac{f}{f_{CHOP}}\right], \quad (4)$$

where, η_o and η_i are output and input noise PSDs, d is duty cycle of the DTPA clock, $f_{CHOP} = 1/T_{CHOP}$ is chopping frequency and h is the nearest integer to B/f_{CHOP}. For worst case scenario when $f = 0$, it can be noted that the noise increases as h increases and it is maximum for $d = 0$.

In case of DTPA based demodulator of Fig. 3, the two DTPAs receive same but inverted polarity noise voltages. At the output of demodulator, noise outputs of two DTPAs are added together. For $f \ll f_{CHOP}$, the DTPA outputs are correlated and noise cancel each other. Whereas for $f \geq f_{CHOP}$, the DTPA outputs are uncorrelated and their PSDs are summed at the buffer input. Therefore, for $f \geq f_{CHOP}$, the noise power increases by 3 dB because of the folding of noise into the signal band.

The above analysis can be used as a starting point for designing the OTA of Fig. 4. The OTA is biased in subthreshold region to obtain higher transconductance at reduced power dissipation. Operating at 525 nA current, the transconductances $g_{m1,2}$ and $g_{m7,8}$ obtained are 6.9 μS and 6.7 μS respectively. The simulated AC magnitude and noise response of the OTA are shown in Fig. 5. The achieved open loop gain and the unity gain bandwidth of the OTA are 90 dB and 9 MHz respectively. The OTA has thermal noise density of -140 dB

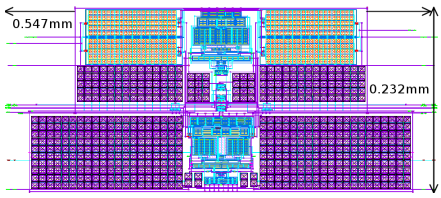

Fig. 6. Layout of the Chopper – DTPA amplifier.

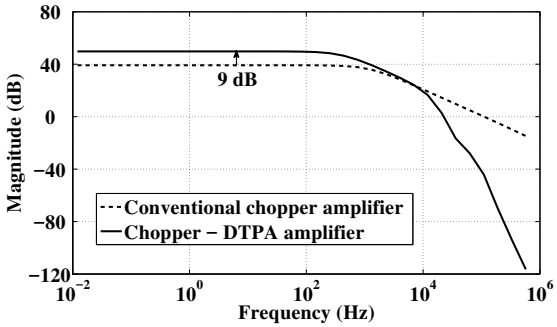

Fig. 7. AC response depicting gain augmentation during signal demodulation.

and flicker noise corner at 1 kHz frequency. The bandpass response of the designed capacitively coupled amplifier is also shown in Fig. 5. The input and feedback capacitance (MIM cap) of 10 pF and 100 fF are used to obtain closed loop gain of 40 dB. In this design, the chopping frequency is chosen as 10 kHz by considering the trade-off between the flicker noise corner of the OTA, the input impedance and -3 dB bandwidth of the AC coupled amplifier and the power consumption specifications.

V. The Post-Layout Simulation Results

The amplifier in Fig. 4 is implemented in a standard 180 nm CMOS process. The layout of the complete design is shown in Fig. 6. The core circuit occupies 0.12 mm^2 area of the chip.

The amplifier design has been verified with post-layout periodic steady state, periodic AC and periodic noise analyses. Furthermore, the analyses are performed using similar environment except for a change in the demodulation mechanism. First, a conventional chopper demodulator is used after the capacitively coupled amplifier and next, the chopper demodulator is replaced with the proposed DTPA demodulator. As depicted in Fig. 7, overall gain of the DTPA based amplifier is 49 dB whereas the gain of conventional chopper amplifier is 40 dB. Additional 9 dB gain is provided by the buffered DTPA demodulator. The -3 dB bandwidth of the amplifier is 400 Hz with 10 pF load capacitance. A 100-run statistical mismatch (Monte Carlo) analysis is performed to calculate CMRR and PSRR. The mean values of the CMRR and PSRR at 50 Hz frequency are found to be 108 dB and 78 dB respectively.

Fig. 8 shows the result of transient analysis for a 1 mV and 100 Hz differential input signal. The amplitude of demodulated and buffered signal is 290 mV. As seen from the inset shown in

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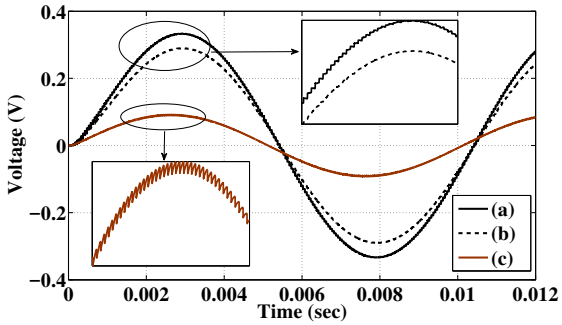


Fig. 8. Time response at various locations of the amplifier signal processing chain: (a) signal down converted by the DTPA demodulator, (b) common drain buffer output, (c) output with conventional chopper demodulator.

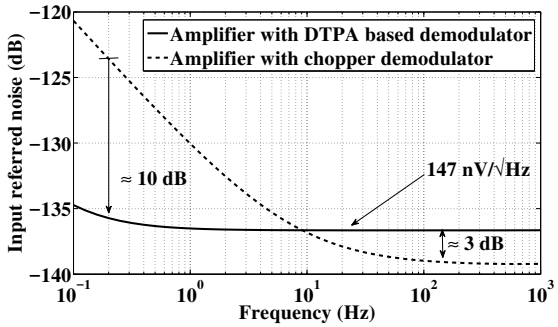
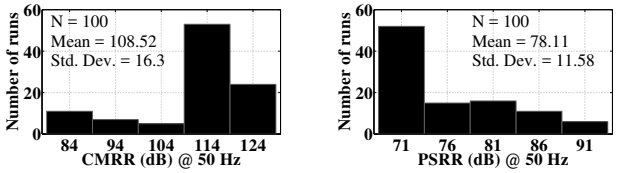


Fig. 9. Input referred noise spectral density of the amplifier.

Fig.8, with chopper demodulator the amplified output consists of chopping spikes. Additional spike nullifying circuitry or ripple rejection loop is required to recover clean signal at the output. On the other hand, because the output of DTPA demodulator is a stair case waveform, post demodulation filtering process reduces to a great extent. A first order low pass filer is sufficient to obtain clean signal at the output.

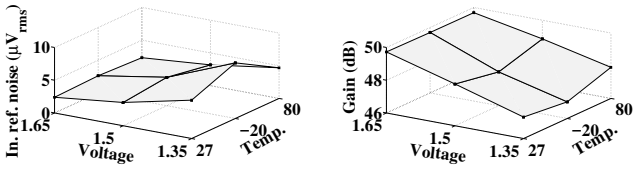
Fig. 9 shows the noise spectral density at the input of amplifier. The proposed amplifier consumes 1.02 μA DC current from a 1.5 V supply voltage and achieves input noise density of -136.7 dB. The noise efficiency factor (NEF) [15] of the amplifer is 5.4. As expected from the analysis in Sec. IV, the low frequency noise in the DTPA based amplifier reduces to a great extent (by ≈10 dB) because of implicit cancellation of correlated noise samples. Although the noise density in the DTPA based amplifier is more by 3 dB than the thermal noise density of conventional chopper amplifier, the signal in the band of interest gets amplified by additional 9 dB; prevailing the noise.

PVT worst case: Noise is one of the paramount specifications in low frequency domain and is expected to change with variations in V_{DD} and temperature. The functionality of the proposed design has been verified at 135 PVT corners. SS corner where both nMOS and pMOS are slow, at 1.35 V and -20°C shows the worst performance. At this corner g_m drops significantly because of reduction in the bias current. The input referred noise voltage and the closed loop gain at SS corner



(a) (b)

Fig. 10. Monte Carlo analysis for CMRR and PSRR of the amplifier.



(a) (b)

Fig. 11. Input referred noise voltage and gain of the amplifier at SS corner for -20°C to 80°C temperature with V_{DD} varying from 1.35 V to 1.65 V.

TABLE I
PERFORMANCE COMPARISON.

Reference	[3]	[5]	[7]	[16]	This Work	
					Typ	Worst⋆
Tech (nm)	180	180	180-500	180	180	180
V_{DD} (V)	1.2	1.8	1.8-5	1	1.5	1.35
Current (μA)	1.1	14.5	12.8	0.3	1	0.2
f_{chop} (kHz)	2	10	500	-	10	10
Gain (dB)	40	40	60	20-60	49	46
Noise (μV_{rms}) (BW in Hz)	0.7 (100)	3.7 (2k)	37† (DC)	6 (250)	2.9 (400)	8.5 (145)
NEF	2.83	-	5.5	3.3	5.4	8.7
CMRR (dB)	110	120	124	75	108	102
PSRR (dB)	105	-	120	77	78	65

⋆ SS, 1.35 V and - 20°C corner, † (nV/$\sqrt{}$Hz)

for -20°C to 80°C with V_{DD} varying from 1.35 V to 1.65 V are plotted in Fig. 11. Table 1 compares performance of the proposed amplifier with its counterparts in the literature.

VI. CONCLUSIONS

The chopper stabilized amplifier which uses a discrete time parametric amplifier (DTPA) for demodulation is described. The DTPA performs spur free down conversion of modulated signal without requiring any additional spike filtering circuit. Improvement in gain of the amplifier is achieved by replacing the chopper demodulator with the DTPA demodulator circuit. Evaluated NEF of 5.4 over 400 Hz bandwidth makes this amplifier suitable for low power and low bandwidth micro-sensing applications. Usability of the design can be further extended to biomedical applications by employing DC servo and impedance boosting loops.

ACKNOWLEDGMENT

The authors would like to thank MeitY, Govt. of India for supporting the work through SMDP-C2SD project.

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