Facile DUV Irradiated Solution-Processed ZrO_2/In_2O_3 for Low Voltages FET Applications

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***Abstract*— Prime challenges for device integration in metal–oxide semiconductors are low voltage operations, low thermal budget, and large area stable thin films for high-performance field-effect transistors (FETs). Although more, high equipment costs and device scalability issues remain challenges with thin film processing. Henceforth, here we present fully solution-processed thin indium oxide (In_2O_3) (E_g ~ 3.2 eV) semiconducting film integrated with high-κ (~14.68) ZrO_2 dielectric thin film for high-performance FETs. Top gate bottom contact (TGBC) architecture is optimized for driving low voltage operations, whereas a low thermal budget (<300 °C) has been made possible with (~1 min) facile deep-ultraviolet (DUV) (~254 nm) irradiation. Al/ZrO_2/In_2O_3/Pt/SiO_2/Si FETs operate well below (~0.5 V), with a high I_{ON}/I_{OFF} ratio (~1.1×10^4), low subthreshold swing (SS) (~104 mV/dec), threshold voltage (~−0.3 V), transconductance (~1.44 μs @ 0.5 V), respectively. The effective field-effect mobility in the linear region is ~44.2 cm^2/Vs at $V_{DS} = 0.1$ V, and in the saturation region is ~15.0 cm^2/Vs at $V_{DS} = 0.5$ V, respectively. The interface trap density ~2.5×10^{12}/eV cm^2 for ZrO_2/In_2O_3 was investigated by conductance (G-V) technique, also electrical stress investigations were performed for reliability analysis. The gate leakage current is ~7.05 nA/cm^2 at $V_{GS} = 1$ V. This work demonstrates the high performance of DUV irradiated solution processed Al/ZrO_2/In_2O_3/Pt thin-film transistor (TFT) structures.**

***Index Terms*— Deep-ultraviolet (DUV) irradiation, field-effect transistors (FETs), indium oxide (In_2O_3), low temperature, low voltage, solution-processed, zirconium oxide (ZrO_2).**

I. Introduction

THE foremost challenges to next-generation metal-insulator-semiconductor field-effect transistors (MIS-FETs) are complementary metal–oxide-semiconductor (CMOS) compatibility, device stability, reliability, lower operating voltages, scalability, costly fabrication/deposition processes, interfacial defects, and substrates inflexibility etc., [1], [2], [3]. Metal–oxide-semiconductors integrated with compatible high-κ dielectrics have been extensively studied in the past few years for applications in thin-film transistors (TFTs), flexible technology, active matrix light-emitting diode (LED) displays, gas/biosensors, etc., [4]. Metal–oxide semiconductors, including transition metal oxides (TiO_2, Cu_2O, WO_3, ZnO) and post-transition metal oxides (SnO_2, Ga_2O_3, In_2O_3) semiconductor offer wider bandgaps, diverse doping profiles, higher electron mobilities as compared with counterparts amorphous-Si etc., [5]. Among all, n-type indium oxide (In_2O_3) semiconductor is superior as compared to counterparts considering tunable wider band gap (WBG) (~2.1–4.5 eV), higher electron mobilities (~10–50 cm^2/V.s), higher degenerate doping density [6], used in flexible display, TFT technology, deep-ultraviolet (DUV) (λ ranging 200–280 nm) detection, etc., [7]. Careful controlling the charge carriers and stoichiometry of the indium and oxygen, including oxygen vacancies and indium interstitials, yields semiconducting In_2O_3. On the contrary, the choice of process and dielectric material for WBG decides the surface/interface properties critical for better gate control and enhanced mobilities. Metal–oxide dielectrics such as Al_2O_3, HfO_2, ZrO_2, Ta_2O_5, and La_2O_3 offer transistor scaling and lower leakage currents; however, field-effect transistors (FETs) also require low defect density, high interface compatibility, lower thermal budget, and thermodynamic stability, which are the foremost criteria in the preselection of the suitable contender [8]. High (κ ~ 25) zirconium oxide (ZrO_2) forms a thermodynamically superior interface with In_2O_3, providing lower leakage current density, higher mobility, reduced interface traps, and lesser defects/oxide charges [9]. Nevertheless, the requisite for costly vacuum equipment and expensive deposition technologies such as sputtering, atomic layer deposition (ALD), molecular beam epitaxy (MBE), and thermal evaporation for metal oxides pose a severe challenge to device technologies scalability and cost-effective bulk production [10]. Solution-processed semiconductors and compatible high-κ dielectric thin-films are excellent alternatives for scalable, eco-friendly, low-cost deposition techniques; however, they possess the challenge

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of fabricating stable, large-area, oxygen vacancy defects-free thin-films [11], [12], [13], [14]. Solution-processed metal–oxide thin films look forward to low-temperature annealing with the help of combustion additives, aging, DUV irradiation, plasma exposure, flash lamp annealing, high-pressure annealing, etc., [15], [16], [17], [18]. Among all, surface passivation DUV irradiation is a reliable tool for depositing enhanced stability large-area thin films at much lower temperatures [19]. DUV exposure accelerates the conversion of metal-hydroxide (M-OH) bonds to metal-oxide-metal (M-O-M) bonds, thereby reducing oxygen vacancies/defects [20]. Bottom gate top contact (BGTC) transistor architecture faces limitations with high operating voltages and nonpassivation of the top layer; however, top gate bottom contact (TGBC) transistor architectures have fabrication difficulties with increased processing steps. For employing low operating voltages to the TGBC architecture, the quality of the semiconductor/dielectric interface and, interface trap charges are critical for transistor action [21]. Capacitance–voltage (C–V) and conductance-voltage (G–V) techniques are used for dielectric, interfacial study, and frequency dispersion related to interface traps [22], [23]. First, solution-processed metal-oxide-semiconductor In_2O_3 integrated with solution-processed high-κ dielectric ZrO_2 transistor structures have been fabricated, which employ low process temperatures (<300 °C) and achieve low operation voltages (0.5 V), contrary to high temperatures (>500 °C) and high voltages achieved (50–100 V) previously [24], [25], [26]. Also, facile DUV irradiation is used for ZrO_2 and In_2O_3 materials combined with TGBC transistor architecture along with the interfacial studies of ZrO_2/In_2O_3 stack through electrical and interfacial microscopy characterizations, such as interface trap state densities, mobile charge density, etc.

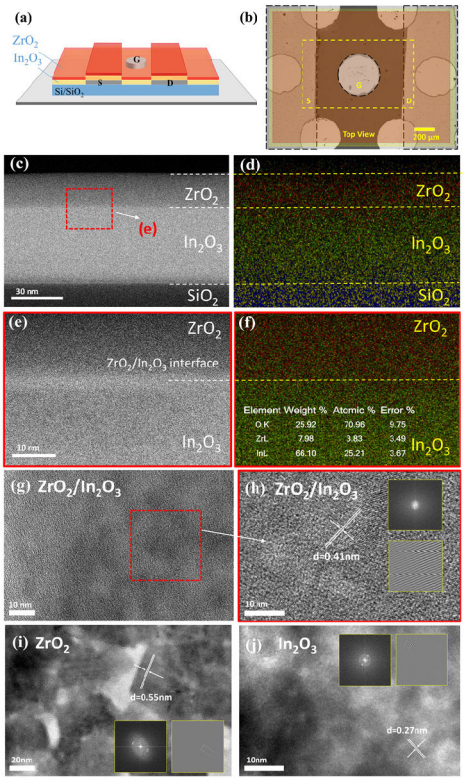

Fig. 1. (a) Fabrication schematic (not on scale). (b) Top view optical image of Al/ZrO_2/In_2O_3/Pt/SiO_2/Si TGBC FET structures gate length 850 μm (scale 200 μm). (c) Cross section FE-SEM of $ZrO_2/In_2O_3/SiO_2$ stack (30 nm scale). (d) Cross section EDX mapping of $ZrO_2/In_2O_3/SiO_2$ stack. (e) High-magnification micrograph cross section FE-SEM of ZrO_2/In_2O_3 interface (10 nm scale). (f) Cross section EDX mapping of ZrO_2/In_2O_3 interface (Inset: EDX elemental composition table). (g) HR-TEM image of ZrO_2/In_2O_3 stack thin films (10 nm scale). (h) High-resolution HR-TEM image of ZrO_2/In_2O_3 stack thin films (10 nm scale) with d-spacing, FFT and IFFT. (i) HR-TEM image of ZrO_2 material (20 nm scale) with d-spacing, FFT and IFFT. (j) HR-TEM image of In_2O_3 material (10 nm scale) with d-spacing, FFT and IFFT.

II. Experiment

TGBC FET architecture onto SiO_2/Si substrates containing metal-oxide In_2O_3 as semiconducting channel layer integrated with high-κ ZrO_2 dielectric has been fabricated, as shown in Fig. 1(a). Fig. 1(b) shows the top-view optical image of one of the many fabricated Al/ZrO_2/In_2O_3/Pt/SiO_2/Si structures (scale 200 μm).

Cross-sectional field-emission scanning electron microscopy (FE-SEM) is conducted with Zeiss GeminiSEM 500, and the image for $ZrO_2/In_2O_3/SiO_2$ stack films is displayed in Fig. 1(c) with the scale of 30 nm identified distinctly by different contrast values. The corresponding cross-sectional energy dispersive X-ray (EDX) mapping is analyzed with SEM in-built EDX for $ZrO_2/In_2O_3/SiO_2$ stack films displayed by discrete regions of ZrO_2 (red), In_2O_3 (green), and SiO_2 (blue), as shown in Fig. 1(d). A high magnification micrograph for cross section FE-SEM of ZrO_2/In_2O_3 interface (10 nm scale) is shown in Fig. 1(e), with the area mapped (red box) in Fig. 1(c). The corresponding cross-section EDX mapping of the ZrO_2(red)/In_2O_3(green) interface is shown in Fig. 1(f) with (Inset) EDX computed elemental composition table. Fig. 1(g) shows the atomic view of ZrO_2/In_2O_3 stack thin films with the high-resolution transmission electron microscope (HR-TEM) image (10 nm scale) with Tecnai G 2 20 S-TWIN HR-TEM. Fig. 1(g) reveals large area fringes with identifiable polycrystalline planes, revealing the formation of uniform ZrO_2/In_2O_3 stack thin films. Fig. 1(h) shows the magnified HR-TEM image of ZrO_2/In_2O_3 stack thin films (10 nm scale) with d-spacing = 0.41 nm, fast Fourier transformation (FFT) and inverse FFT (IFFT) images corresponding to the area mapped (red box) in Fig. 1(g). The HR-TEM images of ZrO_2 (scale = 20 nm) and In_2O_3 (scale = 10 nm) materials are shown in Fig. 1(i) and (j), revealing polycrystalline systems with corresponding d-spacing = 0.55 and 0.27 nm, FFT and IFFT images, respectively.

First, indium (III) nitrate hydrate is mixed with 2-methoxyethanol to form a 0.4 M solution A. Nitrate-based indium precursor is preferred due to high ultra-violet absorption and lower decomposition temperature. After that, 100 μL ethylene glycol is added dropwise to solution A. The solution is heated at 50 °C with vigorous mixing at 900 rpm/min for 60 min, and then aged for 24 h. Likewise, Zirconium (IV) chloride is mixed with 2-methoxyethanol to form 0.5 M homogeneous solution B. The solution is heated at 50 °C with 900 rpm/min for 60 min, then aged for 24 h.

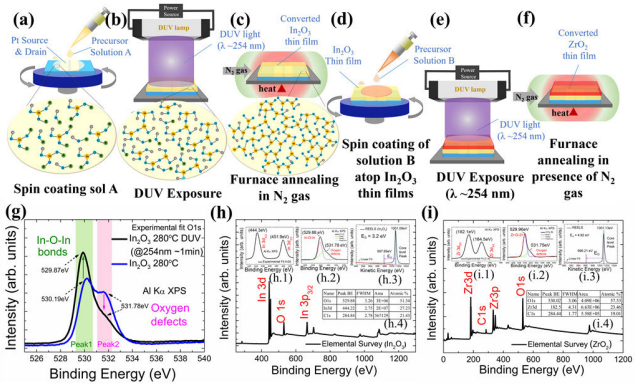

Fig. 2. Fabrication process flow of Al/ZrO_2/In_2O_3/Pt/SiO_2/Si FETs. (a) Spin coating of Sol A. (b) DUV exposure of Sol A films. (c) Furnace annealing In_2O_3 films. (d) Spin coating Sol B atop In_2O_3 thin films. (e) DUV exposure of Sol B films. (f) Furnace annealing ZrO_2 films. (g) O1s experimental fit for In_2O_3 films with (black) and without (blue) facile DUV (~1 min) irradiation. (h) XPS elemental survey of In_2O_3 thin films (h.1) In3d experimental fit, (h.2) O1s concentration, (h.3) REELS of In_2O_3 thin films, and (h.4) XPS peaks data of In_2O_3 thin films. (i) XPS elemental survey of ZrO_2 thin films (i.1) Zr3d experimental fit, (i.2) O1s concentration, (i.3) REELS of ZrO_2 thin films, and (i.4) XPS peaks data of ZrO_2 thin films.

The solutions A and B are filtered with a 0.22 μm syringe before spin coating. RCA-cleaned p-type (100) device-grade silicon wafers (300 μm, 2–10 Ω-cm resistivity) are used to fabricate the MIS-FET structures in a class 100 cleanroom facility. For SiO_2 growth, wafers are heated at 500 °C, 8 °C/min for 60 min in an inert environment, then 900 °C, 6 °C/min for 60 min in an oxygen-rich environment and finally 1060 °C with 2 °C/min for 3 h in an oxygen-rich environment in Thermo scientific three-zone furnace, later cooled naturally. The thickness of grown SiO_2 ~225 nm is measured through an Accurion EP4 ellipsometer. RCA-cleaned SiO_2/Si substrates are used to coat platinum ~40 nm with sputtering to form source and drain (L = 850 μm, W = 1100 μm) contacts through shadow masking. Samples are kept in an ultra-violet (UV) ozone system for ~30 min to remove organic impurities. Fig. 2(a) shows 40 μL of solution A is spin coated on Pt/SiO_2/Si/ substrates at 3000 r/min for 45 s with an angular velocity of 1000 r/min to form large-area thin films consisting of indium hydroxide and methoxide complexes. The spin-coated films are dried on the hot plate at 140 °C for ~10 min to evaporate the solvent. A portion of the coated film is then etched with 1% oxalic acid using dip-coating for 10 s, to reveal bottom Pt contact electrodes [27]. Fig. 2(b) shows the samples are exposed to DUV (~254 nm) for 1 min in air without any heat treatment as surface passivation. Facile (~1 min) DUV irradiation treatment is optimized to partially trigger In-O-In condensation and densification at a much lower thermal budget by the removal of hydroxyl and organic groups [28]. Thereafter, samples are immediately transferred to the three-zone furnace for two-step annealing procedure in N_2 ambient, as shown in Fig. 2(c). The films are heated to 140 °C, and 280 °C at a ramp rate of 10 °C/min with a hold time of 30 min and 1 h 30 min, respectively, to completely transform into In_2O_3 films. In_2O_3 thin films are allowed to cool naturally to room temperature. Likewise, Fig. 2(d) shows 40 μL of solution B is spin-coated on In_2O_3/Pt/SiO_2/Si/ substrates at 3000 r/min for 45 s with an angular velocity of 1000 r/min to form large-area thin films. The spin-coated films are dried on the hot plate at 140 °C for ~10 min, and a portion of the coated films is etched with 1% HF solution using dip-coating for 4 s to reveal the bottom Pt contact electrodes. Fig. 2(e) shows the samples are exposed to DUV (~254 nm) for 1 min and immediately transferred to the 3-zone furnace for a two-step annealing procedure in N_2 ambient. The films were heated to 200 °C and 300 °C with ramp and hold times of 6 °C/min, 30 min, and 10 °C/min, 1 h 30 min, as shown in Fig. 2(f), respectively. Thereafter, ZrO_2 thin films were cooled naturally to room temperature.

Fig. 2(g) shows the X-ray photoelectron spectroscopy (XPS) experimental fit of O1s for In_2O_3 thin films with (black curve) and without (blue curve) DUV (~254 nm, ~1 min) irradiation treatment with corresponding peaks at (529.87, 531.78 eV) and (530.19, 531.78 eV), respectively, with Thermo scientific NEXSA Surface Analysis. The shift of XPS O1s peak of DUV-treated In_2O_3 films from 530.19 to 529.87 eV toward lower binding energies indicates maximum conversions of hydroxyl In-OH and methoxide groups into In-O-In bond formation. Also, the reduction of peak intensity with DUV irradiation treatment at 531.78 eV reveals a reduction in oxygen vacancy/defects due to sparse ionized irradiation. This indicates that DUV irradiation treatment promotes the formation of defect-free In_2O_3 large-area thin films at much lower temperatures. Hence, facile DUV irradiated solution-processed In_2O_3 can be regarded as a promising candidate for fabricating high-performance FETs at low temperatures. Thereafter, the elemental composition of fabricated In_2O_3 and ZrO_2 thin films is verified through XPS survey analysis. Fig. 2(h) shows the elemental survey of In_2O_3 thin films consisting of O1s, In 3d, and In $3p_{3/2}$ peaks. Here, indium and oxygen peaks are visible at binding energies of 444.3, and 529.88 eV, respectively. Fig. 2(h.1) shows In $3d_{3/2}$ and In $3d_{5/2}$ at 451.9 and 444.3 eV experimental fit peaks, respectively. Fig. 2(h.2) shows the O1s peak fit in In_2O_3 thin films, where, 529.88 and 531.78 eV peaks are present. But, the In-O peak at 529.88 eV is much higher than the 531.78 eV peak. It indicates that most of the In-OH bonds have been successfully converted to In-O bonds, favoring the formation of high-quality, large-area In_2O_3 thin films. Indium oxide can be tuned as an insulator, semiconductor, or metallic nature by controlling the indium and oxygen stoichiometry, including oxygen vacancies and indium interstitials. The oxygen-deficient form of $In_2O_{3-\delta}$ is a n-type semiconductor [29]. Therefore, the fabricated In_2O_3 thin films with some oxygen vacancies/defects are semiconducting in nature. Fig. 2(h.3) shows the reflection electron energy loss spectroscopy (REELS) analysis for In_2O_3 thin films, from which the electronic bandgap of In_2O_3 is obtained to be (E_g ~ 3.2 eV) [30]. Fig. 2(h.4) shows XPS peak tables with Binding Energy, full-width half maxima (FWHM), area, and atomic percentage of In_2O_3 thin films. Fig. 2(i) shows the elemental survey of ZrO_2 thin films consisting of Zr 3d, Zr 3p, O1s, and C1s peaks. Here, zirconium, oxygen, and carbon peaks are visible at binding energies of 182.5,

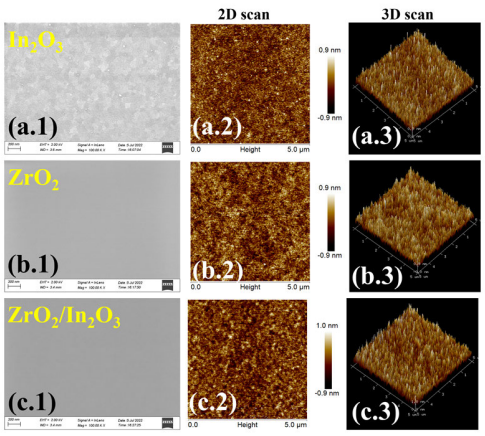

Fig. 3. (a.1)–(c.1) FE-SEM images at 200 nm scale bar. (a.2)–(c.2) Two-dimensional AFM topography images. (a.3)–(c.3) Three-dimensional AFM topography images at 25 μm^2 scanning area for (a) In_2O_3 thin films, (b) ZrO_2 thin films, and (c) ZrO_2/In_2O_3 stack thin films.

529.96, and 284.44 eV, respectively. Fig. 2(i.1) shows the Zr $3d_{3/2}$ and Zr $3d_{5/2}$ peaks at 184.5 and 182.1 eV, respectively. Fig. 2(i.2) shows O1 experimental fit at 529.96 and 531.75 eV peaks, with a prominent peak at 529.96 eV revealing clear O-Zr-O bond formation. Fig. 2(i.3) shows the REELS analysis of ZrO_2 thin film, deriving electronic bandgap to be ($E_g \sim$ 4.92 eV). Fig. 2(i.4) shows XPS peak tables with binding energy, FWHM, area, and atomic percentage of ZrO_2 thin films.

Furthermore, FE-SEM and 2-D and 3-D atomic force microscopy (AFM) is carried out for In_2O_3, ZrO_2, ZrO_2/In_2O_3 stack films with Zeiss GeminiSEM 500 and Bruker Dimension icon AFM, as shown in Fig. 3(a)–(c), respectively. FE-SEM image of In_2O_3, ZrO_2, ZrO_2/In_2O_3 stack films at 200 nm scale bar confirms the formation of highly uniform thin films, as shown in Fig. 3(a.1)–(c.1), respectively.

Correspondingly, 2-D and 3-D AFM images of In_2O_3, ZrO_2, and ZrO_2/In_2O_3 stack films are carried out in 25-μm^2 scanning area, depicting very uniform films with low roughness of $\sim$(2.0 $\pm$ 1.6 nm), $\sim$(1.0 $\pm$ 0.9 nm) and $\sim$(2.2 $\pm$ 1.8 nm), as shown in Fig. 3(a.2-3)–(c.2-3), respectively. These results conclude that the fabricated solution-processed thin films are highly uniform and smooth, which is attributed to low interface trap state density at channel layer In_2O_3 and dielectric ZrO_2 gate-stack. This will positively lead to high-performance stable FETs with higher effective mobilities and smaller sub-threshold swing values. The thickness of thin films In_2O_3 ($\sim$40 nm) and ZrO_2 ($\sim$25 nm) is measured through the Accurion EP4 ellipsometer. Top gate aluminum $\sim$40-nm circular electrodes are deposited through thermal evaporation and shadow masking. For the array of gate electrodes, the average area of the gate electrodes is measured to be $\sim 2.6 \times 10^{-3}$ cm^2. For electrical characterizations, fabricated $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ FET devices are characterized with a compatible prober system attached to Keithey 4200 SCS.

III. Results and Discussion

The drain current versus drain-to-source voltage (I_D–V_{DS}) output characteristics of solution-processed indium oxide

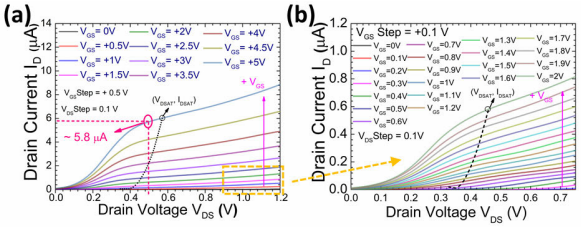

Fig. 4. (I_D–V_{DS}) Output characteristics of $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures (a) V_{GS} 0 to 5 V, V_{GS} step = +0.5 V & V_{DS} step = 0.1 V (b) V_{GS} 0 to 2 V, V_{GS} step = +0.1 V & V_{DS} step = 0.1 V.

(In_2O_3) as a semiconducting channel integrated with solution-processed zirconium dioxide (ZrO_2) as high-κ gate dielectric for $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures is shown in Fig. 4(a) and (b). Fig. 4(a) shows drain-to-source voltage sweep from 0 to +1.2 V and gate-to-source voltage (V_{GS}) sweep from 0 V to +5 V, with a step of +0.5 V. With increasing $+V_{GS}$ voltage, the drain current increases, corresponding to n-channel MISFET operation with clear pinch-off and current saturation. Drain current increases linearly sub 0.5 V V_{DS}; thereafter, becomes independent of V_{DS} and saturates. At an operating point, +0.5 V V_{DS}, the value of the drain current is measured as $\sim$5.8 μA. The low operating voltages originating from TGBC architecture FETs indicate the formation of an excellent defect-free ZrO_2/In_2O_3 gate-stack. This makes them an ideal choice for wearable and flexible electronics; Internet-of-things (IoTs), and edge computing, which require autonomous power sources. Fig. 4(b) shows the magnified (I_D–V_{DS}) characteristics with V_{GS} sweep from 0 to +2 V, with a smaller V_{GS} step +0.1 V voltage. It can be observed that even with such smaller voltage steps, +0.1 V V_{GS} the drain current sweeps are highly distinguishable and increase linearly. It indicates a highly precise gate control of solution-processed high-κ ZrO_2 gate dielectric over inversion charges proportional to drain current in the solution-processed In_2O_3 channel. This reveals the formation of defect-free In_2O_3 and ZrO_2 thin films and excellent interface ZrO_2/In_2O_3 stack for high-performance $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures.

TGBC transistor architecture is essential for providing low operating voltages, such as V_{DS} = 0.5 V, as the back gate is replaced with a much smaller patterned top gate. TGBC architecture also provides necessary passivation to the underlying solution-processed In_2O_3 semiconductor layer against oxygen free radicals adsorption at the surface in exposure to ambient air. This passivation provides the required stability to the In_2O_3 thin films apart from the stability provided by facile sparse ionized DUV exposure for fabricating defect-free thin films. Facile ($\sim$1 min) DUV ($\sim$254 nm) irradiation triggers the breaking of In-OH and complexes into O-In-O bonds at much lower temperatures, thus providing stability to long chain large-area In_2O_3 thin films at much lower ($\sim$280 °C) process temperatures. Thereafter, thermal annealing in an inert environment (N_2) preserves the O-In-O bond formations and passivates the oxygen vacancies into long-chain defect-free In_2O_3 thin films. Low processing temperatures make fabricated $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures suitable for flexible electronics. Indium oxide In_2O_3 thin films are

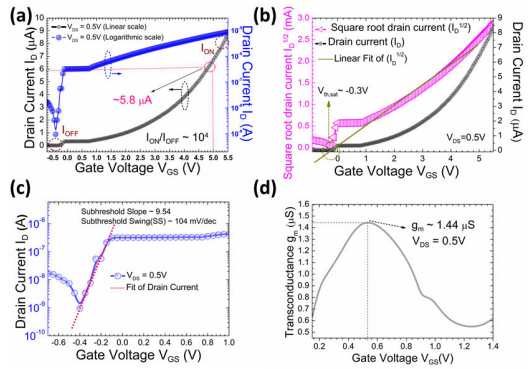

Fig. 5. (a) (I_D–V_{GS}) Transfer characteristics (linear and logarithmic scale), V_{GS} sweep from −1 to +5.5 V and V_{DS} = 0.5 V. (b) Threshold voltage measurements from $I_D^{1/2}$–V_{GS} curve (V_{DS} = 0.5 V). (c) Subthreshold Swing measurements from I_D–V_{GS} curve (d) Transconductance g_m versus V_{GS} from I_D–V_{GS} curve of Al/ZrO_2/In_2O_3/Pt/SiO_2/Si structures.

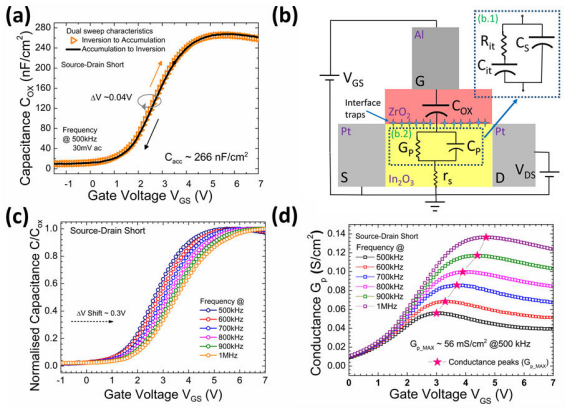

Fig. 6. (a) Dual sweep gate capacitance-voltage (C_{OX}–V_{GS}) characteristics at 500 kHz. (b) Equivalent electric circuit representing oxide capacitance, parallel conductance, parallel capacitance, and series resistance. (c) Normalized capacitance-voltage (C/C_{OX}–V_{GS}) characteristics at 500–1000 kHz, step 100 kHz. (d) Conductance-voltage (G_p–V_{GS}) characteristics at 500–1000 kHz, step 100 kHz for Al/ZrO_2/In_2O_3/Pt/SiO_2/Si structures.

a special courtesy due to tunable electrical properties with adjustable oxygen vacancies. Oxygen vacancy-free In_2O_3 films are highly conducting; hence, defects are also introduced with facile sparse ionized DUV irradiation along with N_2 thermal annealing to achieve semiconducting properties. Uniformity and low surface roughness of In_2O_3 and ZrO_2 thin films are partially attributed to additives of ethylene glycol in the solution-processed films. This justifies the formation of uniform defect-free semiconducting In_2O_3 and high-κ ZrO_2 thin films for Al/ZrO_2/In_2O_3/Pt/SiO_2/Si MISFETs.

A steep drain current versus gate-to-source voltage (I_D–V_{GS}) transfer characteristics of Al/ZrO_2/In_2O_3/Pt/SiO_2/Si structures are shown in Fig. 5(a). Fig. 5(a) measures drain current in linear (black) and logarithmic (blue) scales with V_{GS} sweep from −1 to +5.5 V and constant V_{DS} = 0.5 V operating voltage. Value of drain current is measured ~5.8 μA at V_{GS} = 5 V and V_{DS} = 0.5 V, which is consistent with drain current obtained from (I_D–V_{DS}) output characteristics in Fig. 4. On-current (I_{ON}) or conduction current (~8.6×10^{-6}) has been measured in saturation transistor region @ 5.5 V V_{GS} and OFF-current (I_{OFF}) (~7.4×10^{-10}) of devices have been measured in cut-off region @ −0.4 V V_{GS}. The measured devices exhibit a considerable drain current ON-to-OFF ratio (I_{ON}/I_{OFF}) ratio ~1.1×10^4, as shown in Fig. 5(a). A considerably high I_{ON}/I_{OFF} ratio indicates low power consumption due to excellent interface ZrO_2/In_2O_3 gate stacks and lower leakage currents owing to the formation of highly uniform ZrO_2 dielectric thin films.

The threshold voltage, below which devices cut-off, is measured ($V_{th,sat}$ ~ −0.3 V) at V_{DS} = 0.5 V in the saturation region, from $I_D^{1/2}$–V_{GS} transfer characteristics through its x-intercept, (linear fitting), as shown in Fig. 5(b) [31]. Negative threshold voltage is indicative of depletion mode operation in fabricated transistor structures. The subthreshold slope (~9.54) is measured from the I_D–V_{GS} transfer characteristics in the logarithmic scale, as shown in Fig. 5(c). The inverse of the subthreshold slope is the subthreshold swing (SS) calculated to be (~104 mV/dec). A low SS magnitude is indicative of the superior ability of ZrO_2 gate voltage to control charge carriers in In_2O_3. It indicates a smooth defect-free ZrO_2/In_2O_3 interface and the formation of excellent uniform In_2O_3 and ZrO_2 thin films suitable for high-speed devices. Hence, fabricated cost-effective transistors can be used for low power consumption and high operation speed flexible applications owing to decent I_{ON}/I_{OFF} ratio, $V_{th,sat}$, and SS.

Transconductance versus gate-to-source voltage curve results from the derivative of I_D–V_{GS} transfer characteristics at 0.5 V V_{DS}, as shown in Fig. 5(d). Gate transconductance (g_m) is defined using equations

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}} \quad (1)$$

where I_D is drain current, V_{GS} is gate-to-source voltage, and V_{DS} is drain-to-source voltage, respectively. Fig. 5(d) shows a peak value of transconductance as 1.44 μs at V_{GS} = 0.5 V. Higher transconductance value indicates better gate control by forming highly uniform defect-free ZrO_2 thin films. The higher transconductance is imperative for yielding higher mobilities for Al/ZrO_2/In_2O_3/Pt/SiO_2/Si structures.

Fig. 6(a) shows the dual sweep gate capacitance (C_{OX}) versus gate-to-source voltage (V_{GS}) characteristics, with V_{GS}, DC sweep from −1.5 to 7 V, superimpose with 30 mV, 500 kHz ac signal, for Al/ZrO_2/In_2O_3/Pt/SiO_2/Si structures with source and drain terminals shorted [31]. For an array of fabricated devices, the measured capacitance per unit area in the accumulation region C_{acc} is (~266 nF/cm^2) measured @ V_{GS} = 5 V, and 500 kHz frequency. The dielectric constant κ of solution-processed high-κ ZrO_2 is calculated as ~14.68 at 500 kHz, calculated by [31]

$$C_{OX} = \kappa \varepsilon_O \frac{A}{d} \quad (2)$$

where C_{ox} is oxide capacitance, κ is the dielectric constant, ε_o is absolute permittivity, A is capacitor area and d is oxide thickness, respectively. To understand the presence of effective oxide charges/oxygen vacancies in solution-processed ZrO_2, such as fixed oxide charges (Q_F), trapped

oxide charges (Q_{OT}), mobile ionic charges (Q_M) located at the ZrO_2/In_2O_3 interface, exhibited by bulk/deep-level traps, border/shallow traps, and interface traps, following study is conducted. Cyclic sweep from accumulation to inversion region (black) forward sweep and inversion to accumulation region (orange) reverse voltage sweep with $V_{GS} = -1.5$ to 7 V show a negligible change in voltage $\Delta V \sim 0.04$ V shift toward the left side (negative gate bias side). This negligible left-side shift in flat band voltage indicates the negligible presence of positive fixed oxide charges (Q_O) at or very near the ZrO_2/In_2O_3 interface. This implies an excellent interface at the ZrO_2/In_2O_3 stack and fewer oxygen vacancies/defects in the ZrO_2. This implies facile DUV- irradiated ZrO_2 films are uniform, and defect-free in nature.

Fig. 6(b) shows the electrical equivalent circuit of $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures. Solution-processed high-κ dielectric ZrO_2 is shown with an equivalent capacitance (C_{OX}). Solution-processed metal–oxide In_2O_3 semiconductor is shown in Fig. 6(b.1), equivalent to semiconductor capacitance (C_s) in parallel with interface trap capacitance (C_{it}) and interface trap resistance (R_{it}), respectively. (C_s), (C_{it}), and (R_{it}) be further simplified as parallel capacitance (C_p) and parallel conductance (G_p), as shown in Fig. 6(b.2) and given by the following relations:

$$C_p = C_s + \frac{C_{it}}{1 + (\omega R_{it} C_{it})^2} \tag{3}$$

$$G_p = \frac{\omega^2 R_{it} C_{it}^2}{q[1 + (\omega R_{it} C_{it})^2]} \tag{4}$$

where $\omega = 2\pi f$, f is the frequency, C_s is semiconductor capacitance, C_{it} is the interface trap capacitance, R_{it} is the interface trap resistance, and q is the electronic charge, respectively. Series resistance (r_s) may also be present in series with (C_P) and (G_P), which can cause errors in extracting interfacial properties, as shown in Fig. 6(b.2). (r_s) is to be eliminated with improved fabrication practices, measurements at low frequencies, and also by applying a series resistance correction to the measured admittance. (r_s) is determined by biasing $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures in strong accumulation region and is given by the following relations:

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{5}$$

where, C_{ma} and G_{ma} are the measured capacitance and the measured conductance in the strong accumulation region. After applying series resistance correction to (C_p) and (G_p) corrected capacitance (C_C) and corrected conductance (G_C) are obtained and given by the following relations [22]:

$$C_C = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{a^2 + \omega^2 C_m^2} \tag{6}$$

$$G_C = \frac{(G_m^2 + \omega^2 C_m^2) a}{a^2 + \omega^2 C_m^2}. \tag{7}$$

Here

$$a = G_m - (G_m^2 + \omega^2 C_m^2) r_s. \tag{8}$$

C_m and G_m are the measured capacitance and equivalent parallel conductance across the terminals of $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures, with source and drain shorted. $\omega = 2\pi f$, f is the frequency of interest, and r_s is the series resistance, respectively. To understand the frequency dependant electrical parameters such as interface state density and series resistance in ZrO_2, capacitance–voltage (C–V) and conductance-voltage (G–V) characteristics are measured at different frequencies using Nicollian and Goetzberger method [22]. The time taken for rearrangement of charges in the dielectric is known as dielectric relaxation time (τ_d). When carrier transient time is less than dielectric relaxation time or (τ_c) < (τ_d), space charge polarization is negligible [32]. Therefore, frequencies ranging from ~500 kHz to 1 MHz, are used for detecting the operating range of fabricated devices. Frequency dispersion may be caused by parasitic effects or series resistance (r_S), surface roughness, and interface traps (C_{it}, R_{it}). Fig. 6(c) shows the normalized series resistance corrected capacitance (C/C_{OX}) versus gate-to-source voltage V_{GS} curve, for 500–1000 kHz with a frequency step of 100 kHz, with source and drain terminals shorted for $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures. As the frequency increases from 500 to 1000 kHz, capacitance decreases with slight variations (266–222 nF/cm^2), respectively. This may be attributed to negligible series resistance effects in the accumulation region. Hence, series resistance corrected capacitance and conductance have been taken into account to minimize extrinsic frequency dispersion effects in $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures. As discussed previously, the surface roughness of In_2O_3, ZrO_2, and ZrO_2/In_2O_3 is minimized to obtain smooth surfaces, which eliminates the frequency dispersion in $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures. The capacitance (C/C_{OX}) versus gate-to-source voltage (V_{GS}) curve at multiple frequencies observes a negligible voltage shift $\Delta V \sim 0.3$ V toward the right side (positive gate bias side) with the increasing frequency from 500 to 1000 kHz. This negligible ΔV shift in depletion may be due to the negligible presence of frequency-dependant interface states at the ZrO_2/In_2O_3 interface and/or oxygen vacancies in the oxide ZrO_2. High-frequency (500–1000 kHz), C_{OX}–V_{GS} characteristics show the wide operating range of solution-processed $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ MISFETs. It indicates that $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures deliver noise-free high-speed devices for advanced integrated circuits (ICs) and information & communication technology. Fig. 6(d) shows parallel series resistance corrected conductance versus gate-to-source voltage (G_p–V_{GS}) characteristics with a frequency sweep from 500 to 1000 kHz with a frequency step of 100 kHz corresponding to Fig. 6(c). Maximum conductance or peak G_{p_max} at 500 kHz is measured as ~56 mS/cm^2. The Conductance method [22] investigates the interface trap density (D_{it}) at the ZrO_2/In_2O_3 interface. Interface trap density (D_{it}) extracted from measured maximum conductance at 500 kHz is ~2.5 × 10^{12}/eV cm^2, calculated with the equation [22]

$$D_{it} = \frac{2.5}{qA} \frac{G_{max}}{\omega} \tag{9}$$

where D_{it} is interface trap charge density, q is the electronic charge, A is the area, G_{max} is maximum conductance, and

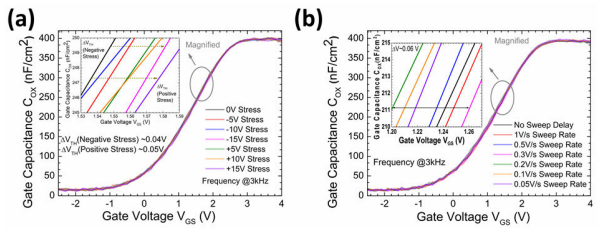

Fig. 7. (a) Capacitance-gate voltage curve for −15 to +15 V stress voltages, V_{stress} step = +5 V @ 3 kHz. (b) Capacitance-gate voltage curve for 0.05, 0.1, 0.2, 0.3, 0.5, 1 V/s sweep rate @ 3 kHz for $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ MISFET structures.

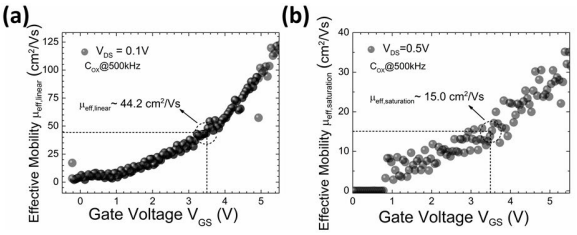

Fig. 8. (a) Effective field-effect mobility in the linear region ($\mu_{eff,linear}$) versus V_{GS} at V_{DS} = 0.1 V. (b) Effective field-effect mobility in the saturation region ($\mu_{eff,saturation}$) versus V_{GS} at V_{DS} = 0.5 V for $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures and C_{OX} at 500 kHz.

$\omega = 2\pi f$, f is the frequency, respectively. The low interface trap density reveals the high compatibility of high-κ ZrO_2 with semiconducting In_2O_3 thin films. Low interface trap density also confirms negligible frequency dispersion in $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures and the presence of excellent interface for ZrO_2/In_2O_3, consistent with the above results.

For the reliability of $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures, constant positive/negative voltage stress (CVS) analysis on the C_{OX}–V_{GS} characteristics is performed at room temperature. Fig. 7(a) shows the C_{OX}–V_{GS} characteristics at applied −5, −10, −15, and 0, +5, +10, +15 V negative and positive stress voltages at 3 kHz with gate bias sweep from −2.5 to 4 V with a step of 0.1 V on $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures. A slight shift in threshold voltage ΔV_{TH} (positive stress) ~ 0.05 V and ΔV_{TH} (negative stress) ~ 0.04 V in the C_{OX}–V_{GS} curve toward the positive gate bias side was detected. It indicates the increase in the accumulation of charge carrier's density in the inversion region due to the application of additional stress voltages. Hence, the investigated structures demonstrate considerable electrical reliability with the application of CVS, even at higher positive and negative electrical stresses. C_{OX}–V_{GS} characteristics are measured with variation in the sweep delay to investigate the prominent effects of mobile ionic charges. Fig. 7(b) shows C_{OX}–V_{GS} characteristics with sweep delay 1, 0.5, 0.3, 0.2, 0.1, 0.05 V/s at 3 kHz frequency and gate bias sweep from −2.5 to 4 V on $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ MISFET structures, respectively. Negligible threshold voltage ΔV_{TH} ~ 0.06 V shift due to sweep delay variation reveals insignificant mobile ionic charges in $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures.

According to Matthiessen's rule, the net mobility μ depends on the various mobilities based on different scattering mechanisms and the lowest mobility dominates [31]. The drain current is a combination of drift and diffusion currents, considering low drain voltages (V_{DS}), where channel charge is more uniform, allowing diffusion current to be neglected. Effective field-effect electron mobility ($\mu_{eff,linear}$) in the linear region may be defined by the following relations [25]:

$$\mu_{eff,linear} = \frac{Lg_m}{WC_{ox}V_{DS}} \tag{10}$$

where V_{DS} is drain-to-source voltage, L is channel length, W is channel width, C_{ox} is oxide capacitance, and g_m is transconductance, the slope of (I_D–V_{GS}) defined in relation (1) where V_{DS} is constant, respectively. Fig. 8(a). shows the effective field-effect mobility $\mu_{eff,linear}$ in the linear region with gate-to-source V_{GS} voltage sweep from −0.5 to +5.5 V. Effective mobility is calculated at drain-to-source voltage V_{DS} = 0.1 V (linear region) and C_{OX} is measured at 500 kHz frequency. Calculated value of $\mu_{eff,linear}$ is (~7.2 cm^2/Vs) at V_{GS} = 0.5 V, (~44.2 cm^2/Vs) at V_{GS} = 3.5 V, and (~96.6 cm^2/Vs) at V_{GS} = 5 V, respectively. This high mobility is indicative of the large ON-current and higher switching speed of the fabricated device structures. This corresponds to defect-free interface ZrO_2/In_2O_3 gate-stack and highly uniform, smooth, wide bandgap In_2O_3 semiconducting films. This is partially achieved by facile DUV irradiation of In_2O_3 and ZrO_2 thin films, which promotes stability and defect-free films and interface.

According to a multiple-trap-and-release (MTR) model, higher electron mobility may originate from an increased gate capacitance C_{OX}, which stems from the higher dielectric constant (κ) of the gate dielectric ZrO_2 relative to SiO_2 [33]. Hence, the higher value of mobility is also contributed by integrating high-κ ZrO_2 dielectric thin films into the $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ structures. Effective mobility can also be defined in the saturation region $\mu_{eff,saturation}$ and is given by the following relation [31]:

$$\mu_{eff,saturation} = \frac{2Lm^2}{WC_{OX}} \tag{11}$$

where m is the slope of $I_D^{1/2}$ versus (V_{GS}–V_{th}) curve, L is the channel length, W is the channel width, and C_{OX} is the oxide capacitance. The effective field-effect mobility in saturation region is calculated with gate-to-source V_{GS} voltage sweep from 0 to 5.5 V at V_{DS} = 0.5 V, and C_{OX} measured at 500 kHz, as shown in Fig. 8(b). The calculated value of $\mu_{eff,saturation}$ is obtained as (~0.1 cm^2/Vs) at V_{GS} = 0.5 V, (~15.0 cm^2/Vs) at V_{GS} = 3.5V, and (~30.5 cm^2/Vs) at V_{GS} = 5V, respectively. The higher value of $\mu_{eff,saturation}$ indicates the fabrication of high-performance $Al/ZrO_2/In_2O_3/Pt/SiO_2/Si$ MISFET devices, with excellent ZrO_2/In_2O_3 interface and uniform defect-free solution-processed In_2O_3 films.

Fig. 9(a) shows the gate leakage current density (J_G) versus gate-to-source (V_{GS}) voltage sweep from −2 to 2 V, V_{DS} = 0 V. J_G leakage current density is measured to be (~7.05 nA/cm^2) at V_{GS} = 1 V. This low leakage current density may be due to DUV irradiated ZrO_2 producing a hydroxyl group and/or oxygen vacancies free thin films, which control the conduction path of the leakage current. This signifies excellent

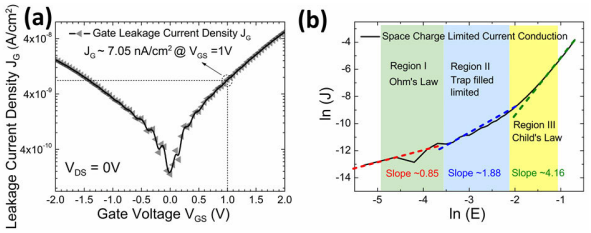

Fig. 9. (a) Gate leakage current density versus gate voltage curve at V_{DS} = 0 V and (b) SCLC current conduction mechanism in Al/ZrO_2/In_2O_3/Pt/SiO_2/Si structures.

dielectric ZrO_2 properties and good ZrO_2/In_2O_3 interface in Al/ZrO_2/In_2O_3/Pt/SiO_2/Si structures.

Space charge limited current (SCLC) leakage dominant current conduction mechanism with plot of natural log of leakage current density ln(J)- natural log of electric field ln(E) at room temperature is shown in Fig. 9(b). Three regions Region I, II, and III with slopes (∼0.85), (∼1.88), and (∼4.16) have been identified, respectively. Therefore, as per slope measurements, region 1 is governed by Ohm's law ($J \propto V$) for low leakage current before $V < V_{ON}$, where V_{ON} (∼0.3 V) is the transition voltage at the departure from Ohm's law. J–V characteristics followed by Ohm's law imply that the density of thermally generated free carriers (n_0) inside the films is larger than the injected carriers (n) or ($\tau_c > \tau_d$) carrier transit time is greater than dielectric relaxation time. The injected charges will redistribute themselves in the dielectric to maintain charge neutrality. Here, trap centers are partially filled with the weak injection of charge carriers. Region 2 is governed by trap-filled limited (TFL) $V_{ON} > V < V_{TFL}$, where V_{TFL} (∼1.2 V) is transition voltages at the departure from the TFL curve. Here, ($\tau_c \leq \tau_d$) carrier transit time is less than equal to dielectric relaxation time. The increased applied voltage may increase the density of free carriers resulting from injection to such a value that the Fermi level (E_{Fn}) moves up above the electron trapping level (E_t). After all traps are filled up, the subsequently injected carriers are free to move in the dielectric films. Thereafter, region 3 is governed by Child's law ($J \propto V^2$) after $V > V_{TFL}$ [32]. In the case of very strong injection, all traps are filled, and ($\tau_c < \tau_d$) carrier transit time is less than dielectric relaxation time, thus a space charge layer in the dielectric builds up. The traps get gradually saturated, which means that the Fermi level gets closer to the bottom of the conduction band. This results in a strong increase in the number of free carriers, thus explaining the increase in the current. The following relations define the current density in these regions [34]:

$$J_{\text{Ohm}} = q n_o \mu \frac{V}{d} \tag{12}$$

$$J_{\text{TFL}} = B\left(\frac{V^{l+1}}{d^{2l+1}}\right) \tag{13}$$

$$J_{\text{Child}} = \frac{9}{8}\mu\varepsilon\frac{V^2}{d^3} \tag{14}$$

where q is the electronic charge, n_o is the concentration of free charge carriers in thermal equilibrium, μ is the mobility, d is the thickness of dielectric, B is an l-dependent parameter, ($l = T_c/T$), T_c is characteristic temperature related to trap distribution, T is absolute temperature, V is the applied voltage, ε is the dielectric constant of ZrO_2 dielectric thin film. The computed effective field-effect mobility ($\mu_{\text{eff,linear}}$), SS, $I_{\text{ON/OFF}}$, D_{it} is commensurate and superior to the reported elsewhere [2], [7], [13], [16], [24], [25].

IV. Conclusion

High-performance, cost-effective, facile solution-processed thin film transistors have been successfully fabricated. The integration of indium oxide (In_2O_3) as n-channel with high-κ zirconium oxide (ZrO_2) as gate dielectric with facile DUV irradiated at low thermal budget depositions are demonstrated here. The FETs with TGBC architecture show very low device operation voltages and high effective electron mobility, depicting excellent ZrO_2/In_2O_3 interface and defect/oxygen vacancy-free uniform thin film interface formations. Furthermore, the dielectric properties are also investigated for ZrO_2 thin films, and a low interface trap density was computed, suggesting very good compatibility of In_2O_3 with ZrO_2 thin films. This study shows stable CMOS-compatible scalable FETs process flow for wearable, flexible, and printed electronics applications.

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