Micro and Nanostructures 208 (2025) 208377

Contents lists available at ScienceDirect

Micro and Nanostructures

journal homepage: www.journals.elsevier.com/micro-and-nanostructures

Design and analysis of multi-layer ZrO_2-based resistive random access memory (RRAM) for next-generation non-volatile memory

Mukul Jangid [a], Kunal Kaushik [a], Gaurav M. Khanal [b], Simranjit Singh [a], Sanjeev Kumar [c], Satinder K. Sharma [d], Arun K. Singh [a,*]

[a] *Semiconductor Research Centre, Department of Electronics and Communication Engineering, Punjab Engineering College (Deemed to be University), Chandigarh, India*
[b] *Department of Electrical and Electronics Engineering, J K Lakshmipat University, Jaipur, Rajasthan, India*
[c] *Department of Physics, Punjab Engineering College (Deemed to be University), Chandigarh, India*
[d] *School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology (IIT), Mandi, Himachal Pradesh, India*

ARTICLE INFO

Keywords:
RRAM
Non-volatile memory
ZrO2
Resistive switching
CMOS
Neuromorphic computing

ABSTRACT

This paper presents a RRAM (Resistive Random Access Memory) device having multiple buffer layers of HfO_x and TiOx along with switching layer of ZrO_2 to improve the overall performance of the device. Utilizing Technology Computer Aided Design (TCAD) software, the set and reset operations of the RRAM device are simulated, focusing on the formation and separation of conductive filaments (oxygen vacancy) in response to applied voltages. The conductive filaments are based on the number of defects present in the active switching layer. The proposed multi-layer device configuration consisting of ZrO_2 as the switching material is analyzed for its resistive switching behavior. The electrical characteristics, such as forming voltage, set/reset voltage, current switching ratio (I_{on}/I_{off}) and formation of low-resistance state (LRS), and high-resistance state (HRS) of the RRAM device are measured to evaluate the overall proposed device performances. The proposed $Ti/TiO_x/HfO_x/ZrO_2$ RRAM shows improved performance over the conventional $TiO_x/HfO_x/HfO_2$ RRAM device. With enhanced switching speed, reduced power, and high endurance $Ti/TiO_x/HfO_x/ZrO_2$ device is suitable for next-generation non-volatile memory (NVM) applications and neuromorphic computing system design.

1. Introduction

As the future technology of electronic system design include towards data-centric, low-power, and highly efficient nano computing systems, a critical need for novel non-volatile memory (NVM) arises to ensure scalability, high switching for fast processing and energy efficiency computing. The resistive random-access memory (RRAM) is a promising candidate for the next-generation memory technology due to simple two terminal metal–insulator–metal (MIM) structure, fast switching speed, low forming voltage requirement and potential for three-dimensional (3D) integration [1]. Zirconium dioxide (ZrO_2) is used as switching layer in RRAM devices due to its thermal stability, high dielectric constant, suitability with CMOS back-end-of-line (BEOL) fabrication process and compatibility with low-temperature processing [2]. The switching layers of HfO_2 in previously reported devices require large forming voltage due to high activation energy for generating oxygen vacancies, which results in the power loss and misalignment of conductive filament formation.

* Corresponding author.
E-mail address: arun@pec.edu.in (A.K. Singh).

https://doi.org/10.1016/j.micrna.2025.208377
Received 27 July 2025; Received in revised form 2 October 2025; Accepted 3 October 2025
Available online 4 October 2025

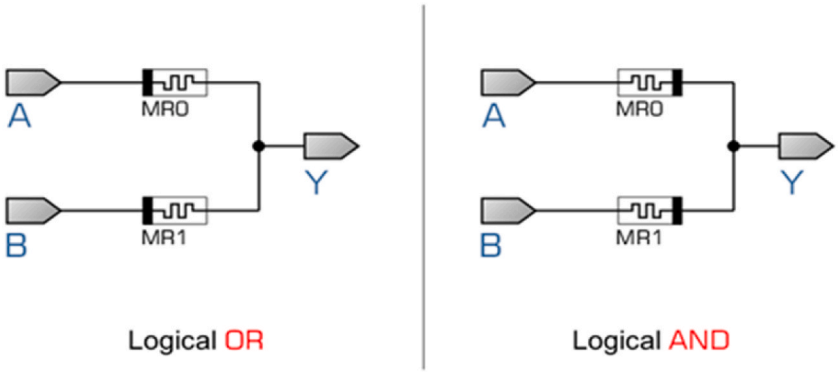

Fig. 1. Next generation logic gate circuit using RRAM device [9].

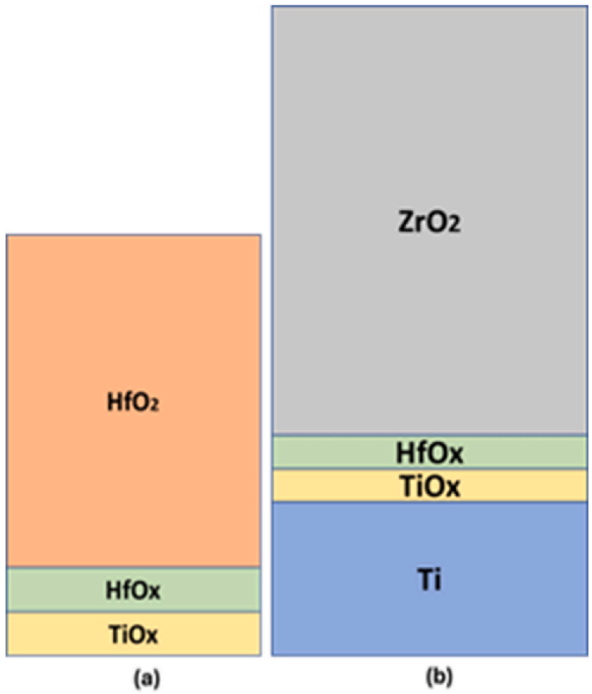

Fig. 2. Resistive switching structures used for simulations (a) conventional device $TiO_x/HfO_x/HfO_2$ (b) the proposed device $Ti/TiOx/HfOx/ZrO_2$.

On the other hand, single-layer of ZrO_2 in devices suffer from variability in forming voltage, switching endurance, and retention time [3]. These limitations can be addressed by interface engineering and multi-layer designs, which provide better control over filament dynamics and defect migration [4,5]. The improved design of memristor utilizing oxide-based bilayer ZrO_2/IGZO demonstrates potential applications including neuromorphic systems, attributed to their superior synaptic plasticity and capacity to emulate artificial nociceptor functions [3–5].

The interface layer engineering reduces forming voltages and improves switching reproducibility, highlighting the importance of electrode–oxide interfaces [6]. The atomic layer deposition (ALD) has been utilized for creating monolayer of ZrO_2 and HfO_2 material to improve the overall behavior of device [7]. An NiO barrier between Cu and ZrO_2 effectively has been demonstrated to eliminate the negative set operation in which typically a device fails to reset properly while improving retention beyond 3×10^4 s and endurance over 500 cycles [8]. These studies highlighted the key role of oxygen vacancy generation - recombination and energy barriers at the electrode interface in improving RRAM reliability.

The MIM device structures have also been explored in which ZrO_2 nanoparticle layers were fabricated by electron-beam evaporation [2–5]. These ZrO_2-based devices have demonstrated the stable resistive switching behavior with UV–visible light responsiveness and low-voltage operation, broadening its potential to be used in next generation like as logic gates as shown in Fig. 1 [9]. The advances in 2D oxide-sulfide based devices, such as the HfO_xS_y/HfS_2 heterostructure, show that forming-free and compliance-free operation is possible while maintaining low power (<20 pJ per cycle), fast speeds (60–80 ns), and excellent thermal stability

(retention over 10^4 s at 150 °C) [10].

In this work, we have proposed Ti/TiO_x/HfO_x/ZrO_2 device structure, the Ti top electrode works as an oxygen vacancy generator; the HfO_x and TiOx buffer layers control oxygen diffusion and reduce redundant filament growth; and the ZrO_2 base layer behaves as a stable resistive switch. The idea for the proposed design comes from previously reported work where inserting TiOx or NiO interface layers between electrodes and as switching oxides significantly improved the overall performance by lowering forming voltage, enhancing uniformity, and preventing premature breakdown [5,6]. The TiO_x interface layer between the bottom electrode and HfO_x layer reduces forming voltages and improves switching reproducibility, highlighting the importance of electrode and oxide interfaces.

2. Device structure and tcad modeling

The proposed Ti/TiO_x/HfO_x/ZrO_2 RRAM device combines the strengths of previously reported multilayer, top contact, and interface-controlled structures, offering enhanced endurance, reduced forming voltages, high I_{on}/I_{off} ratio, and improved resistance switching uniformity, all while maintaining the CMOS process compatibility. This device can be a strong representative for future flexible electronics, neuromorphic hardware, and embedded memory solutions. The schematics of both the conventional and proposed device structures are shown in Fig. 2(a) and (b), respectively.

RRAM devices use different types of materials, including gold (Au), platinum (Pt), and titanium nitride (TiN) as electrodes that are stable in an electrochemical property. [11,12]. Researcher also often use active metal electrodes like nickel (Ni), titanium (Ti), aluminum (Al), tantalum (Ta), and copper (Cu) to make RRAM devices [1–7]. Tantalum oxide (TaO_x), copper oxide (CuO_x), aluminum oxide (AlO_x), silicon oxide (SiO_x), zirconium oxide (ZrO_x), titanium oxide (TiO_x), and hafnium oxide (HfO_x) are all common materials use for the insulating layers [13–15]. Zirconium oxide (ZrO_2) is one of these materials that is widely studied and used as a switching layer in RRAM because it has good resistive switching characteristics [6–8]. The proposed device in Fig. 2(b) can be fabricated by first depositing bottom electrode of TiN using E-beam evaporator followed by multilayer deposition of different dielectric layers. Thin layer of ZrO2 can be prepared using either sputtering or sol-gel method followed by spin coating. The next step is to deposit HfO_x layer using sputtering. The interfacial titanium oxide (TiO_x) layer is subsequently formed either by depositing a thin Ti layer using sputtering followed by controlled oxidation. Finally, top electrode will be made of Ti using electron-beam evaporation. The developed devices will be annealed using rapid thermal annealing (RTA) technique to stabilize the oxide stoichiometry and enhance the switching reliability.

In the present work, simulations are carried out using Sentaurus TCAD Tool from Synopsys to evaluate the electrical, structural, and thermal properties of zirconium oxide (ZrO_2) in RRAM device. The material conductivity (σ) stays low at $1e^{-11}$S/cm, the electrical conductivity of individual particles (σ_{def1}) is set to 10 S/cm. Optical and dielectric properties are defined by an optical permittivity of 5.6 and a static permittivity (ε) of 40.0, which affect the electric field distribution. The activation energy (E_A) is set at 3.0 eV, governing thermally activated conductions, and the electron affinity (χ_0) and band gap energy (E_{G0}) are 2.5 eV and 5.4 eV, respectively. These parameters are for precise numerical modeling and evaluation of ZrO_2-based RRAM devices under various electrical and thermal conditions. Bulk materials are fixed at 0.23 W/cm/K, indicating moderate thermal transport necessary for heat dissipation modeling. The volume densities of particles and filaments are both $1.5e^{22}$ cm^{-3}, influencing filament formation dynamics.

In this design, TiN is selected as the electrode material for its excellent conductivity with the ZrO_2 switching layer [6,10]. Titanium Nitride (TiN) is a ceramic material, which is commonly used in resistive switching devices because it enables efficient current injections during the switching process and allows for easy formation of conductive filaments. The oxygen vacancy generator metal considered for this device is Titanium (Ti), due to its excellent stability, high work function, and inertness in reactive environments. The selection of the top and bottom electrodes also considers the need for uniformity in contact resistance, which is modeled as an idealized contact of no thickness. The electrodes must be designed to ensure that the switching layer is uniformly contacted, preventing localized effects that could result in ideal switching characteristics [10].

The interface layer is very important for making multi-layer RRAM devices that use ZrO_2 as the switching material more reliable, faster to switch, and longer-lasting. We chose Titanium oxide (TiO_x) and Hafnium oxide (HfO_x) as the middle layer because they have a high dielectric constant and resistive switching material like ZrO_2. The perfect arrangement of these layers to improve the device electrical properties. Both TiOx and HfOx interface layers are used for reduce the potential barrier between ZrO2 active switching layer and metal electrodes. The presence of ZrO_2 active layer used in proposed device to ensures smoother electrical conduction and changes the electric field distribution. Thus, enhancing the uniformity of the resistive switching process. And the interface layers help to change the impact of defects and impurities in the ZrO_2 layer, preventing any performance degradation over time. The overall stability and performance of the RRAM device are enhanced, resulting in high performance for non-volatile memory applications.

The proposed multi-layer structure in Fig. 2 (b) with interface layers exhibits better electrical characteristics over the conventional Tri-layer RRAM device. It improves switching uniformity by ensuring a more consistent electric field distribution across the switching material, which leads to stable and reliable switching behavior. The multi-layer device enhances the endurance by reducing the risk of limited defects and particles, which are often seen in single-layer devices, thus extending the device's lifetime [6–8]. The interface layers in the proposed device also helps to reduce the forming voltage for stable resistive switching, reduce power consumption. The multi-layer device structure enhances scalability and enables easy integration with other semiconductor memory devices. It is a key feature for next-generation memory technologies. The material selection and multi-layer technique of RRAM devices enhance the high performance, low set-reset voltage, and scalability for non-volatile memory applications, including those in neuromorphic computing and artificial intelligence [16].

The switching performance of oxide-based RRAM devices is fundamentally governed by the morphology of conductive pathways, which are developed through oxygen vacancy formation and annihilation in the dielectric matrix [17–20]. In set operations, oxygen

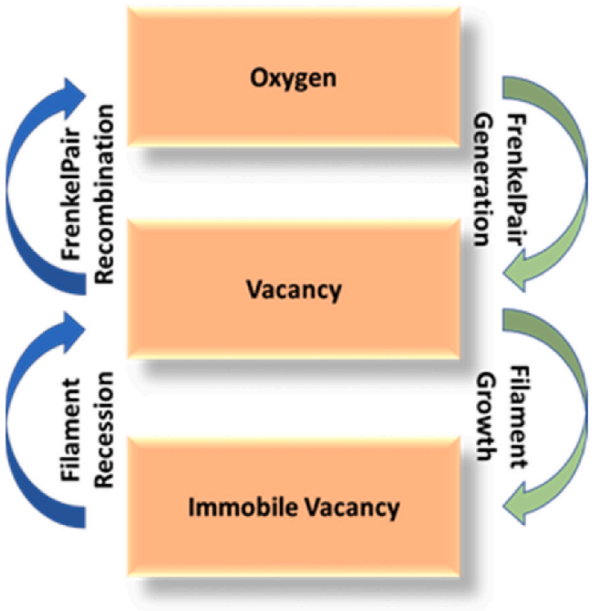

Fig. 3. Kinetic Monte Carlo (KMC) simulation mechanisms of conductive filaments in TCAD.

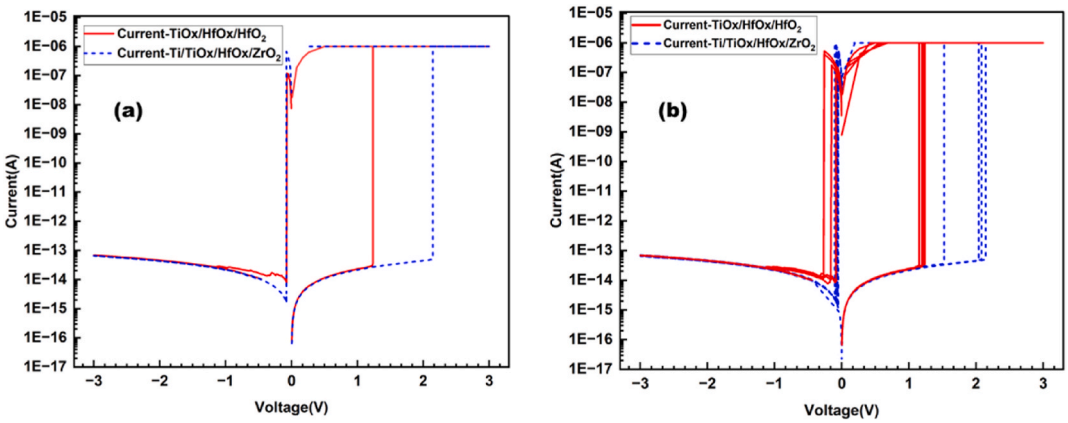

Fig. 4. Comparison of *I–V* switching characteristics for conventional and proposed RRAM devices with compliance current (CC) fixed at 1 μA for (a) a single cycle and (b) 5 cycles.

ions separate from the crystalline structure and drift to the active electrode, producing vacancy clusters. These clusters progressively create a low-resistance conduction path through the dielectric [18,20]. During the reset operations, reverse polarity voltages induce oxygen ion migration from interfacial regions back into the dielectric bulk. Subsequently vacancy-ion recombination dismantles the conduction paths, reinstating high resistance states. Precise simulation of these switching mechanisms demands integrated evaluation of charge carrier transport, ionic diffusion processes, and their statistical variability. The simulation approach is implemented in TCAD using a Kinetic Monte Carlo (KMC) methodology integrating the set–reset operation, showcased in Fig. 3.

Within this framework, oxygen ions are modeled as Particle1, to characterize their role non-conductive species involved in diffusion, generation, and recombination events. These interactions can result in the formation of Frenkel defects. Vacancies, defined as Particle2, are mobile within the insulating layer and may recombine with oxygen ions to annihilate defects. The dynamic processes of filament growth and dissolution are governed by the spatial and temporal evolution of these vacancies. When a critical concentration of vacancies is reached, a percolation path forms, enabling filamentary conduction processes. During a recession, the filament becomes vacant again.

3. Results and discussion

The multi-layer RRAM device described in this study uses a titanium (Ti) layer between the titanium nitride (TiN) top and bottom

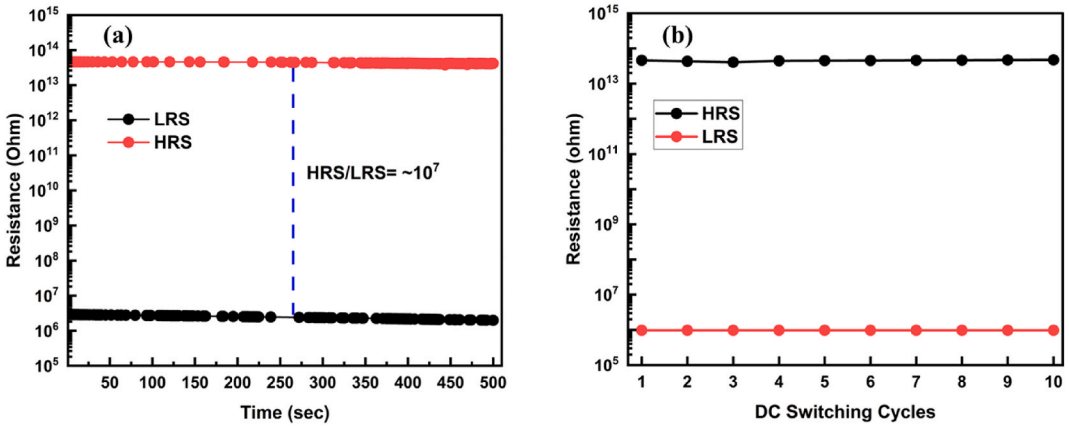

Fig. 5. Electrical characteristics of the proposed RRAM with compliance current (CC) fixed at 1 μA to estimate (a) retention and (b) endurance by measuring resistance as a function of time and DC switching cycles, respectively.

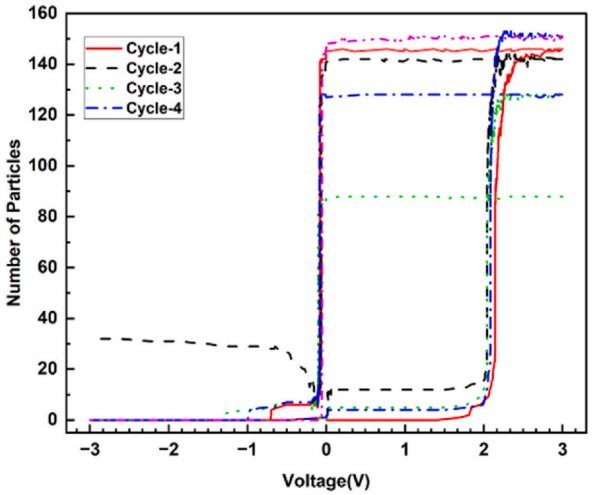

Fig. 6. Number of particles per cycle as a function of applied voltage for proposed RRAM device.

electrodes, with TiO_x and HfO_x as interface layers. As shown in Fig. 2 (b), the structure consists of a 1 nm-thick HfO_x layer and 1 nm thick TiO_x layer inserted between a 8 nm thick ZrO_2 layer and a 5 nm thick Ti layer. Although the combination of HfO_x and TiO_x creates an unstable interface; however, combining these with an active electrode—rather than using a single HfO_2 layer—enhances interfacial properties. This design combination contributes in making the device more stable in switching characteristics for RRAM.

Both conventional and proposed RRAM devices are analyzed with compliance current fixed at 1 μA. Fig. 4 illustrates the current-voltage characteristics under this condition. Reduced compliance current leads to earlier reset voltage initiation due to insufficient conductive filament formation. In this study, we have observed that higher compliance current (CC) may prevent the complete filament rupture, hindering the proper set/reset state of switching. The bias voltage starts from 0 to +3, +3 to 0, 0 to −3, and −3 to 0 and repeats these cycles 5 times. The resulting current-voltage characteristics are shown in Fig. 4. The first cycle forming voltage occurs at 2.25 V. After several voltage sweep cycles, the set voltage stabilizes in the range of 1.8–2.2 V, while the reset voltage is −0.1 V. In the proposed device, HfO_2 replaced with ZrO_2 which demonstrates improved switching behavior, indicating enhanced performance.

Fig. 5 (a) shows the retention time characteristics of the proposed device throughout a 500 s measurement interval. Both resistance states demonstrate exceptional stability over the complete period, with the high-resistance state (HRS) sustaining roughly 10^{13} Ω and the low-resistance state (LRS) keeping steady at around 10^6 Ω. The resistance window size (HRS/LRS ratio) maintains a value of around 10^7, indicating a superior memory margin for dependable data storage and retrieval operations. The lack of resistance degradation or drift during this time frame validates the nonvolatile characteristics of the memory states and indicates strong long-term data retention potential The endurance performance, assessing the device's capacity to endure repeated switching operations is shown in Fig. 5 (b). The ten successive DC switching cycles and the device reliably oscillates between the two discrete resistance states without any direct deterioration in switching performance. The high-resistance state (HRS) values constantly approximate 10^{13} Ω, but the low-resistance state (LRS) values uniformly measure about 10^6 Ω over all cycles. The resistance values for endurance and

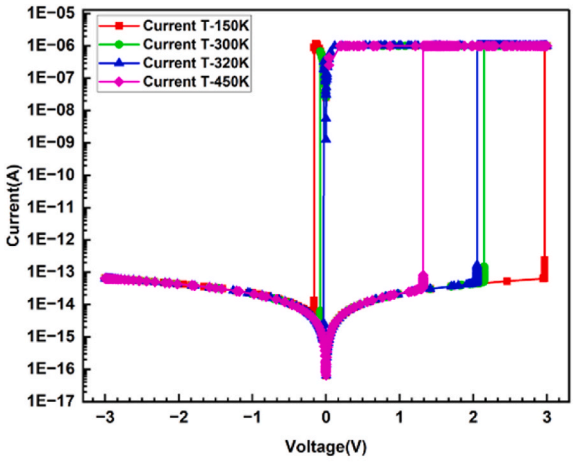

Fig. 7. *I–V* characteristics with different temperature ranges of the proposed RRAM device.

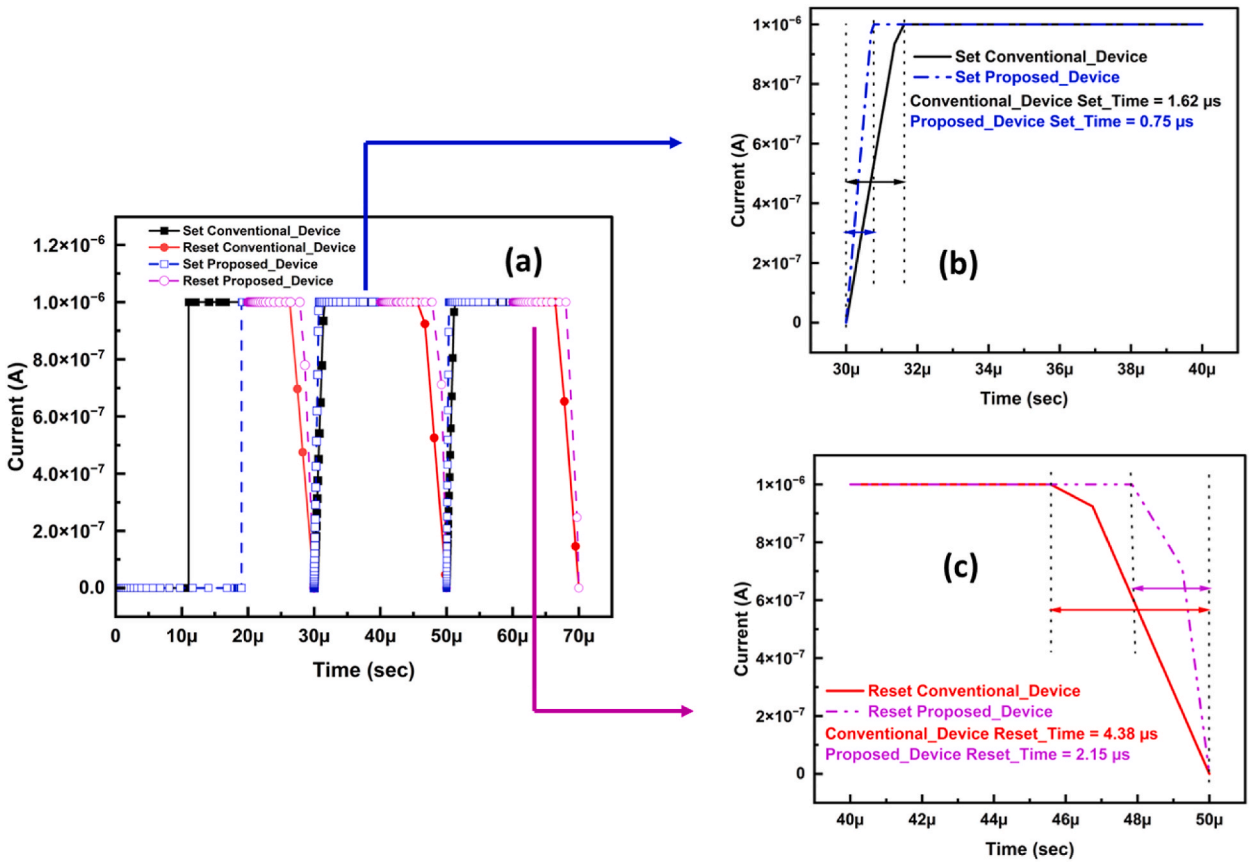

Fig. 8. Current behavior of the conventional and proposed RRAM device as a function of time for (a) set-reset state. The set state operation of proposed device in (b) during 30 µs–40 µs lasts for smaller duration than the reset state operation in (c) during 40 µs–50 µs, and is also smaller than that of the conventional device.

retention time characteristics are obtained at read voltage of +0.98V. The uniform switching behavior signifies that the proposed device can consistently execute several set/reset operations, essential for non-volatile memory applications.

Fig. 6 shows the variation in number of conductive particles as a function of applied bias voltage across the proposed RRAM device. The results suggest that the generation and recombination of the number of particles in the form of conductive filaments, which typically create defects, are responsible for switching behavior. In the positive voltage sweep (0 to +3 V and +3 to 0 V), high particle

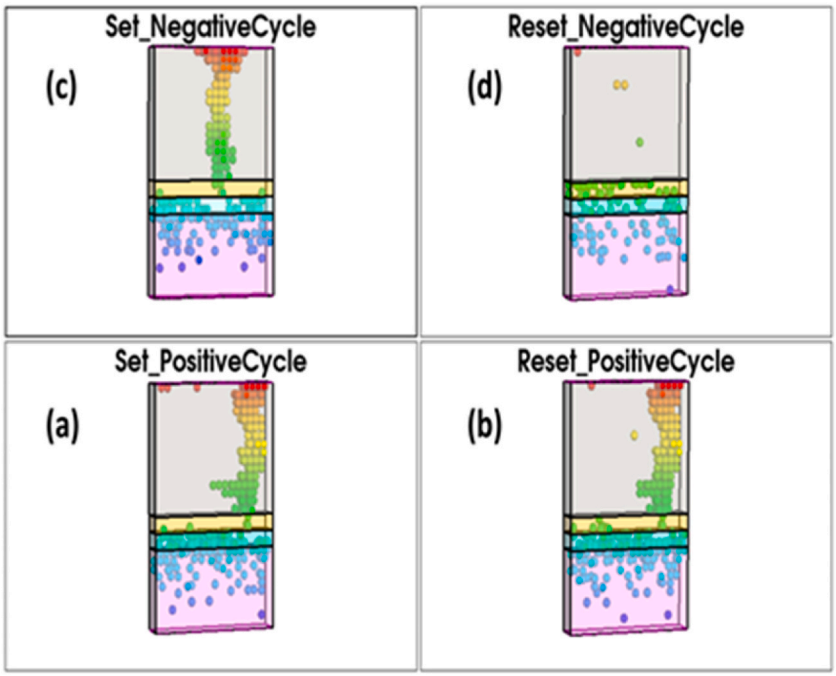

Fig. 9. Generation and recombination of 3rd cycle conductive filament and oxygen vacancies: (a) initial set state positive cycle (0 to +3), (b) Reset state positive cycle (+3 to 0), (c) Set state negative cycle (0 to −3), and (d) Reset state negative cycle (−3 to 0).

count is observed, however, there is an abrupt reduction in the particle count in the negative voltage sweep (0 to −3 V and −3 to 0 V). It confirms the non-volatile switching behavior characteristics of the proposed RRAM device.

To observe the temperature-dependent behavior of resistive switching characteristics of proposed device, DC voltage (+3 to −3) sweeps were performed both below the room temperature (150K) and above the room temperature (450K), and the results are as shown in Fig. 7.

As temperature rises, the forming voltage reduces, and also the reduction in the size of memory window. This behavior is attributed to the rupture of the conductive filament near the layer of dielectric/electrode interface, which enables leakage current to pass through the disrupted path. Based on crystal defect theory, the probability p that the oxygen ions overcome the potential barrier and generate oxygen vacancies is given by equation (1) as given below,

$$p \approx \nu \exp(-E / K_B T) \tag{1}$$

where E is the probability of defect formation rises correspondingly to 0.87 ev [21]. This leads to an increased density of oxygen vacancies related traps at elevated temperatures, which enhances trap-assisted tunneling (TAT) and results in higher temperature-dependent leakage current.

Fig. 8 (a) shows cycling behavior across three consecutive operational cycles having a bias variation from 0 to +3 V, and +3 to 0 V for both the conventional and proposed RRAM device shown in Fig. 2(a) and (b). The switching in current confirms successful transitions between HRS and LRS with excellent repeatability, a key metric for device endurance and reliability. The magnified view in Fig. 8 (b) focuses on the set operation during the second cycle, occurring between 30 μs and 40 μs. The proposed device transitions from HRS to LRS with a remarkably fast set time of 0.75 μs, indicating rapid conductive filament formation. This enables set-reset operations essential for practical memory applications. Fig. 8 (c) shows the reset process of the same cycle from 40 μs to 50 μs. The LRS-to-HRS transition of proposed device has a longer reset time of 2.15 μs, reflecting the physical mechanisms underlying filament rupture, which typically requires more energy and time compared to filament formation. This asymmetric switching behavior, in which reset operations consistently last longer than set operations, is consistent with theoretical predictions of resistive switching mechanisms. The lower values of switching time of proposed device in both set and reset state highlights its superior speed and efficiency over the conventional device. The results provide valuable insights into the device's operational characteristics suggesting both the temporal evolution and resistance state transitions required for nonvolatile memory operation.

Fig. 9(a) shows the 3rd cycle initial set state of positive cycle conductive filaments (CF) formed. The input voltage (0 to +3) crosses the threshold voltage value CF and connects the upper and lower electrodes in a stable state. In Fig. 9(b), after the initial set state demonstrates the reset state of the positive cycle, here, the input voltage (+3 to 0) falls below the threshold value, and the small number of CF collapses. Fig. 9(c) shows the state of the negative cycle after the first reset of the positive cycle CF formed. The input voltage (0 to −3) crosses the threshold voltage, and CF is formed. Fig. 9(d) shows the reset state of the negative cycle conductive filament which is not formed because when the input voltage (−3 to 0) falls below the threshold voltage, the substantial number of

Table 1
Comparison with other state-of-the-art RRAM devices.

Ref.	Device	V_{set} (V)	V_{reset} (V)	$I_{on/off}$	LRS (Ω)	HRS (Ω)	Remarks
[1]	$Ag/ZrO_2/ITO$	~2.0	−4.7	10^4	$\sim10^3$	$\sim10^6$	Experimental
[2]	$Au/HfAlOx/ZrO_2/TiN/Si$	~2.7	~ - 2.4	$\sim10^5$	$\sim10^2$	$\sim10^8$	Experimental
[3]	$Au/ZrO_2/TF$	~4.5	~ - 4.3	10	–	–	Experimental
[4]	$Pt/ZrO_2/I$ GZO/TiN	~0.9	~ - 0.7	10^5	10^2	10^4	Experimental
[5]	$Ag/ZrO_2/ITO$	~3.1	~ - 7.5	–	$\sim10^3$	$\sim10^6$	Experimental
[6]	$Cu/TiO_2/ZrO_2/TiO_2/Pt$	~2.83	~ - 0.99	–	~66.14	$\sim10^7$	Experimental
[7]	$N_2(Au/TiN/ZrO_2/HfO_2/Pt/Ti/SiO_2/Si)$	~1.4	~ - 0.9	–	$\sim10^5$	$\sim10^6$	Experimental
[8]	$ITO/ZrO_2/NiO/Ag$	~2.4	~0.6	–	$\sim10^2$	$\sim10^5$	Experimental
[10]	$TiOx/HfOx/HfO_2$	~1.5	~ −0.5 to −1	–	–	–	Simulation
Proposed Device	$ZrO_2/HfO_x/TiOx/Ti$	2.2	−0.1	10^7	$\sim10^6$	$\sim10^{13}$	Simulation

conductive filaments collapses. Table 1 represents the comparison of different multi-layer structures with the proposed (with ZrO_2 layers) RRAM device. In this study, the proposed device delivers better performance, including low reset voltage, high I_{on}/I_{off} ratio, and stable set-reset voltage.

4. Conclusion

This work discusses the design and analysis of a multi-layer ZrO_2-based RRAM device for high-performance non-volatile memory. The proposed structure enhanced the resistive switching behavior and improved high-resistance state (HRS) up to 10^{13} Ω with high $I_{on/off}$ current ratio up to 10^7, indicating its strong potential for next-generation memory technologies. RRAM device has an extra feature i.e, it is easily integrated with Back-End-Of-Line (BEOL) manufacturing technology. The simulation results of the proposed multi-layer RRAM have shown the improved device performance. Continued research will explore further optimization for improved set-reset time, retention and endurance. Future efforts will also be focused on the integration of this device with neuromorphic computing systems to support emerging applications in artificial intelligence and cognitive computing.

CRediT authorship contribution statement

Mukul Jangid: Writing – original draft, Software, Methodology, Investigation, Formal analysis. **Kunal Kaushik:** Software, Methodology, Formal analysis. **Gaurav M. Khanal:** Writing – review & editing, Visualization, Validation, Funding acquisition, Data curation. **Simranjit Singh:** Writing – review & editing, Supervision. **Sanjeev Kumar:** Writing – review & editing, Project administration, Funding acquisition. **Satinder K. Sharma:** Writing – review & editing, Visualization, Resources. **Arun K. Singh:** Writing – review & editing, Supervision, Funding acquisition, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

This work is supported by Ministry of Electronics & Information Technology (MeitY), Government of India (GoI) under grant sanction order EE-9/2/2021-R&D-E dated 22.05.2023. Authors acknowledge the use of research facilities developed under DST-FIST grant SR/FST/ETI-411/2016. MJ and KK acknowledge the financial support under "Visvesvaraya PhD Scheme for Electronics and IT: Phase-II", MeitY(GoI),

Data availability

All data that support the findings of this study are included within the article.

References

[1] B. Jang, J. Kim, J. Lee, J. Jang, H.-J. Kwon, Stable switching behavior of low-temperature ZrO_2 RRAM devices realized by combustion synthesis-assisted photopatterning, J. Mater. Sci. Technol. 189 (2024) 68–76, https://doi.org/10.1016/j.jmst.2023.12.016.
[2] P.R. Sekhar Reddy, V.R. Nallagatla, Y.A. Kumar, G. Murali, Enhanced resistive switching properties of $HfAlOx/ZrO_2$-based RRAM devices, Prog. Nat. Sci. Mater. Int. 32 (2022) 602–607, https://doi.org/10.1016/j.pnsc.2022.09.013.
[3] V.K. Yadav, A. Nath, M.B. Sarkar, Glancing angle fabricated Au/ZrO_2 nanoparticles-based device for non-volatile capacitive memory application, J. Mater. Sci. Mater. Electron. 35 (2024) 1234–1242, https://doi.org/10.1007/s10854-024-12780-5.
[4] X. Chen, Y. Jin, Z. Tao, Li Jiang, Xinjiang Wu, Yongyue Xiao, Bei Jiang, Xin Wen, Jun Zhang, Min Zhu, Cong Ye, An oxide-based bilayer ZrO_2/IGZO memristor for synaptic plasticity and artificial nociceptor, IEEE Trans. Electron. Dev. 70 (2023) 1001–1005, https://doi.org/10.1109/TED.2023.3236588.

[5] S. Lee, T. Kim, B. Jang, W.-Y. Lee, K.C. Song, H.S. Kim, G.Y. Do, S.B. Hwang, S. Chung, J. Jang, Impact of device area and film thickness on performance of sol-gel processed ZrO_2 RRAM, IEEE Electron Device Lett. 39 (2018) 668–671, https://doi.org/10.1109/LED.2018.2820141.
[6] Y. Li, Xi Li, Y. Wu, L. Fu, R. Chen, H. Wang, X. Gao, Tseng, effect of interface layer engineering on resistive switching characteristics of ZrO_2-Based resistive switching devices, IEEE Trans. Electron. Dev. 65 (2019) 376–382, https://doi.org/10.1109/TED.2018.2876942.
[7] L. Tang, H. Maruyama, T. Han, J.C. Nino, Y. Chen, D. Zhang, Resistive switching in atomic layer deposited HfO_2/ZrO_2 nanolayer stacks, Appl. Surf. Sci. 515 (2020), https://doi.org/10.1016/j.apsusc.2020.146015.
[8] T. Sun, F. Yu, C. Li, T. Ning, X. Liu, Z. Xu, Z. Yu, H. Li, F. Zhang, Q. Liao, Stable and repeatable ZrO_2 RRAM achieved by NiO barrier layer for negative set phenomenon elimination, Solid State Electron. 217 (2024) 108948, https://doi.org/10.1016/j.sse.2024.108948.
[9] A. Mishra, K. Singh, Low power high speed full adder design using CMOS memristor hybrid circuits, in: 2022 2nd International Conference on Intelligent Technologies (CONIT), 2022, pp. 1–7, https://doi.org/10.1109/CONIT55038.2022.9848115. Hubli, India.
[10] A. Xhameni, A. AlMutairi, X. Guo, I. Chirca, T. Wen, Stephan Hofmann, Valeria Nicolosi, Antonio Lombardo, Forming and compliance-free operation of low-energy, fast-switching HfO_xS_y/HfS_2 memristors, Nanoscale Hori 10 (2025) 616–627, https://doi.org/10.1039/D4NH00508B.
[11] K. Gayakvad, K. Somdatta, Mathe, Vikas, Dongale, Tukaram, Madhuri, Patankar, Ketaki, Spinel ferrites for resistive random access memory applications, Emergent Mater 7 (2024) 103–131, https://doi.org/10.1007/s42247-023-00576-y.
[12] M.K. Saini, M. Khosla, B. Raj, Review—exploring emerging materials for memristor fabrication: a review of recent progress, ECS J. Solid State Sci. Technol. 13 (2024) 115004, https://doi.org/10.1149/2162-8777/ad9401.
[13] H.-S. Philip Wong, Heng-Yuan Lee, Shimeng Yu, Yu-Sheng Chen, Yi Wu, Pang-Shiu Chen, Byoungil Lee, Frederick T. Chen, Ming-jinn tsai, metal–oxide RRAM, IEEE ASME J. Microelectromech. Syst. 100 (6) (2012) 1951–1970, https://doi.org/10.1109/JPROC.2012.2190369.
[14] N. Jain, S.K. Sharma, R. Kumawat, P.K. Jain, D. Kumar, R. Vyas, Resistive switching, endurance and retention properties of ZnO/HfO2 bilayer heterostructure memory device, Micro and Nanostructures 169 (2022) 207366, https://doi.org/10.1016/j.micrna.2022.207366.
[15] H.Z. Zhang, D.S. Ang, K.S. Yew, X.P. Wang, Observation of self-reset during forming of the TiN/HfOx/TiN resistive switching device, IEEE Electron Device Lett. 37 (9) (2016) 1116–1119, https://doi.org/10.1109/LED.2016.2590471.
[16] S. Yu, H.-S.P. Wong, A phenomenological model for the reset mechanism of metal oxide RRAM, IEEE Electron Device Lett. 31 (2010) 1455–1457, https://doi.org/10.1109/LED.2010.2078794.
[17] R. Jiang, Z. Han, X. Du, Reliability/uniformity improvement induced by an ultrathin TiO2 insertion in Ti/HfO2/Pt resistive switching memories, Microelectron. Reliab. 63 (2016) 37–41, https://doi.org/10.1016/j.microrel.2016.05.013.
[18] Ryo Nakajima, A. Azuma, H. Yoshida, T. Shimizu, T. Ito, S. Shingubara, Hf layer thickness dependence of resistive switching characteristics of Ti/Hf/HfO2/Au resistive random access memory device, Jpn. J. Appl. Phys. 57 (2018) 06HD06, https://doi.org/10.7567/JJAP.57.06HD06.
[19] X. Guan, S. Yu, H.-S.P. Wong, On the switching parameter variation of metal-oxide RRAM—Part I: physical modeling and simulation methodology, IEEE Trans. Electron. Dev. 59 (2012) 1172–1182, https://doi.org/10.1109/TED.2012.2184545.
[20] U. Russo, D. Ielmini, C. Cagli, A.L. Lacaita, Self-accelerated thermal dissolution model for reset programming in unipolar resistive-switching memory (RRAM) devices, IEEE Trans. Electron. Dev. 56 (2009) 193–200, https://doi.org/10.1109/TED.2008.2010584.
[21] C. Kittel, Introduction to Solid State Physics, eighth ed., Wiley, Hoboken, NJ, 2004, pp. 585–591.