Integrated Lith-To-Etch Protocols For Indigenous Resists Technology Enabling High-Fidelity Device Fabrication

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Abstract

Semiconductor processing of next-generation electronics increasingly relies on robust pattern transfer technologies that can be adapted to diverse compatible resist material formulations and pattern transfer protocols. Here, we developed reactive ion etching (RIE) protocols for the prototype devices using distinct resist chemistries: organic non-chemically amplified resist (n-CAR) and metal-organic cluster (MOC) resist. The designed resists are well established for their high-resolution performance across next-generation lithography (NGL) technologies, through robust investigation of their distinct etching and process integration strategies. For frontline semiconductor platforms, likewise Si/Ge, the organic resist was combined with a conventional wet development process, followed by an optimised RIE step to achieve high-fidelity pattern transfer in semiconductor material. Moreover, for hygroscopic and solvent-selective systems, such as halide perovskites, where wet development is inhibited, novel MOC resists were employed due to their superior etch resistance and enhanced selectivity toward standard etchants, including SF_6 chemistry. This enables dry development and controlled feature transfer without solvent exposure.

Introduction

Continued scaling of semiconductor and emerging electronic devices has made pattern transfer more critical, rather than lithographic resolution alone, a central challenge in device fabrication. Although next-generation lithography (NGL) technologies, including extreme ultraviolet lithography (EUVL), electron-beam lithography (EBL), and helium-ion beam lithography (HIBL), are capable of defining features well below 10 nm, the final feature size accuracy and structural integrity of these patterns are governed by the subsequent resist development and plasma etching protocols, used to transfer them into nano features. With the increasing adoption of heterogeneous device architectures incorporating semiconductors, compound materials, and hybrid stacks, mismatches between resist chemistry and etch processes have become a critical limitation in overall process integration.

Reactive ion etching (RIE) continues to serve as the primary pattern transfer technique due to its anisotropic ion bombardment, flexible plasma chemistry, and compatibility with high-aspect-ratio nanostructures[1,2]. However, plasma-induced phenomena such as resist erosion, line edge roughness (LER) increment, and near-surface substrate damage are strongly influenced by the chemical composition and mechanical stability of the lithographic resist[1,2]. The conventional organic chemically amplified resists (CARs)[3,4] and non-chemically amplified resists (n-CARs)[5–8], are the mainstay materials for the latest lithography techniques such as DUV, immersion-based and EUV lithography. The conventional organic resists exhibit high sensitivity and resolution; however, their resistance to fluorine- and oxygen-based plasmas is comparatively limited. During RIE, this can lead to noticeable resist erosion, which often requires either thicker resist coatings or the use of additional hard-mask layers to preserve pattern integrity. Such adjustments increase process complexity and can introduce variability during pattern transfer.

In addition to plasma stability, the development step plays a critical role in determining compatibility with different material platforms. Wet chemical development, widely used for organic resists, may not be suitable for hygroscopic or solvent-sensitive materials such as halide perovskites and certain low-dimensional semiconductors. Solvent interaction during development can cause swelling, feature deformation, compositional changes, or interfacial degradation. Even short exposure times may alter stoichiometry or generate defect states, thereby affecting device performance and long-term stability. For these material systems, conventional wet-processed lithography can therefore become a limiting factor in achieving reliable nanopattern transfer.

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To address these limitations, resist systems with more robust inorganic frameworks have been explored, particularly metal-oxide[9] and metal-organic cluster (MOC) resists[10–13], have attracted growing interest because of their inherently higher plasma durability and favourable etch selectivity. The inorganic backbone of these resists provides enhanced resistance to fluorine-based plasmas such as SF_6 / CF_4, enabling the use of thin resist coating while maintaining pattern fidelity. Consequently, inorganic resists are increasingly regarded not only as high-resolution lithographic materials, but also as enablers of robust lithography-to-etch integration[14,15].

Nevertheless, resist development and plasma etching are addressed as largely independent process steps, typically optimised for a single resist formulation or a specific substrate. Fewer studies consider how resist chemistry, development route (wet or dry), and plasma conditions interact when integrated into a complete pattern-transfer flow. Direct comparisons between conventional organic resists (n-CARs) and hybrid MOC-based resists, particularly across substrates with substantially different chemical and mechanical stability, such as Si / Ge in contrast to halide perovskites, remain relatively uncommon.

Here, we present an integrated lithography-to-etch process framework based on two fundamentally different resist platforms: a long-chain organic non-chemically amplified resist (n-CAR)[16], poly-MAPDST and a hybrid metal-organic cluster, In-MAA resist[10] . Both materials have been previously demonstrated to support high-resolution patterning in NGL regimes, allowing the present work to focus on etch behaviour and process integration rather than lithographic limits. For chemically and mechanically stable substrates such as Ge/Si, n-CAR patterns generated and resolved using conventional wet development are transferred through optimised RIE conditions to achieve well-defined features for FinFET. On the other hand, the ReRAM stack exhibits switching of resistance states upon applied electric field and enables memory retention [17,18]. In contrast, for solvent-sensitive materials such as lanthanohalide, MOC resists combined with dry development and fluorine-based plasma etching are employed to realise the Metal/Oxide/Metal ReRAM stack. Through a direct comparison of these workflows, this study establishes practical guidelines for resist selection and development methodology aimed at high-fidelity pattern transfer across diverse material platforms.

2. Experimental Section

2.1 Processing and Characterisation

PlannarTech RIE system was used for the etching process. Resist nano-patterns transferred over substrates were characterised using field-emission scanning electron microscopy (FESEM) from the Zeiss Gemini SEM 500, Germany, to measure pattern feature width and uniformity. Film thickness measurements were performed using an atomic force microscope (AFM); from Bruker Dimension Icon to evaluate thickness uniformity across the coated substrates. Line-edge roughness (LER) and line-width roughness (LWR) of the exposed line patterns were quantified using SuMMIT® metrology software, an industry-standard tool for nanoscale roughness analysis in lithographic patterning. The Bruker contour gt-k 3D optical profilometer was used to image the Ag-electrode micro-patterns.

3. Results and Discussion

3.1 Lithography-to-Etch Integration Using n-CAR for FinFET Fabrication

To demonstrate the applicability of indigenous organic resist platforms for advanced device fabrications, a lithography-to-etch process flow was implemented for the realisation of Ge-on-Si FinFET structures using a negative-tone chemically amplified resist, poly-(4-(methacryloyloxy) phenyl)-dimethyl sulfonium triflate (poly-MAPDST)[16,19]. The process was designed to evaluate resist performance, pattern fidelity, and etch compatibility to pattern critical features of scaled transistors such as channel fins, with emphasis on controlled fin definition and minimal pattern degradation during plasma transfer.

The FinFET fabrication flow was based on a mesa-type architecture, in which a Si/Ge buffer stack was first deposited on the Si substrate to form a relaxed virtual substrate and mitigate lattice-induced strain[20,21]. An n-type Ge layer was then introduced to provide electrical isolation from the substrate, followed by deposition of the p-type Ge channel layer[22]. Essential processing, such as surface passivation of Ge with the halogens, was immediately performed prior to resist coating over Ge to prevent GeO_x interference.

Afterwards, the poly-MAPDST resist was spin-coated at 2000 rpm for 45s and pre-baked at 100 °C for 1 min to form ~ 30 nm uniform thin films, optimised for sub-20-nm critical dimension (CD) patterning, maintaining considerable LER/LWR as ~ 1.8 nm / ~ 1.6 nm respectively, at EBL dose ~ 600μC/cm^2 for L/9S line-patterns, meeting the criteria for

sub-20 nm fin patterning[22]. This poly-MAPDST resist dose optimisation was carried out using a square-pattern exposure matrix with doses ranging from 10 to 1000 μC/cm^2 at 18 keV e-beam energy. After exposure, samples were post-baked at 115 °C for 90 sec and developed in aqueous tetramethyl ammonium hydroxide (TMAH) for 30 sec, followed by DI water rinse and N_2 drying. e-beam exposure induces chemical modification of the sulfonium groups in poly-MAPDST, leading to selective dissolution of unexposed regions during aqueous development and retention of exposed features, consistent with negative-tone behaviour[16].

Pattern transfer into the underlying Ge layer was carried out using RIE, with the optimised process parameters such as power = 20W, SF_6 = 20 sccm, O_2 = 5 sccm, and chamber vacuum at 1mTorr. The relatively high etch resistance of poly-MAPDST, as reported by *Choudhary et al.,* enabled direct plasma transfer of the fin patterns into Ge without excessive resist erosion or profile distortion[22]. After mesa etching, residual poly-MAPDST was removed using a mild Ar/O_2 plasma, avoiding damage to the Ge surface while ensuring complete resist stripping. Following the fin definition, subsequent process steps, including gate stack formation and metallisation, were carried out using standard process modules; however, the fidelity of these downstream steps was strongly dependent on the quality of the initial lithography-to-etch pattern transfer. Figure 1: (a) Process sequence for fin patterning; (b) e-beam exposure of the polyMAPDST resist; (c) schematic of the patterned mesa highlighting the critical fin features; (d) mask layout file; and (e) corresponding RIE-patterned mesa and fins.

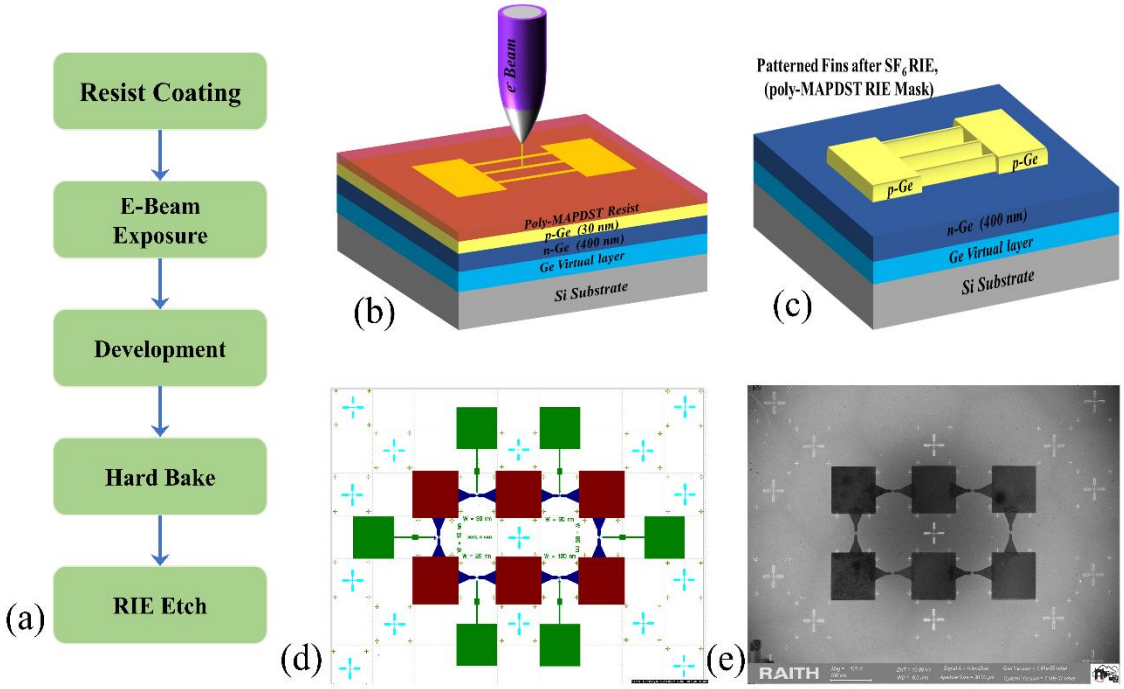

Figure 1 (a) Process Sequence to pattern fins, (b) E-beam exposing the polyMAPDST resist (c) Schematic patterned mesa along with critical feature fins, (d-e) depicts the mask layout file, correspondingly RIE patterned mesa and fins FE-SEM micrograph, respectively.

The successful realisation of Ge-on-Si FinFETs with narrow fin widths and sharp profiles underscores the suitability of poly-MAPDST as an indigenous n-CAR platform for advanced nanopatterning [Figure 2]. More importantly, this process flow highlights how careful co-optimisation of resist chemistry, exposure conditions, and RIE parameters enables high-fidelity pattern transfer in scaled device architectures without relying on complex hard-mask schemes.

The presented FinFET process flow demonstrates that poly-MAPDST functions as an effective indigenous n-CAR platform for high-resolution FinFET fabrication on mechanically stable Ge-on-Si substrates. Key enablers include surface passivation prior to aqueous development, stable negative-tone behaviour during EBL, and high etch resistance under SF_6-based RIE. The poly-MAPDST wet-developed RIE process serves as a benchmark for comparison with alternative resist chemistries and pattern transfer strategies.

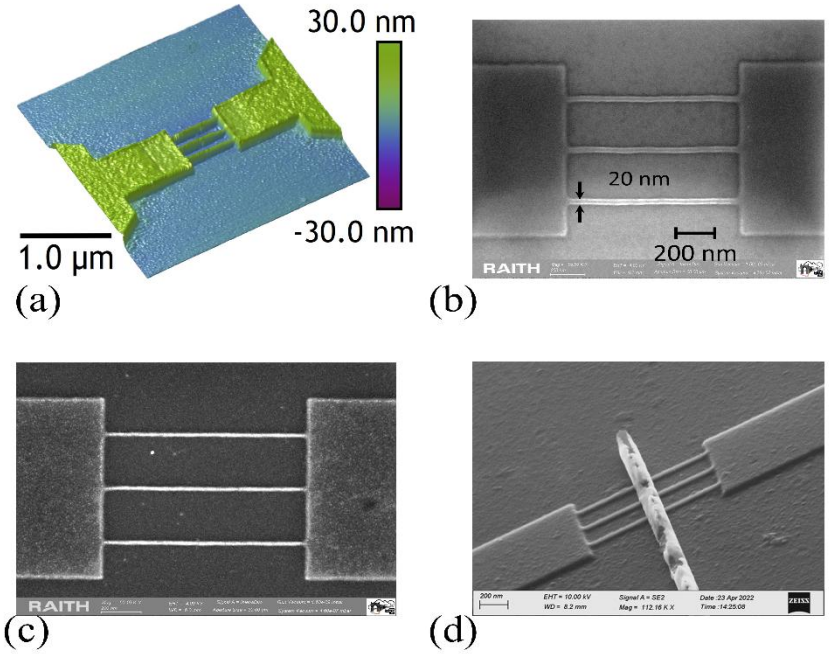

Figure 2: (a) AFM image of the pattern fins, (b) depicts the FESEM micrograph of the resist after development, (c) patterned fins after $SF_6 + O_2$ RIE plasma etch with optimized parameters: power = 20W, SF_6 = 20 sccm, O_2 = 5 sccm, and chamber vacuum at 1mTorr, (d) Tilted view of the FinFET after patterned gate.

3.2 Lithography-to-Etch Integration Using In-MAA MOC Resist for Perovskite ReRAM Stack Fabrication

To extend lithography-to-etch integration towards perovskite or similar chemically fragile and solvent-sensitive material systems, such as pnictohalides, lanthanohalides, etc., a fully dry patterning protocol was implemented for ReRAM device fabrication using an indigenous indium methacrylate (In-MAA, $InC_{14}H_{18}O_8$) MOCs-based resist[10]. This process flow was specifically designed to eliminate wet chemical development and thereby preserve the structural and interfacial integrity of halide-based switching layers.

The ReRAM device stack consisted of a spin-coated $AgEuBr_4$ lanthanohalide switching layer (SL) deposited on FTO-coated glass substrates. Afterwards, a sheet of Ag metal was deposited over the $AgEuBr_4$ SL, which was defined using lithography-assisted pattern transfer to realise Ag/$AgEuBr_4$/FTO ReRAM stack, where In-MAA served as the primary resist and etch mask [Figure 3].

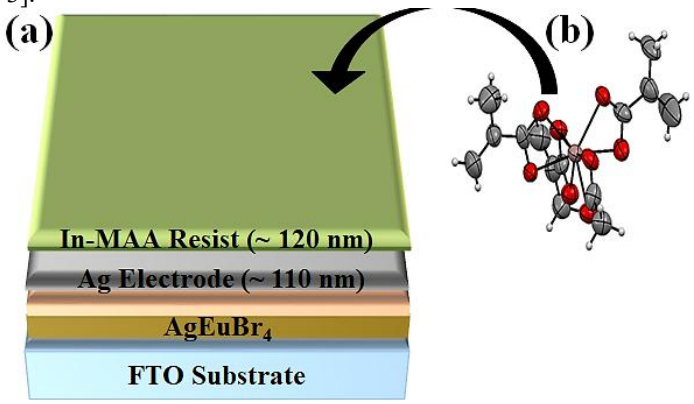

Figure 3 (a) 3-D schematic of In-MAA resist/Ag Electrode/Lanthanohalide/FTO input stack for RIE processing, and (b) Single crystal structure of developed In-MAA, MOC resist formulation. *Colour code: grey sphere, C; red sphere, O; purple sphere in the middle, In; white sphere, H.*[10]

An In-MAA MOC resist layer (~120 nm) was spin-coated directly onto the Ag top-electrode blanket film (~ 110 nm). Resist was exposed using a deep-ultraviolet (DUV, 248 nm) source through a photomask defining circular electrode arrays. Upon exposure, the In-MAA MOCs underwent localised photo-induced crosslinking, producing hardened regions with significantly enhanced resistance to plasma etching[10]. In contrast, unexposed regions retained their original metal–organic structure and remained susceptible to plasma-assisted removal.

Resist development was performed entirely through sequential dry plasma treatments, avoiding any solvent interaction with the underlying SL. Initially, a low-power (20 W RF) O_2 plasma was employed at 2.6 x 10^4 mbar to selectively decompose the organic ligands within the unexposed In-MAA resist regions. This was followed by an SF_6 plasma step operated at 4.5 x 10^4 mbar & 45 W RF. Under these conditions, fluorine species interact with the indium-rich fragments formed after O_2 exposure, allowing the unexposed resist to be removed as fluorinated by-products. The O_2/SF_6 sequence was applied iteratively until the unexposed regions were fully cleared, while the cross-linked resist features remained intact.

After dry development, the cross-linked In-MAA layer served directly as the etch mask for Ag pattern transfer. The underlying Ag film was etched using an SF_6-based RIE process. In the fluorine-rich plasma environment, Ag removal proceeds through the formation of Ag-F species, which are weakly bound and readily removed under ion bombardment[23]. Under the same conditions, the exposed In-MAA mask showed a much slower etch rate. This difference arises from the inorganic In-O backbone and plasma-induced densification of the cross-linked network, which enhances its resistance to fluorine chemistry. The resulting etch selectivity was sufficient to define circular micro-electrodes. The higher Ag etch rate relative to the cross-linked MOC layer allowed controlled vertical transfer while suppressing lateral undercutting and limiting ion interaction with the underlying $AgEuBr_4$ SL.

Exposure to SF_6 plasma can lead to temporary surface fluorination of the In-matrix, with the formation of InF_3 expected because of the strong In-F bond energy[24]. Any InF_3 formed during plasma exposure is gradually removed by continued ion-assisted sputtering or destabilised during subsequent O_2 and Ar treatments, where fluorinated species are desorbed. Following Ag etching, the remaining In-MAA MOCs mask was stripped using a controlled N_2/Ar plasma ashing sequence[25,26]. A short bake step (100–120 °C) for 10 min in N_2 was then applied to remove physisorbed species and stabilise the patterned interfaces before electrical characterisation.

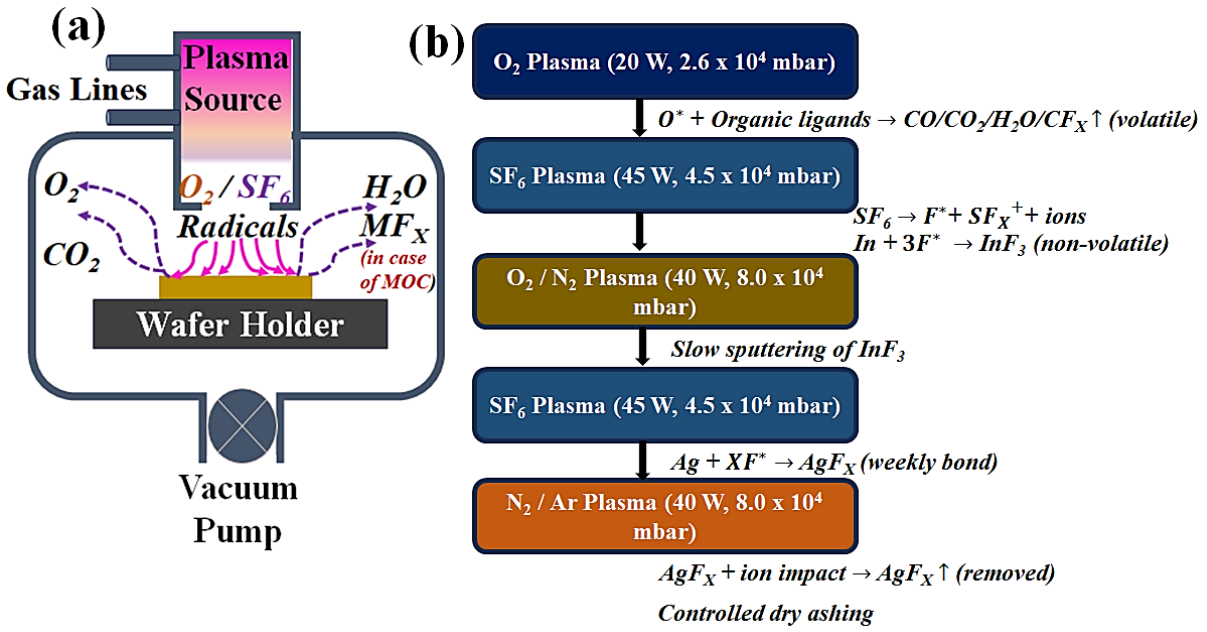

Figure 4 (a) Schematic illustration of plasma-based processing over the input samples inside the RIE chamber, (b) process flow summary of plasma-assisted chemistry during dry development of In-MAA MOC resist and subsequent Ag etching.

Figure 4 shows the plasma processing sequence implemented during lithography-to-etch integration. As illustrated in Figure 4(a), the samples were placed in controlled reactive ion plasma environments inside the RIE chamber, plasma

conditions were controlled through adjustment of RF power, gas flow rate, and chamber pressure. Figure 4(b) summarises the key chemical pathways involved during dry development of the In-MAA resist and subsequent Ag etching. The schematic highlights how ligand removal, transient fluorination, and ion-assisted desorption collectively enable selective clearing of unexposed resist regions and efficient Ag pattern transfer, while preventing the accumulation of stable fluorinated residues. This visualisation supports the experimental observations by clarifying the role of sequential plasma.

This fully dry lithography-to-etch workflow enabled reproducible definition of Ag top electrodes without exposing the $AgEuBr_4$ SL to solvents at any stage. The Ag etch process produced circular electrodes with a nominal diameter of ~ 250 µm, corresponding to a device area of 0.0005 cm^2 for the ReRAM, while maintaining the integrity of the underlying stack. The optical micrographs in Figure 5(a-c) showed uniform Ag electrode patterns on the $AgEuBr_4$/FTO substrate, exhibiting considerable memristive J-V resistive switching (RS) characteristics, switching to its low resistance state (LRS) from high resistance state (HRS) at 0.28 V (SET) and reverting to its HRS at -0.36 V (RESET), yielding ~ 859.09 LRS/HRS. The fifty consecutive cycle-to-cycle (C2C) J-V sweeps shown in Fig. 5(d) demonstrate stable and repeatable switching, validating the robustness and pattern fidelity of the fully dry fabrication process.

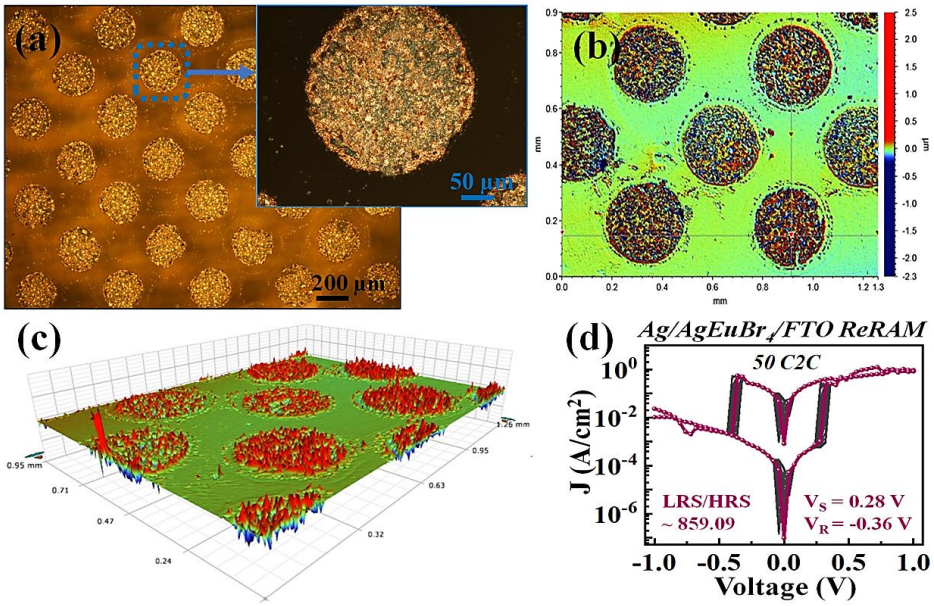

Figure 5. (a) Optical micrograph of the patterned Ag top electrode on the $AgEuBr_4$/FTO stack. (b) Planar optical profilometry map showing the lateral definition and uniformity of the etched Ag electrode. (c) 3-D surface profilometry image illustrating the topographical profile of the patterned electrode, and (d) J-V RS characteristic of Ag/$AgEuBr_4$/FTO ReRAM.

Within the broader context of this study, the In-MAA-based dry etch process represents a complementary integration pathway to wet-developed organic resists used on mechanically stable substrates. Together, these approaches establish a substrate-adaptive lithography-to-etch framework in which resist chemistry, development strategy, and plasma conditions are co-optimised to achieve high-fidelity pattern transfer across heterogeneous device material systems.

4. Conclusion

This work presents two practical lithography-to-etch approaches using indigenous resists for high-fidelity pattern transfer on very different material platforms. For Ge/Si FinFET processing, poly-MAPDST (n-CAR) was patterned by EBL and wet-developed, then transferred into Ge /Si substrates using an SF_6/O_2 RIE recipe, producing narrow fins with (sub-20 nm) controlled feature. For solvent-sensitive lanthanohalide ReRAM, In-MAA (MOC) enabled an all-dry flow; plasma development (O_2 then SF_6) and SF_6-based Ag etching yielded ~ 250 µm circular top Ag-electrodes while avoiding wet exposure of the switching layer. Together, these results show that matching resist chemistry with development mode and plasma conditions improves pattern fidelity, reduces process complexity, and supports reproducible device fabrication across stable and fragile stacks.

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