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Effect of electrical stress on Au/Pb ($Zr_{0.52}Ti_{0.48}$) O_3/TiO_xN_y/Si gate stack for reliability analysis of ferroelectric field effect transistors

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Metal-Ferroelectric-Insulator-Semiconductor (MFIS) structure with 20 nm thin lead zirconate titanate (PZT) ferroelectric film and 6 nm ultrathin high-κ titanium oxynitride (TiO_xN_y) insulator layer on p-Si substrate were fabricated. Effect of constant voltage stress (CVS) on electrical characteristics of MFIS structure was investigated to study the reliability of fabricated devices. The experimental results showed trivial variation in memory window (ΔW) from 1.05 to 1 V under CVS of 0 to 15 V (5.76 MV/cm) at sweep voltage of $\pm$5 V. Also, leakage current density (J) reduced from 5.57 to 1.94 μA/cm^2 under CVS of 5.76 MV/cm, supported by energy band diagram. It signifies highly reliable TiO_xN_y buffer layer for Ferroelectric Random Access Memory. After programming at $\pm$5 V, the high (C_H) and low (C_L) capacitances reliability remains distinguishable for 5000 s even if we extrapolate measured data to 15 years. Microstructures analysis of XRD reveals the formation of (100) and (111) orientation of PZT and TiO_xN_y, respectively. Thus, Au/PZT/TiO_xN_y/Si, MFIS gate stacks can be potential candidate for next generation reliable Ferroelectric Field Effect Transistors. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4897952]

Non-Volatile memories are classified into charge storage memories NAND, NOR FLASH and non-charge storage memories Ferroelectric Random Access Memory (FeRAM), Magnetic RAM (MRAM), Phase Change RAM (PCRAM), and Resistive RAM (ReRAM). The next generation scaling of charge storage devices in sub-nano-metric regime is hampered by availability of inadequate number of electrons. Therefore, the memory devices with memory states, but devoid of charges, are prospective contenders for next technology node.[1] In recent years, FeRAM has attracted much attention due to its fast access time, low power consumption, high security, excellent retention, and endurance time.[2] Current commercial applications of FeRAM include Radio-Frequency Identification (RFID) card, Identity (ID) card, smart card, and various other low density embedded applications.[1] The performance of ferroelectric field effect transistors (FeFET) with metal-ferroelectric-semiconductor (MFS) structure is hampered by interdiffusion and interface reaction between silicon substrate and ferroelectric thin film. This degrades the device performance resulting in process integration problems and degradation of retention time.[3–9] This problem was resolved by depositing an insulating layer between silicon substrate and ferroelectric layer forming MFIS structure, which results in improved retention time.[10–12] The insulating material for this structure should have relatively high dielectric constant, good interface with silicon substrate, low leakage, and good thermal stability.[13,14] While, ferroelectric materials in aforesaid structure should have high-κ, low leakage, long data retention, high P_r value, low E_c, and low crystallization temperature.[13,14] Numerous attempts have been made to make FeRAM using ZrO_2,[3,15] HfO_2,[5,16,17] Al_2O_3,[9] Y_2O_3,[12,18] Dy_2O_3,[19] MgO,[20] La_2O_3,[21] TiO_2,[22] and TiAlO[23] as insulator and $Pb(Zr_xTi_{1-x})O_3$ (PZT),[9,18–21] $SrBiTaO_9$ (SBT),[5] $BiFeO_3$[3,12] as ferroelectric material in MFIS structures. However, there is very limited work on MFIS structure with thin ferroelectric films thinner than 60 nm. Recently, the ability to engineer ferroelectricity in HfO_2 (10 nm)[24] has motivated the scientific community to scale FeRAM further, but this 1T-1C structure requires separate switching (1T) and storage circuit (1C), hence demands additional area as compared to 1T-MFIS structure.[1] Moreover, the 10 nm Si-doped HfO_2 in MFIS structure was also investigated but showed a much lower fatigue of $\sim 10^4$ cycles[25,26] as compared to PZT. In fact for FeRAM to be the strong candidate for future universal memory,[2] it is necessary to accomplish the high density projected goals for next generation FeRAM technology node.[1] Thus, it becomes imperative to study the characteristics of MFIS structures with thin ferroelectric layers and ultrathin buffer layers for next technology node. However, the ferroelectric materials are unfamiliar and might be degraded by the conventional CMOS processing. Thus, the buffer, ferroelectric materials, and device processing conditions for FeRAM are still being refined.[1]

Recently, metal-ferroelectric-nitride-semiconductor (MFNS) structure showed its strong candidature for FeRAM device applications as compared to metal-ferroelectric-oxide-semiconductor (MFOS) structure.[27] However to achieve future scaling, nitride layer must be replaced by a high-κ dielectric. Formerly, TiO_xN_y films showed higher resistance to interfacial oxide formation, an excellent diffusion barrier[28,29] and high dielectric constant, which allows proportionally higher voltages to be applied across ferroelectric layer.[19] Still, there is very limited effort on the investigation of ultrathin ($\sim$ 6 nm) TiO_xN_y as an alternate buffer material and thin ($\sim$ 20 nm) PZT layers in MFIS structure for next generation FeRAM device applications to the best of authors knowledge. High dielectric constant, high P_r value, and low crystallization temperature of PZT make it suitable for FeRAM application as compared to other ferroelectrics.[13] MFIS structures with BFO(250 nm)/TiO_2(150 nm),[30] SBT(300 nm)/

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HfO_2(6 nm),[5] and PZT(160 nm)/La_2O_3(16 nm)[21] have been reported with ΔW of 0.5 V at ±5 V, 1.1 V at ±5 V, 0.65 V at −2 to +6 V, and 0.7 V at ±7 V, respectively. The leakage current density (J) reported in BFO(250 nm)/TiO_2(150 nm)[30] is of order 10^{-7} A/cm^2 at +5 V. The most advanced MFIS structure till date is Metal/SBT(300 nm)/HfO_2(6 nm)/Si with ΔW of 0.65 V at −2 to+6 V cyclic sweep and 10 years extrapolated retention time.[5] Previous experimental results show that stress[31] has significant effect on polarization of ferroelectrics.[17] Thus, it becomes necessary to study the behaviour of MFIS structures under CVS to check reliability of FeRAM devices especially at lower ferroelectric and buffer layer thicknesses. In this letter, first time employed ultrathin 6 nm TiO_xN_y as buffer and thin 20 nm PZT as ferroelectric films were chosen for fabrication of MFIS structure of FeRAM deposited by RF magnetron sputtering. The ΔW, retention analysis, and J, of fabricated devices were investigated with and without stress by Capacitance-Voltage (C-V), Capacitance-Time (C-T), and Leakage Current Density-Voltage (J-V) characteristics, respectively, supported by proposed model. The crystallinity of deposited ultrathin and thin films was analyzed by X-ray diffraction (XRD).

The MFIS capacitors were fabricated on 2-in. P-type ⟨100⟩ oriented silicon wafers (1–10 Ω cm). After standard RCA cleaning, deposition of TiO_xN_y films was carried out by radio frequency (R.F) magnetron sputtering at R.F power 90 W, 3.9×10^{-2} Torr, pressure of Ar/N_2 (60:19 sccm), and temperature of 300 K. These ultrathin films of TiO_xN_y deposited Si wafers were annealed at 873 K for 30 min in N_2 ambient. Subsequently, the deposition of PZT thin films was followed by R.F magnetron sputtering at R.F power 120 W, 1.8×10^{-2} Torr pressure of Ar and temperature of 300 K. The PZT deposited samples were annealed at 973 K for 60 min in inert ambient. For gate electrodes, Au thin film (∼100 nm) was deposited by RF magnetron sputtering at 3.9×10^{-2} Torr pressure of Ar and gate electrodes of area 3.855×10^{-3} cm^2 are patterned through the standard photolithography and chemically etching techniques. The thickness of deposited TiO_xN_y and PZT thin films was measured by Accurion EP3 imaging ellipsometer. The C-V, C-T, and J-V, without and with CVS were carried out at room temperature using KEITHLY 4200 SCS system. The C-V characteristics are taken at 1 MHz frequency and 0.01 V/s sweep rate. The orientations and crystallinity of the deposited thin films were analyzed using XRD with Cu-Kα radiation.

Figure 1 represents the cyclic C-V characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structures of FeRAM measured for forward −5 to +5 V [accumulation to inversion] gate voltage sweep and for reverse +5 to −5 V [inversion to accumulation] gate voltage sweep at 1 MHz frequency in conjunction with external stress voltage of 0, 5, 10, and 15 V, respectively. The C_{max} and C_{min} of FeRAM memory measured from the cyclic voltage sweep without stress is 331 and 34 pF, respectively. The ΔW defined by the flatband voltage (V_{fb}) shift from forward and back sweep[21] is ∼1.05 V calculated from C-V characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS system at cyclic sweep voltage of ±5 V indicated at (i) of Figure 1. The cyclic C-V curve shows a hysteresis loop with a clockwise trace indicating the polarization in PZT suitable for non-volatile FeRAM applications.[21] The

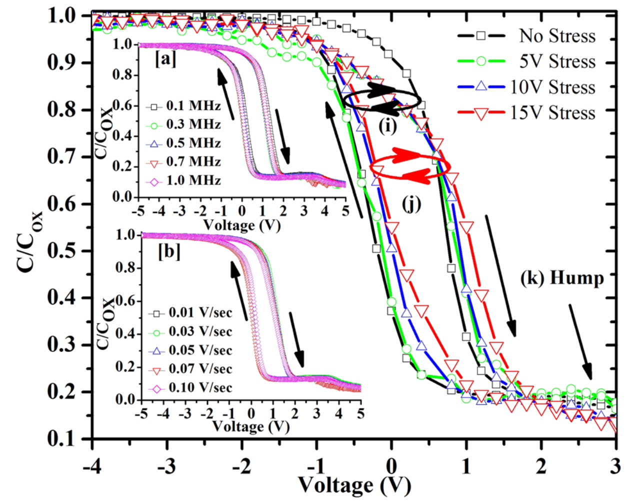

FIG. 1. Normalized C-V characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, (MFIS) structure at different stress voltages. Inset shows C-V characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si (MFIS) devices at different frequencies (a) and at different sweep rates (b).

experimental memory window width is close to the theoretical results obtained from[21]

$$\Delta W \approx 2 d_f E_C - \Delta V_{FB,ci}, \quad (1)$$

where d_f is the thickness of PZT, E_C is the coercive electric field, and $\Delta V_{FB,ci}$ is flat band voltage shift caused by charge injection. The voltage drop across ferroelectric is given by[21]

$$\frac{V_f}{V_i} = \frac{D_f}{D_i} * \frac{\varepsilon_f}{\varepsilon_i}, \quad (2)$$

where V_f, V_i are the voltage across ferroelectric and insulator, respectively. D_f, ε_f, and D_i, ε_i are the thickness, dielectric constant of ferroelectric and insulator thin films, respectively. The calculated ΔW (∼1.05 V) of fabricated devices with PZT(20 nm)/TiO_xN_y(6 nm) is certainly comparable to 1.1 V with BFO(250 nm)/TiO_2(150 nm) reported by Xie *et al.*[30] at ±6 V sweep voltage. The V_{fb} of FeRAM memory calculated for forward −5 to +5 V gate voltage sweep along with external stress voltage of 0, 5, 10, and 15 V are 0.55, 0.68, 0.70, and 0.80 V, respectively. There is insubstantial variation in V_{fb} (∼ 0.25 V) noticed under CVS as shown at (i) and (j) of Figure 1. This shift in V_{fb} as a result of CVS may be attributing to the presence of fairly significant number of defects at the TiO_xN_y/Si interface. Additionally, the cyclic C-V hysteresis curves at (i) and (j) of Figure 1 show the variation of FeRAM memory window (ΔW) ∼ 0.05 V with increase in stress voltage from 0 to 15 V. The observed variation in hysteresis may be attributed to the trapping and de-trapping mechanism at the TiO_xN_y/Si system and not due to dielectric polarization or ionic displacement (e.g., Na^+, K^+, etc.).[32] When the gate voltage approaches the weak inversion region, de-trapping of the trapped charges occurs by charge exchange with the Si substrate. The proposed structure at the weak inversion does not favour strong intrinsic trapping sites in TiO_xN_y of TiO_xN_y/Si system. However, the amount of charge de-trapped at TiO_xN_y should be sufficient to cause the shift in V_{fb} as observed in the curve after CVS as depicted in the cyclic C-V curve at (i) and (j) of Figure 1. Therefore, the

reduction in memory window after CVS indicates the reduction in traps at the Si/TiO_xN_y system. Further, there is an interesting hump noticed in all reversed C-V curves as shown at (k) in Figure 1, signifying the strong de-trapping of intrinsic trapped charges of TiO_xN_y/Si structure during reverse sweep. As conveyed by the C-V curves, this hump vanishes after CVS. It indicates the traps at TiO_xN_y/Si system get reduced upon increasing the CVS. The interface traps, mobile ions, bulk traps, and impurities in high-κ layer can also cause charge effect and hence hysteresis in C-V curves. Thus, frequency dependent measurements are performed on Au/PZT(20 nm)/TiO_xN_y(6 nm)/Si, MFIS structure as shown in inset (a) of Figure 1 to study this effect, since interface traps do not respond fast enough in high frequency range.[33] The Memory window shows an insignificant change with frequency variation from 0.1 MHz to 1 MHz. Thus, memory window is due to polarization of PZT thin films and not due to interface traps. To confirm the effect of mobile ionic charges and interfacial polarization on hysteresis, memory window is observed with variation in sweep voltage from 0.01 to 0.1 V/s. The inset (b) of Figure 1 shows the C–V characteristics of FeRAM devices with Au/PZT(20 nm)/TiO_xN_y(6 nm)/Si, MFIS structure with different sweep rates. The memory window of Au/PZT(20 nm)/TiO_xN_y(6 nm)/Si, MFIS structure remains consistent around ~1 V regardless of variation in sweeping speed. This confirms that memory window is primarily determined by the ferroelectric polarization of PZT thin film and other factors have minor impact.[5]

For real FeRAM device applications, it is essential to check retention time behaviour of FeRAM MFIS structures. Figure 2 shows the retention characteristics of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, FeRAM MFIS structures, characterized through the C–T analysis. The inset of Figure 2 shows the experimental data in linear time scale. In this systematic investigation, the proposed MFIS device is applied a write pulse of ±5 V in height and 100 ms in duration, followed by a read voltage near flatband voltage of 1.5 V.[17] Here, the write pulse of −5 V corresponds to C_H and that of +5 V correspond to C_L. For the first 1000 s, exponential decay and rise was observed in C_H and C_L, respectively. After this, the capacitance values decay linearly w.r.t time. Thus, linear extrapolation is done after 1000 s. As shown in Figure 2, the difference in capacitance magnitudes ($\Delta C = C_H - C_L$) is evidently distinguishable for 5000 s even if we extrapolate[34,35] the experimental data to 15 years, which is desired for next generation non-volatile memories.[1] It is clearly seen in inset of Figure 2 that the slope of C_H (Figure 2(a)) becomes positive and C_L (Figure 2(b)) becomes negative, i.e., ΔC increases under CVS, hence result in improvement of retention time of FeRAM devices, which is in agreement with the leakage current density results with CVS shown in Figure 3.

Figure 3 shows the gate leakage current density (J) as a function of gate sweep voltage (V_g). The low leakage current density (J) of 55.7×10^7 A/cm^2 of fabricated devices with 6 nm TiO_xN_y is greatly superior to 150 nm TiO_2 reported by Xie *et al.*[29] with J of order 10^7 A/cm^2 at +5 V sweep voltage. The measured gate leakage current for Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, FeRAM MFIS structures at dc voltage of 5 V along with stress voltage of 0, 5, 10, and 15 V are 5.57, 2.41, 2.22, and 1.94 μA/cm^2, respectively. It is apparent that with the variation in stress voltage from 0 to 15 V, there is enduring reduction in gate leakage current by a factor 3.63 μA/cm^2, which is probably because of decrease in the intrinsic trapping sites in TiO_xN_y of TiO_xN_y/Si system. Clogging of neutral defects may result in deep trap so that electrons are no longer available for conduction.[36] This considerable higher strength to stress voltage is an indication of the elevated reliability and feasibility to use Au/PZT(20 nm)/TiO_xN_y(6 nm)/Si, MFIS structures for FeRAM device applications.

Figure 4(a) shows the XRD pattern of ultrathin TiO_xN_y films deposited on Si, followed by annealing at 873 K. The TiO_xN_y thin films exhibited a high (111) orientation with relatively small (220), (304), and (400) peaks. The most stable tetragonal rutile phase of TiO_2 (110) is also observed along with small peak of anatase TiO_2 (111). Figure 4(b) shows the XRD pattern of PZT-Si structure annealed at 873 K, which confirms the presence of perovskite phase of PZT film, which is one of prime importance for the excellent remanent polarization. The PZT thin film exhibited (100) along with (220) preferred orientation, which are the best phases for good fatigue endurance and higher remanent polarization,

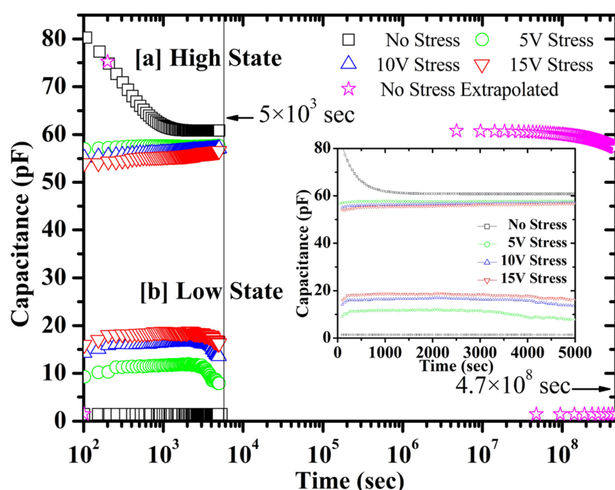

FIG. 2. C-T of Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si (MFIS) structure showing retention characteristics.

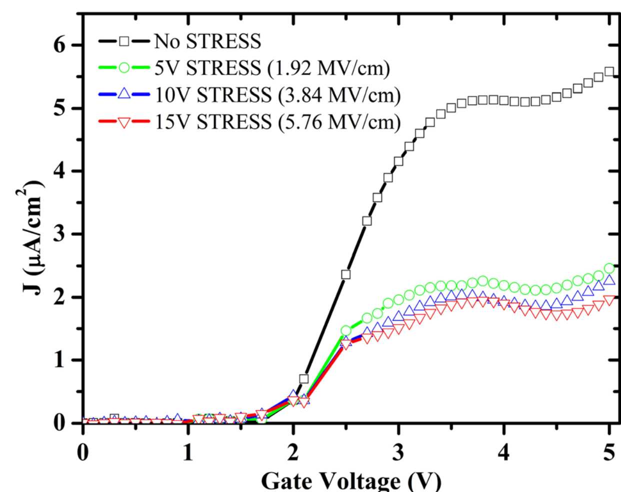

FIG. 3. Leakage current density for Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si, MFIS structures at different stress voltages.

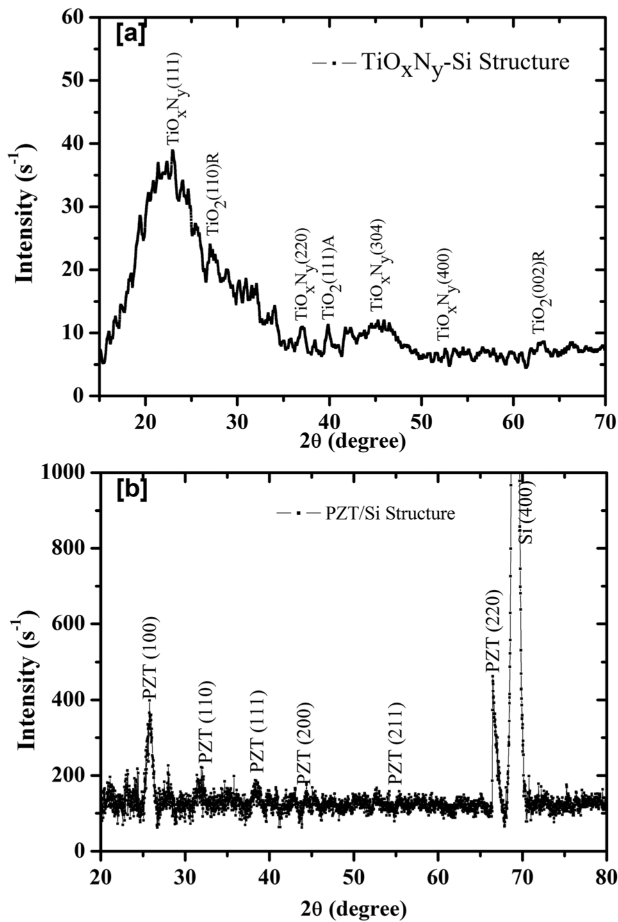

FIG. 4. XRD pattern of (a) TiO_xN_y-Si and (b) PZT-Si structures.

respectively,[37] along with relatively small (110), (111) peaks.

Figure 5 shows the energy band diagram of Au/PZT(20 nm)/TiO_xN_y(6 nm)/Si, MFIS structure, using the work function of Au as 5.1 eV, PZT electron affinity as 2.15 V, PZT energy band gap[38] as 3.4 V and assuming the TiO_xN_y energy band gap[39] as ~2 eV. In Figure 5(a), when $V_g < 0$, device is in accumulation and traps are occupied in TiO_xN_y due to stress voltage. In Figure 5(b), when $V_g > 0$, device is in onset

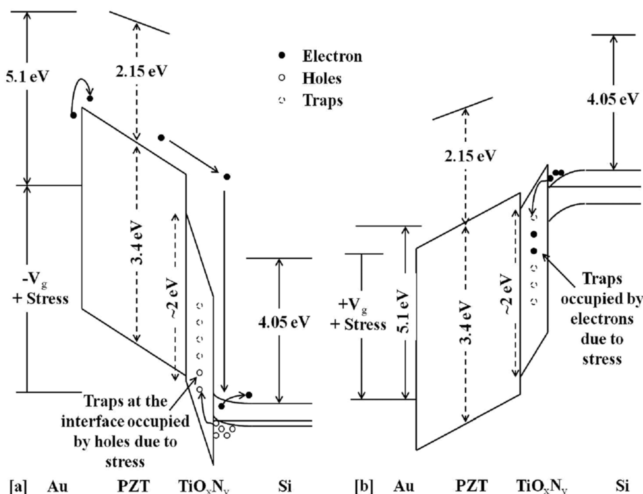

FIG. 5. Energy band diagram for Au/PZT (20 nm)/TiO_xN_y (6 nm)/Si under CVS with (a) $-V_g$ + Stress and (b) $+V_g$ + Stress.

of inversion region with small barrier height at TiO_xN_y/Si interface. The charge carriers trapped in TiO_xN_y result in the decrease of J with increase of stress due to decrease in intrinsic trapping sites in TiO_xN_y of TiO_xN_y/Si system and clogging of oxide neutral traps, which do not participate in conduction.

In Summary, MFIS structure of FeRAM was fabricated using ultrathin 6 nm TiO_xN_y buffer and thin 20 nm PZT ferroelectric films on p-Si by RF-magnetron sputtering and annealed in N_2 ambient. The electrical characteristics of fabricated devices were analyzed under CVS to test their reliability. It is shown that with the variation in CVS from 0 to 15 V, there is trivial alteration in V_{fb} (~ 0.25 V) and ΔW (~ 0.05 V). Moreover, the clockwise ΔW of ~1.05 V showed insignificant variation in C-V characteristics with variation in frequency and sweep rate. This signified the excellent TiO_xN_y/Si interface and confirms that memory window is due to polarization of PZT thin films and other factors like interface traps, mobile ions have minor impact. The reduction in gate leakage current by a factor 3.63 $\mu A/cm^2$ under CVS suggests the decrease in intrinsic trapping sites and clogging of neutral defects in TiO_xN_y and hence the improvement of retention characteristics of fabricated Au/PZT(20 nm)/TiO_xN_y(6 nm)/Si, MFIS FeRAM devices extrapolated beyond 15 years. Thus, MFIS FeRAM gate stacks with TiO_xN_y as buffer layer and PZT as ferroelectric layer is a potential candidate for long retention FeFET.

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