ResearchGate

See discussions, stats, and author profiles for this publication at: https://www.researchgate.net/publication/337966146

Alternate lanthanum oxide/silicon oxynitride-based gate stack performance enhancement due to ultrathin oxynitride interfacial layer for CMOS applications

Article *in* Journal of Materials Science Materials in Electronics · December 2019

DOI: 10.1007/s10854-019-02718-7

CITATIONS
0

READS
53

3 authors:

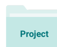
Prachi Gupta
Indian Institute of Technology Mandi
3 PUBLICATIONS 0 CITATIONS
SEE PROFILE

Mahesh Soni
University of Glasgow
40 PUBLICATIONS 219 CITATIONS
SEE PROFILE

Satinder K. Sharma
Indian Institute of Technology Mandi
110 PUBLICATIONS 610 CITATIONS
SEE PROFILE

Some of the authors of this publication are also working on these related projects:

Graphene based nanocomposites for photocatalytic water purification View project


RERAM devices View project

All content following this page was uploaded by Prachi Gupta on 23 December 2019.

The user has requested enhancement of the downloaded file.

Journal of Materials Science: Materials in Electronics
https://doi.org/10.1007/s10854-019-02718-7

Alternate lanthanum oxide/silicon oxynitride-based gate stack performance enhancement due to ultrathin oxynitride interfacial layer for CMOS applications

Prachi Gupta[1] · Mahesh Soni[1] · Satinder K. Sharma[1]

Received: 6 September 2019 / Accepted: 6 December 2019
© Springer Science+Business Media, LLC, part of Springer Nature 2019

Abstract

Metal–insulator–semiconductor (MIS)-based Pt/La_2O_3/SiO_XN_Y/p-Si/Pt structures are fabricated using ultrathin silicon oxynitride (SiO_XN_Y ~ 4 nm) interfacial layer underneath of lanthanum (III) oxide (La_2O_3 ~ 7.8 nm) with Pt as gate electrode for CMOS applications. Capacitance–voltage (*C–V*) characteristics of Pt/La_2O_3/SiO_XN_Y/p-Si/Pt at 500 kHz showed a positive gate bias threshold voltage (V_{th}) shift of ~ 0.43 V (~ 43.8%) and flat-band (V_{fb}) shift of ~ 1.24 V (~ 42.3%) as compared to Pt/La_2O_3/p-Si/Pt MIS structures, attributing to the reduction in effective positive oxide charges at La_2O_3/SiO_XN_Y/Si gate stack. Likewise, conductance–voltage (*G–V*) characteristics show ~ 0.56 (~ 44.4%) reduction in FWHM for Pt/La_2O_3/SiO_XN_Y/p-Si/Pt as compared to Pt/La_2O_3/p-Si/Pt MIS structures revealing the reduction in interface states at La_2O_3/SiO_XN_Y/Si interface. There is a considerable reduction of effective oxide charge concentration (N_{eff}) ~ 3.99×10^{10} cm^{-2} by (~ 15.2%) and ~ 56.8% lower gate leakage current density ~ 4.47×10^{-7} A/cm^2 (|*J*|–*V*) at − 1 V for SiO_XN_Y based MIS structures w.r.t its counterpart. Capacitance–time (*C–t*) characteristics, constant voltage stress (CVS) and temperature measurements for *C–V* and |*J*|–*V* demonstrate the considerable retention ~ 12 years, electrical improvement and reliability of MIS structures. The depth profile analysis X-ray photoelectron spectroscopy (XPS) for SiO_XN_Y/Si gate stack clearly reveals that less nitrogen concentration in bulk than SiO_XN_Y/Si interface. Atomic force microscopy (AFM) micrographs of La_2O_3/Si and SiO_XN_Y/Si showed the significantly lesser r.m.s roughness of ~ 1.11 ± 0.39 nm and ~ 0.97 ± 0.11 nm, respectively. Thus, the ultrathin SiO_XN_Y interfacial layer underneath of La_2O_3 demonstrates a significantly improved electrical performance and prelude the gate stack strong potential for reliable CMOS logic devices and integrated circuits.

1 Introduction

As Moore's scaling law becomes less effective in CMOS technology beyond 90 nm, high-*κ* dielectrics especially rare-earth oxides attract significant attention from scientific and industrial community for high-performance CMOS devices [1]. Scaling of traditionally used gate dielectric silicon dioxide SiO_2 (~ 1.2 nm) comes with its own inherent fundamental material science and technological challenges leading towards large gate leakage current density (|*J*|) (~ > 1 A/cm^2), which may be attributed to quantum mechanical tunnelling, higher interface defects, subthreshold swing, boron penetration and stress-induced leakage, etc. [1–4]. Hence, to drive the CMOS technology scaling towards the next-generation technology node, one of the possible solutions is to find an alternate dielectric to replace thin SiO_2 layer with an alternate high-*κ* or gate dielectric stack, demonstrating improvements in equivalent oxide capacitance, equivalent oxide thickness (EOT) and lower gate leakage current density |*J*| as per current technology node [3, 5].

High-*κ* oxides with *κ* (dielectric constant) value > 12 (preferably ~ 25 to ~30), large band offset > 1 eV and wide band gap > 5 eV are preferred choices for alternate gate dielectric materials. There are several high-*κ* oxides demonstrating properties as discussed above includes Al_2O_3, ZrO_2, HfO_2, Y_2O_3, Er_2O_3 and La_2O_3 [6–11]. Among these, rare-earth lanthanum (III) oxide (La_2O_3) has attracted immense attention from scientific and industrial community due to high-*κ* (~ 25 to ~30), wide-band gap (~ 6 eV), conduction band offset (~ 2.3 eV) and thermodynamic stability [5, 12]. Despite several advantages of La_2O_3, there are still few

✉ Satinder K. Sharma
satinder@iitmandi.ac.in

[1] School of Computing and Electrical Engineering (SCEE), Indian Institute of Technology (IIT) Mandi, Mandi, Himachal Pradesh 175005, India

Published online: 16 December 2019

reports in literature demonstrating highly reactive nature of La_2O_3 with silicon (Si) causing formation of Lanthanum Hydroxide ($La(OH)_3$) at interface [13] resulting in poor interface with Si, thermal instability, high interface trap-density and leakage current-density $|J|$ [5, 14, 15]. Also, higher density of interfacial fixed oxide charges and interface trap levels are extremely undesirable hence high-κ materials such as Al_2O_3 [16–18], HfO_2 [19, 20], TiO_2 [21], La_2O_3 and Y_2O_3 [22] are preferred for futuristic CMOS configurations. Thus, posing challenges for its use in high-performance CMOS devices for lower technology node.

In order to encounter these fundamental concerns and improve the interface of Si with the traditionally used high-κ oxides, controlled incorporation of fluorine and chlorine, oxynitridation of SiO_2 or use of heterogenous gate dielectrics are reported as one of the possible solutions [13, 23–26]. Moreover, there is a report from IBM about the use of silicon oxynitride (SiO_XN_Y) interfacial layer for high-performance logic devices over its counterpart due to its improved interface with Si resulting in the lower $|J|$ and adjustment of threshold voltage (V_{th}) [24, 27]. To cope up with the interface issue, in the present investigations, ultrathin oxynitridation of Si, SiO_XN_Y was used as interfacial layer (underneath) for the uniform deposition of La_2O_3 [9, 28]. Not only the use of ultrathin silicon oxynitride (SiO_XN_Y) interfacial layer improves the interface with Si, but it will also prevent the formation of $La(OH)_3$ (as discussed previously), which will further boost the next-generation CMOS devices' performance and stability [13]. In addition, detailed discussions on the use of SiO_XN_Y over its counterparts can found in [15, 16, 24, 29–36].

Therefore, the present work investigates the performance of fabricated metal–insulator–semiconductor (MIS) structures, $Pt/La_2O_3/SiO_XN_Y$/p-Si/Pt and Pt/La_2O_3/p-Si/Pt, with and without the presence of ultrathin SiO_XN_Y interfacial layer. The performance of the gate stacked memory devices was systematically investigated based on electrical, optical and spectroscopy techniques. The electrical measurements were performed using Keithley 4200 semiconductor characterization system (SCS) attached to the probe station through tri-axial cables. To study and analyse electrical properties such as charge storage capability and retention, capacitance–voltage (C–V) with varying frequencies and capacitance–time (C–t) measurements were performed, respectively. In addition to this, to study the stability and reliability of the MIS structures, $|J|$–V measurements with varying temperature and C–V measurements with varying constant voltage electrical stress (CVS) were performed. The thickness, interface properties and surface roughness of the deposited ultrathin layers have been characterized using ellipsometry, XPS and atomic force microscope (AFM), respectively.

2 Experiment

2.1 Fabrication of MIS devices

The process flow for the fabrication of two different MIS structures, Pt/La_2O_3(~ 7.8 nm)/p-Si/Pt and Pt/La_2O_3(~ 7.8 nm)/SiO_XN_Y(~ 4 nm)/p-Si/Pt, are shown in schematic Fig. 1a, b, respectively. Two sets of 2-inch p-type ⟨100⟩ silicon wafers with resistivity of 2–10 Ω-cm were used as substrates for fabrication of $Pt/La_2O_3/SiO_XN_Y$/Si/Pt and Pt/La_2O_3/Si/Pt, MIS structures. For high quality and uniform deposition of ultrathin SiO_XN_Y tunnel dielectric, one set of RCA cleaned Si wafers were loaded to rapid thermal oxidation (RTO) (AS–One, ANNEALSYS, France Make) at 25 °C under N_2 flow ~ 800 sccm and the temperature was then raised to 900 °C at a ramp rate of ~ 25 °C/s. Followed by this, the wafers were subjected to nitrous oxide flow ~ 800 sccm at 900 °C for 90 s, resulting in oxide growth on both sides of wafer in SiO_XN_Y/p-Si/SiO_XN_Y structure (as shown with the help of Fig. 1b1, b2). Afterwards, the SiO_XN_Y/p-Si/SiO_XN_Y samples were subjected to back-side etch to result in SiO_XN_Y/p-Si (as shown in Fig. 1b3). For back-side

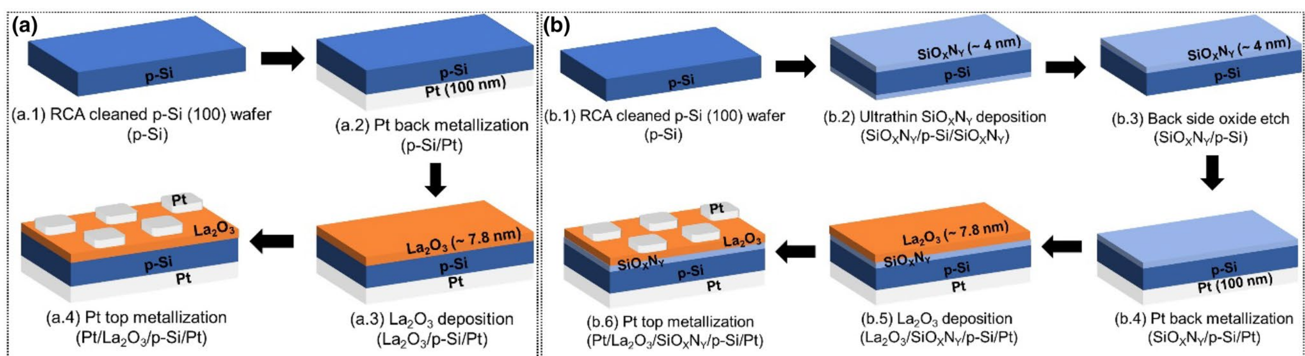


Fig. 1 **a** Schematic of Pt/La_2O_3/Si/Pt MIS structures. **b** Schematic of $Pt/La_2O_3/SiO_XN_Y$/Si/Pt MIS structures

metallization, the samples (SiO_XN_Y/p-Si and second set of RCA cleaned p-Si) were loaded into sputtering chamber, where ~100 nm of platinum (Pt) was sputtered at a pressure of $\sim 6\times10^{-3}$ torr at 60 W to result into SiO_XN_Y/p-Si/Pt (shown in Fig. 1b4) and p-Si/Pt (shown in Fig. 1a2). For the deposition of uniform and thin La_2O_3 film, the samples SiO_XN_Y/p-Si/Pt and p-Si/Pt were again loaded into the sputtering chamber with La_2O_3 target (purity 99.99%) and the chamber was pumped down to $\sim 7.2\times10^{-7}$ torr. Through out the sputtering process, the base pressure and process pressure were maintained at $\sim 7.2\times10^{-7}$ torr vacuum. Prior to sputtering on silicon wafers, pre-sputtering was carried out at 60 W for 10 min to remove impurities present on the target surface. Deposition of thin film was carried out at 300 K, RF power 60 W and pressure of ultrapure (99.9999%) Ar ~ 80 sccm.

For in-situ post-deposition annealing (PDA), both sets of resulting samples La_2O_3/SiO_XN_Y/p-Si/Pt (shown in Fig. 1b5) and La_2O_3/p-Si/Pt (shown in Fig. 1a3) were subjected to 700 °C for 30 min with ramp up rate of 35 °C/min at chamber pressure of $\sim 5.2\times10^{-6}$ torr. For the top electrode formation, Pt thin films ~ 100 nm were sputtered at process pressure of $\sim 5.0\times10^{-3}$ torr patterned using a shadow mask with a circular area of $\sim 4.37\times10^{-3}$ cm^2 for the Pt/La_2O_3/SiO_XN_Y/p-Si/Pt (shown in Fig. 1b6) and Pt/La_2O_3/p-Si/Pt (shown in Fig. 1a4) metal-insulator-semiconductor (MIS) structures.

2.2 Characterizations

The fabricated Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt and Pt/La_2O_3(PDA)/Si/Pt MIS structures were electrically characterized at room temperature for capacitance-voltage (*C–V*) (with variable frequencies, CVS, and sweep delays), gate leakage current density–voltage (|*J*|–*V*) (with variable temperatures and CVS) and capacitance–time (*C–t*) measurements using Keithley 4200 SCS system. To confirm the formation of ultrathin SiO_XN_Y layer on p-Si, the SiO_XN_Y/Si samples were placed in Thermo scientific XPS chamber pumped to pressure of $\sim 1\times10^{-9}$ mbar with Al-K_α X-ray source, for the bonding nature and elemental analysis of constituent species. The thickness of the RTO grown SiO_XN_Y was measured ~ 4 ± 0.2 nm by J. A. Woolman Imaging Ellipsometer [37]. The thickness of deposited La_2O_3 dielectric film was measured ~ 7.8 ± 0.2 nm by Accurion EP_4 imaging ellipsometer. The EOT of gate stack La_2O_3/SiO_XN_Y dielectric layers can be computed by the following relation as given by Eq. (1) [2, 28]:

$$\mathrm{EOT} = \varepsilon_{\mathrm{SiO_2}}\left(\frac{t_{k1}}{\kappa_{k1}} + \frac{t_{k2}}{\kappa_{k2}}\right). \tag{1}$$

Here, t_{k1} and t_{k2} are the thickness of individual gate dielectric La_2O_3 (~ 7.8 nm) and SiO_XN_Y (~ 4 nm) layers, respectively, ε_{SiO_2} is the optical dielectric constant of silicon dioxide (SiO_2), and κ_{k1} and κ_{k2} are the individual optical dielectric constants of gate dielectric La_2O_3 ($\kappa \sim 24.60$) and SiO_XN_Y ($\kappa \sim 6.76$) layers, respectively, as measured by Accurion EP_4 imaging ellipsometer. The EOT of gate dielectric La_2O_3/SiO_XN_Y stack was calculated as ~ 2.71 nm for Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures. The measured (r.m.s) surface roughness of La_2O_3/Si and SiO_XN_Y/Si thin films by atomic force microscopy (AFM) was ~ 1.11 ± 0.39 nm and ~ 0.97 ± 0.11 nm, respectively.

3 Results and discussion

3.1 Electrical characterizations

Figure 2a shows the capacitance-voltage (*C–V*) characteristics of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt (I) and Pt/La_2O_3(PDA)/Si/Pt (II) MIS structures, at room temperature. Measured *C–V* characteristics from positive (+ 2 V) to negative (− 4 V) bias voltages, (inversion, depletion and accumulation regions) are shown in Fig. 2a for Pt/La_2O_3/SiO_XN_Y/Si/Pt (I) and Pt/La_2O_3/Si/Pt (II) MIS structures, at 500 kHz. As clearly reveals from Fig. 2a, there is significant positive gate bias (right side) shift in threshold voltage (V_{th}) and also flat-band voltage (V_{fb}) of Pt/La_2O_3/SiO_XN_Y/Si/Pt with respect to Pt/La_2O_3/Si/Pt MIS structures. The computed flat-band voltage (V_{fb}) and threshold voltage (V_{th}) from Fig. 2a *C–V* curves at 500 kHz are ~ − 1.69 V and ~ − 0.55 V for Pt/La_2O_3/SiO_XN_Y/Si/Pt MIS structure and ~ − 2.93 V and ~ − 0.98 V for Pt/La_2O_3/Si/Pt MIS structure, respectively. The noticeable positive gate side shift of ~ 1.24 V (~ 42.3%) in V_{fb} and ~ 0.43 V (~ 43.8%) in V_{th} clearly indicates the reduction of effective positive oxide charges at La_2O_3/SiO_XN_Y/Si interface, with incorporation of ultrathin SiO_XN_Y interfacial layer in La_2O_3/p-Si structure [38]. Also, the presence of SiO_XN_Y interfacial layer prevents the formation of thermodynamically unstable La–O/Si–O bonds, thus resulting in highly stable Si–O–Si and Si–N bonds passivating the interface against diffusion of impurities into silicon [6, 8, 32]. Figure 2b (inset) shows the *C–V* characteristics with variation in frequency from 500 kHz to 1 MHz with step voltage of 100 kHz for Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures at room temperature. The variation in oxide capacitance (C_{ox}) from ~ 23.20 to ~ 7.93 nF/cm^2 is observed as a function of frequency variation from 500 kHz to 1 MHz, respectively. In addition, from Fig. 2b with increase in frequency, accumulation capacitance is observed to decrease. This decrease in accumulation capacitance indicates the frequency dispersion of capacitance in accumulation region, which may be due to the presence of frequency-dependant interface states in the

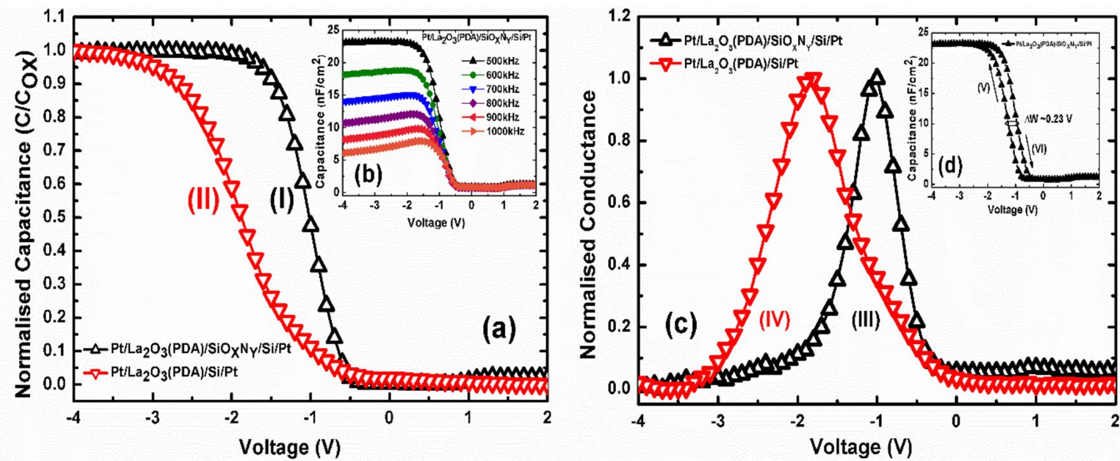


Fig. 2 **a** C/C_{OX}–V characteristics of (I) Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt and (II) Pt/La_2O_3(PDA)/Si/Pt MIS structures at 500 kHz. **b** (inset) C–V characteristics of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures at 500 kHz to 1 MHz with a step of 100 kHz. **c** G–V characteristics of (III) Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt and (IV) Pt/La_2O_3(PDA)/Si/Pt MIS structures. **d** (inset) Cyclic C–V characteristics of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures at 500 kHz

MIS structures, whereas there is an insignificant frequency dispersion noticed in the inversion region. Also, the positive (right) shift of flat-band voltage (V_{fb}) ~ 0.18 V and threshold voltage (V_{th}) ~ 0.19 V are observed at 1 MHz frequency, as compared to 500 kHz C–V characteristics. This variation in V_{fb} and V_{th} with variation in frequency may be attributed due to the frequency-dependant border traps/slow and fast states located close to the La_2O_3/SiO_XN_Y and SiO_XN_Y/Si interface or mobile charges exchange [4, 15].

Figure 2c depicts the conductance–voltage (G–V) characteristics of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt (III) and Pt/La_2O_3(PDA)/Si/Pt (IV) MIS structures. In the depletion region, the maximum conductance (G_{p_max}) peaks are obtained as ~ 1.77 mS at ~ − 1 V and ~ 1.37 mS at ~ − 1.8 V corresponding to Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt (III) and Pt/La_2O_3/Si/Pt (IV) MIS structures, respectively. The observed positive gate voltage side shift of corresponding G_{p_max} peaks must be due to incorporation of SiO_XN_Y layer and reduction of effective positive oxide charges at La_2O_3/SiO_XN_Y/Si interface. The full width at half-maximum (FWHM) of G–V curves is measured as ~ 0.70 and ~ 1.26 for Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt and Pt/La_2O_3/Si/Pt MIS structures, respectively. The considerable reduction in FWHM ~ 0.56 (~ 44.4%) reveals the reduction in interface states localized at La_2O_3/SiO_XN_Y/Si interface, for Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt (III) MIS structures. The observed difference in FWHM of (III) and (IV), G–V curves clearly reveals the improvement in the La_2O_3/Si interface with the incorporation of ultrathin SiO_XN_Y interfacial layer.

The effective oxide charge concentration (N_{eff}) in high-κ-based La_2O_3/SiO_XN_Y system is computed by following relation (2):

$$N_{eff} = \frac{C_{ox}(\emptyset_{ms} - V_{fb})}{qA}, \tag{2}$$

where N_{eff}, C_{ox}, $\emptyset_{ms}$, V_{fb}, q and A are effective oxide charge concentration, measured accumulation oxide capacitance, metal–semiconductor work function, flat-band voltage, electronic charge and gate area, respectively. Nicollian and Brews's [32] conductance-based technique is used to extract interface trap density (D_{it}) from the conductance–voltage (G–V) characteristics. The parallel conductance (G_p) is extracted from G–V curves corrected for series resistance effects [32, 39] as shown by the following relation (3):

$$G_p = \frac{\omega G C_{ox}^2}{G^2 + \omega^2 (C_{ox} - C_p)^2}, \tag{3}$$

where ω is angular frequency, given by $\omega = 2\pi f$, G is measured conductance, C_{ox} is measured accumulation oxide capacitance and C_p is depletion capacitance. Interface trap density D_{it} (eV^{-1} cm^{-2}) is extracted from the peak of G–V curve (G_{p_max}) as follows in Eq. (4) [32, 39]:

$$D_{it} = \frac{2.5}{qA} \frac{G_{p_max}}{\omega}. \tag{4}$$

The calculated values of N_{eff}, D_{it} and G_{p_max} are ~ 3.99 × 10^{10} cm^{-2}, ~ 2.20 × 10^{11} eV^{-1} cm^{-2} and ~ 1770.5 µS, respectively, for Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures.

Figure 2d (inset) shows the cyclic C–V (500 kHz) curve of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures with forward (VI) gate voltage sweep from accumulation (− 4 V) to inversion (+ 2 V) and reverse (V) gate voltage sweep from inversion (+ 2 V) to accumulation (− 4 V). The maximum accumulation capacitance C_{max} and minimum inversion

capacitance C_{min} of MIS structures measured from cyclic voltage sweep are ~ 23.20 nF/cm^2 and ~ 1.20 nF/cm^2, respectively. From the cyclic *C*–*V* curve, the following parameters are extracted at 500 kHz: flat-band voltage (V_{fb}) of ~ − 1.69 V and threshold voltage (V_{th}) of ~ − 0.55 V for Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures. The memory window (ΔW) defined by the flat-band voltage (V_{fb}) shift in forward (− 4 V to + 2 V) and reverse (+ 2 V to − 4 V) cyclic sweep is ~ 0.23 V. This insubstantial ΔW may be caused due to trapping and de-trapping of charges at La_2O_3/SiO_XN_Y/Si system [40].

Figure 3a represents the improved gate leakage current density–voltage (|*J*|–*V*) characteristics of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt (I) over Pt/La_2O_3(PDA)/Si/Pt (II) MIS structures at room temperature. The gate leakage current density of Pt/La_2O_3/SiO_XN_Y/Si/Pt and Pt/La_2O_3/Si/Pt MIS structures at − 1 V is ~ 4.47×10^{-7} A/cm^2 and ~ 1.02×10^{-6} A/cm^2, respectively. There is considerable ~ 5.73×10^{-7} A/cm^2 (~ 56.8%) reduction in leakage current density with the inclusion of ultrathin interfacial SiO_XN_Y interfacial layer due to the formation of Si–N–Si bonds, showing better dielectric interfacial properties. Also, the lower leakage current density for Pt/La_2O_3/SiO_XN_Y/Si/Pt MIS structures saturate at negative voltage ~ − 1 V bias as compared to Pt/La_2O_3/Si/Pt MIS where the current is varing gradually even at − 5 V voltage bias. As represented in |*J*|–*V* characteristics, the gate leakage current density of Pt/La_2O_3/SiO_XN_Y/Si/Pt MIS structures varies partially linearly as compared to Pt/La_2O_3/Si/Pt MIS structures, at positive bias voltage ~ 0.5 V, evidently indicating the improved La_2O_3/SiO_XN_Y/Si interface of MIS structures.

Figure 3b represents the $\ln(J) - \ln(E)$ and $\ln(J/E^2) - 1/E$ plots derived from |*J*|–*V* characteristics of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures to establish its current conduction mechanism. However, in ultrathin dielectric layer, some fraction of leakage current density may be attributed to its rate of (RTO) growth causing effective tunnelling thickness to be less than average thickness [41]. In $\ln(J) - \ln(E)$ current–conduction plot, there exists two regions, where Regions (III) and (IV) show the partially direct tunnelling (DT) current at low field E (MV/cm) and Fowler–Nordheim (F–N) tunnelling current at high field E (MV/cm) regions, respectively, as marked in Fig. 3b. The partially direct tunnelling current density (J_{DT}) at low E is modelled by following Eq. (5) [42]:

$$J_{DT} = qfnT, \tag{5}$$

where q, f, n and T are the electronic charge, impact frequency against the barrier, density of electrons available for tunnelling, and oxide transparency or transmission probability which depends on the oxide voltage, respectively. As shown in Fig. 3b (IV), the Fowler–Nordheim (F–N) tunnelling current density (J_{FN}) at high E is given by Eqs. (6), (7) [43]:

$$J_{FN} = AE^2 \exp \frac{-B}{E}, \tag{6}$$

$$B = \frac{\left(8\pi \sqrt{2m^*(q\emptyset_B)^3}\right)}{3qh}, \tag{7}$$

where E, A, m^*, q, h and $\emptyset_B$ are electric field (MV/cm), constant, effective mass of electron, electronic charge, Planck's constant and effective barrier height, respectively. For F–N tunnelling to be dominant, $\ln(J/E^2) - 1/E$ plot must be a straight line as depicted in Fig. 3b (V). In the Fig. 3b (IV) for values of E higher than 3 MV/cm, straight line of logarithmic

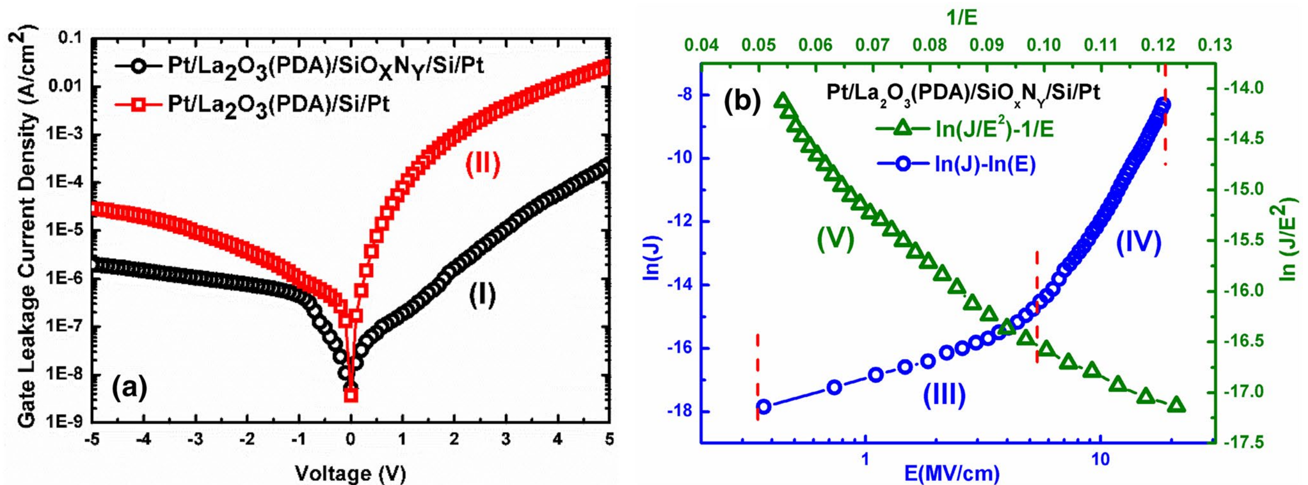


Fig. 3 **a** |*J*|–*V* characteristics of (I) Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt and (II) Pt/La_2O_3(PDA)/Si/Pt MIS structures. **b** Current conduction mechanism of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures in $\ln(J) - \ln(E)$ regions (III–IV) and $\ln(J/E^2) - I/E$ (*V*) plots, respectively

gate leakage current density depicts F–N tunnelling mechanism. Electrical characterizations investigated in Figs. 2 and 3 are in agreement with that, $Pt/La_2O_3/SiO_XN_Y/Si/Pt$ MIS shows significant improvement in interface properties with respect to $Pt/La_2O_3/Si/Pt$ MIS structures, with the inclusion of ultrathin SiO_XN_Y interfacial layer. Table 1 compares the electrical parameters of fabricated MIS structures investigated in this work, $Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt$ and $Pt/La_2O_3(PDA)/Si/Pt$, showing clear improvements in electrical performance of $Pt/La_2O_3/SiO_XN_Y/Si/Pt$ MIS structures.

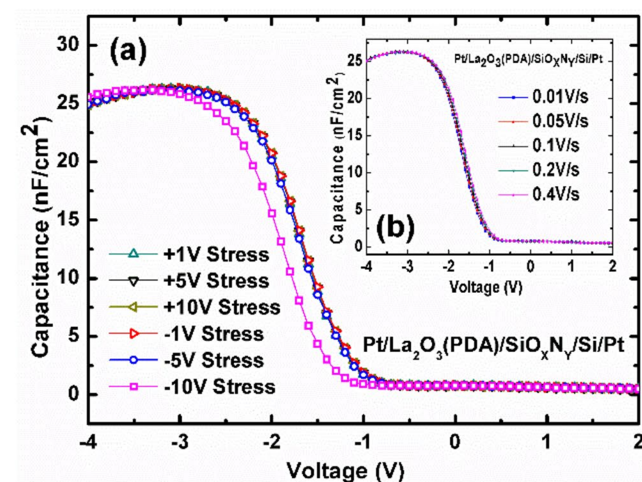
For reliability and stability investigations of fabricated $Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt$ MIS structures, constant voltage electrical stress (CVS), variable sweep delay and temperature measurements are performed. Figure 4a shows *C–V* characteristics ranging CVS from positive bias (+ 1 V, + 5 V, + 10 V) and negative bias (− 1 V, − 5 V, − 10 V) stresses. As perceives that with the application of positive stress, insubstantial change in threshold voltage (V_{th}) is observed, whereas, with the application of negative stress, there is a small negative (left) gate bias side shift in threshold voltage (V_{th}) ~ 0.27 V, especially at higher − 10 V stress. This V_{th} shift may be due to generation of more positive oxide charges in the MIS structures. To investigate the more prominent effects of mobile ionic charges for MIS structures, Fig. 4b (inset) shows the *C–V* characteristics with variation in sweep delay. With variation in sweep delay from 0.01 V/s, 0.05 V/s, 0.1 V/s, 0.2 V/s to 0.4 V/s, respectively, *C–V* characteristics of $Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt$ MIS show negligible change in threshold voltage (V_{th}) ~ 0.1 V. This evidently indicates the insignificant effect of mobile ionic charges in the $La_2O_3/SiO_XN_Y/Si$ systems.

Table 1 Electrical performance comparison

Electrical performance	$Pt/La_2O_3/SiO_XN_Y/Si/Pt$	$Pt/La_2O_3/Si/Pt$
C_{fb} (nF/cm^2)	22.25	35.75
V_{th} (V)	− 0.55	− 0.98
EOT (nm)	2.71	1.12
N_{eff} (cm^{-2})	3.99×10^{10}	4.71×10^{10}
|J| (A/cm^2)	4.47×10^{-7}	1.02×10^{-6}

Temperature stability measurement test has been performed with temperature variation ranging from 25 °C to 120 °C in negative voltage (− 5 to 0 V) bias (onset of depletion region to the accumulation region), as shown in Fig. 4c. The gate leakage current density–voltage (|*J*|–*V*) characteristics (plots) are measured with 10 °C increment in temperature. The leakage current density increases from ~ 4.47×10^{-7} A/cm^2 at 25 °C to ~ 2.28×10^{-6} A/cm^2 at 120 °C. To establish the effect of CVS on leakage current density of $Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt$ MIS structures, positive bias (+ 1 V, + 2 V, + 5 V) and negative bias (− 1 V, − 2 V, − 5 V) stresses are applied to positive voltage (0 V to + 5 V) bias in inversion region as shown in Fig. 4d. As clearly indicates that there is an insubstantial decrease of leakage current density at 1 V with the application of − 5 V negative CVS. To summarize, positive and negative CVS, temperature and sweep delay measurement tests for $Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt$ MIS devices, there is insignificant variation in *C–V* and |*J*|–*V* characteristics. Hence, the $Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt$ MIS devices are supporting towards stable and reliable real-world logic applications.

For practical applications, data retention in DRAM devices is of primary importance. Figure 5a presents the



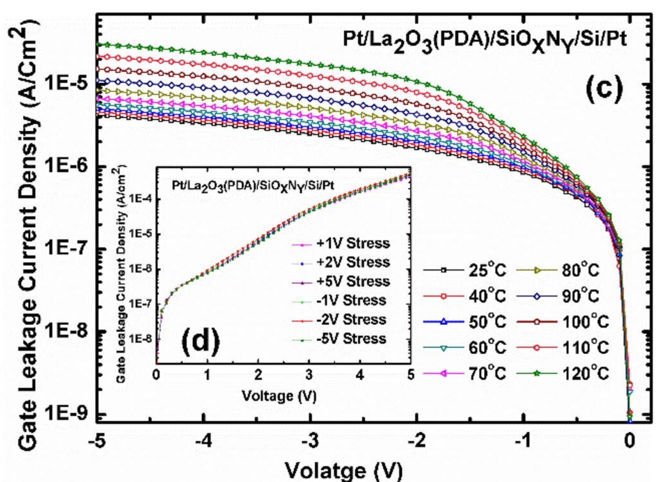


Fig. 4 Stability and reliability tests of $Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt$ MIS structures. **a** *C–V* characteristics with variable CVS (+ 1 V, + 5 V, + 10 V, − 1 V, − 5 V, − 10 V). **b** (inset) *C–V* characteristics with variable sweep delay (0.01 V/s, 0.05 V/s, 0.1 V/s, 0.2 V/s, 0.4 V/s). **c** *I–V* characteristics with variable temperature (25 °C to 120 °C) with 10 °C step. **d** (inset) *I–V* characteristics with variable electrical stress (+ 1 V, + 2 V, + 5 V, − 1 V, − 2 V, − 5 V)

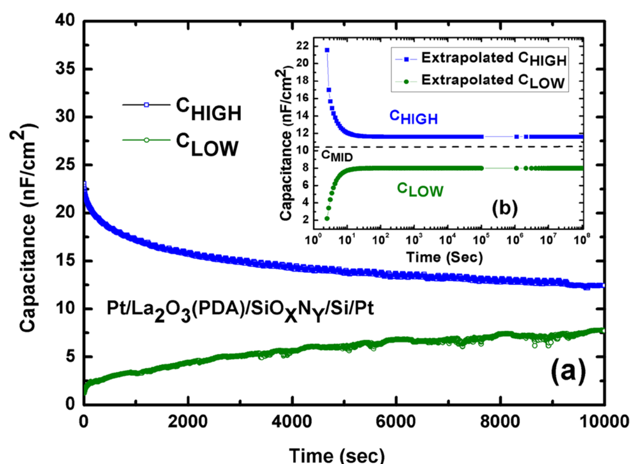


Fig. 5 **a** Capacitance–time (*C–t*) retention characteristics of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures. **b** (inset) *C–t* characteristics (extrapolated)

retention behaviour of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures through capacitance–time (*C–t*) retention characteristics at room temperature. In this characterization, a "write" voltage pulse of + 5 V for low capacitance state (C_{LOW}) and − 7 V for high capacitance state (C_{HIGH}) for the duration of 100 ms is applied to MIS devices. Mid capacitance (C_{MID}) is ((C_{HIGH} + C_{LOW})/2), a straight line defined at middle of C_{HIGH} and C_{LOW}. The high and low capacitance values are measured separately as a function of time, keeping the "read" bias voltage at − 1.5 V near V_{fb} of Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS devices. Initially, the C_{HIGH} and C_{LOW} capacitances decay exponentially and lose almost ~ 25% of charge within first 1000 s and later decays linearly with time. C_{HIGH} and C_{LOW} capacitances remain clearly distinguishable till ~ 10^4 s with considerable difference in capacitance magnitude ($\Delta C = C_{HIGH} - C_{LOW}$) as shown in Fig. 5a. The difference ΔC remains evident even when experimental data are extrapolated to ~ 10^8 s, as shown in Fig. 5b (inset). Hence, Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures show good data retention characteristics up to ~ 12 years, which make them suitable candidates for reliable logic integrated circuits.

3.2 Structural characterizations

X-ray photoelectron spectroscopy (XPS), a non-destructive method, has been employed to investigate the interface, chemical states, bonding structure and presence of different species in SiO_XN_Y/Si film interface as shown in Fig. 6. A wide scan XPS survey is performed to confirm the presence of different species and then detailed high-resolution spectra are performed for component species regions. The wide scan survey of the ultrathin SiO_XN_Y film reveals the presence of Si2p (Fig. 6d), O1s (Fig. 6f) and N1s (Fig. 6h) level regions. Carbon peak may appear due to hydrocarbon contamination. XPS Depth profile study of ultrathin SiO_XN_Y/Si film has been performed as shown in Fig. 6a, b, c, e, g to investigate atomic concentration profile of different species at different depth levels in the SiO_XN_Y/Si thin film. Depth profile of XPS study is performed by etching the surface by low-energy Ar ions for about 10 s repeatedly, until the films interface and underneath substrate is approached. XPS depth spectra of Si2p (Fig. 6c), O1s (Fig. 6e) and N1s (Fig. 6g) are measured after every etch cycle. Figure 6a shows the depth profile of Si2p, O1s and N1s atomic concentrations in SiO_XN_Y/Si ultrathin film measured by XPS as a function of sputter time. When the etch rate is set at ~ 0.1 nm/s, it is observed from the Fig. 6a that initially O1s concentration starts to descend with increase in etch time and Si2p concentration starts to ascend. The N1s concentration is relatively lower as compared to O1s and Si2p concentrations. SiO_XN_Y/Si interface is reached at ~ 0.70 min sputter time, giving the SiO_XN_Y thickness to be ~ 4.2 nm. At the SiO_XN_Y/Si interface, O1s and Si2p have reached ~ 50% atomic concentrations each. It is evident that, at the end of 5 min, Si2p and O1s have reached ~ 100% and ~ 0% atomic concentrations, respectively. Figure 6b (inset) shows the normalized atomic concentration vs sputter time plot. Starting with bulk SiO_XN_Y film at zero min sputter time, N1s is at ~ 40% concentration relative to other concentrations at the SiO_XN_Y/Si interface. With the increase in the sputter time to ~ 0.7 min, N1s increases to ~ 100% concentration, indicating maximum nitrogen concentration at the SiO_XN_Y/Si interface. Now, with further increase in sputter time from ~ 0.8 to ~ 3 min, the N1s concentration gradually decreases to ~ 20% and with sputter time beyond ~ 3 min, N1s is reduced to ~ 1% concentration. Hence, the N1s depth profile reveals the presence of less nitrogen concentration in the bulk of SiO_XN_Y film as compared to nitrogen concentration at the SiO_XN_Y/Si interface, whereas more O1s concentration is present in the bulk of the SiO_XN_Y film as compared to the SiO_XN_Y/Si interface. This increase in intensity of nitrogen concentration as an increasing function of depth towards the SiO_XN_Y/Si interface could be due to high stress at the SiO_XN_Y/Si interface. Due to lattice mismatch, at the SiO_XN_Y/Si interface, more nitrogen vacancies arise, whereas as we move towards the bulk SiO_XN_Y film, stress is reduced and hence the number of nitrogen vacancies decreases [44].

As shown in Fig. 6d, (inset) XPS core level Si2p spectra of SiO_XN_Y film obtain two binding energy peaks: (1) at 99.7 eV showing Si–Si bonding mostly in silicon substrate and (2) at 103.5 eV showing Si–O–Si bonding [45]. From the depth profile of Si2p at different etch levels as shown in (Fig. 6c), it is evident that after ~ 300 s of etching top SiO_XN_Y layer, intensity of first peak at 99.7 eV becomes stronger as compared to its intensity at start of etching profile, whereas the intensity of second peak at 103.5 eV

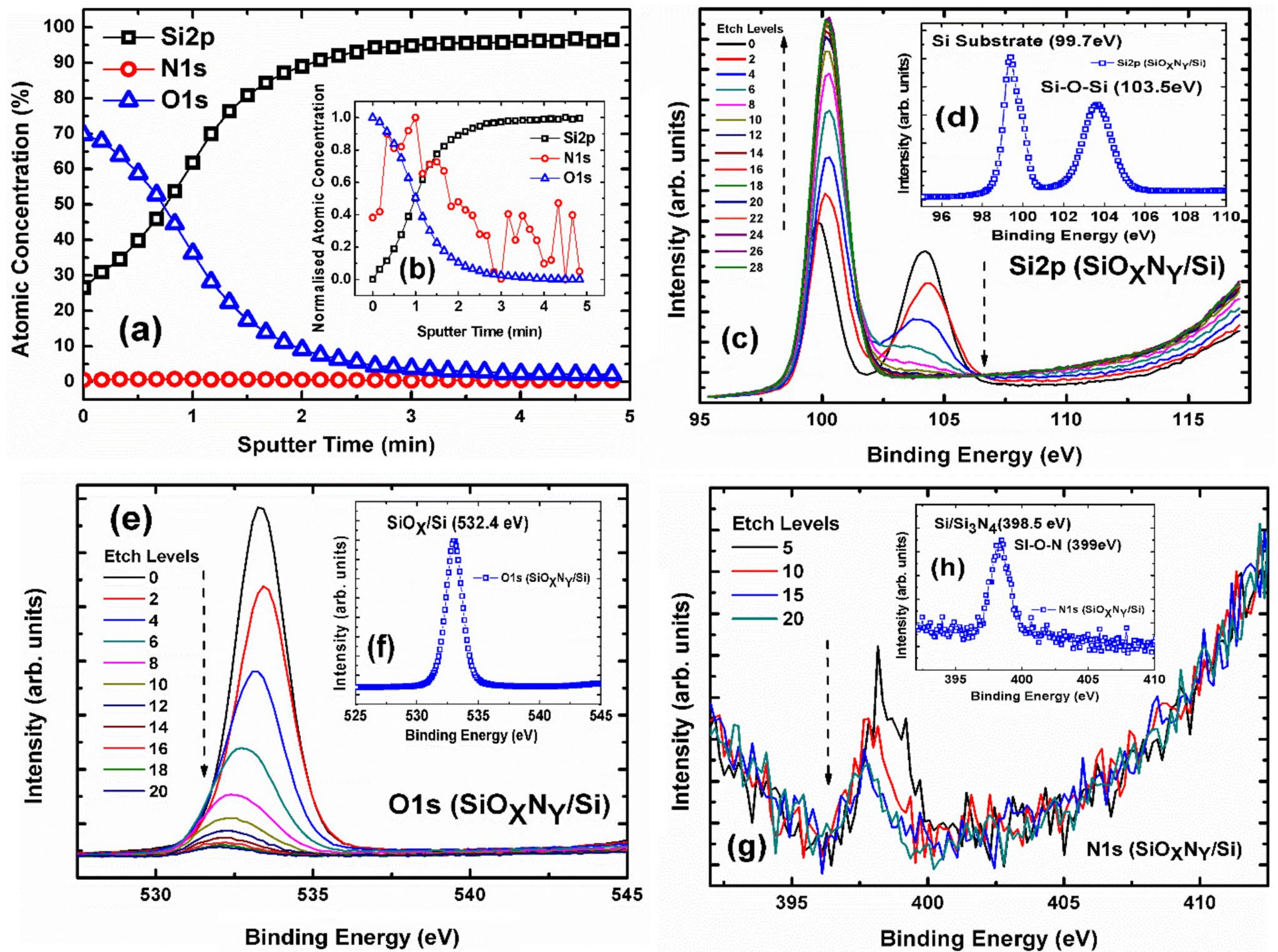


Fig. 6 XPS depth profile of SiO_XN_Y/Si interface. **a** % atomic Si2p, O1s and N1s concentrations vs sputter time (min). **b** (inset) Normalized atomic Si2p, O1s and N1s concentrations vs sputter time (min). **c** Depth etch profile of Si2p. **d** (inset) XPS core level Si2p spectra. **e** Depth etch profile of O1s. **f** (inset) XPS core level O1s spectra. **g** Depth etch profile of N1s. **h** (inset) XPS core level N1s spectra

diminishes after ~ 300 s etch time. This shows that SiO_XN_Y layer is fully etched, exposing the bare wafer with Si–Si bonding, and no Si–O–Si bond remains.

As shown in Fig. 6f, (inset) XPS core level O1s spectra in SiO_XN_Y film obtain single peak at 532.4 eV showing SiO_X/Si bonds [46]. From the depth profile of O1s at different etch levels (Fig. 6e), it is evident that after ~ 200 s of etching top SiO_XN_Y layer, intensity of peak at 532.4 eV completely diminishes. This again confirms that SiO_XN_Y layer is fully etched and no Si–O–Si bond remains. With increasing etch levels, decrease in the intensity of O1s peak is observed, with no shift in O1s peak spectra taken deeper in the SiO_XN_Y/Si film. As shown in Fig. 6h, (inset) XPS core level N1s spectra in SiO_XN_Y film obtain the form of multi-component peak behaviour deconvoluted to peaks at 398.5 and 399 eV showing Si_3N_4/Si bonds and Si–O–N bonding in different form such as O–N–Si_2 [47, 48]. Hence, this spectrum confirms the presence of SiO_XN_Y interfacial layer for SiO_XN_Y/Si system. From the depth profile of N1s at different etch levels (Fig. 6g), it is evident that after ~ 200 s of etching top SiO_XN_Y layer, intensity of peak at 398.5 and 399 eV disappears and approaches to the silicon substrate. A slight shift of N1s peak toward the lower binding energy is observed at the higher etch levels in the SiO_XN_Y/Si film. This indicates the change in chemical environment of nitrogen deeper into the bulk SiO_XN_Y film compared to chemical environment of nitrogen at or near the SiO_XN_Y/Si interface [44].

Figure 7a–d shows the 2D and 3D AFM tapping mode images (4 × 4 μm^2) for the La_2O_3 and SiO_XN_Y thin dielectric layers over p-Si ⟨100⟩ wafers, respectively. The figures clearly depict that La_2O_3 and SiO_XN_Y thin films are distributed all over the sample surface, and the height profile analysis of the individual film measures r.m.s surface roughness of ~ 1.11 ± 0.39 nm and ~ 0.97 ± 0.11 nm for La_2O_3/Si and SiO_XN_Y/Si thin films, respectively. The lesser surface roughness of SiO_XN_Y/Si thin films as compared to La_2O_3/Si

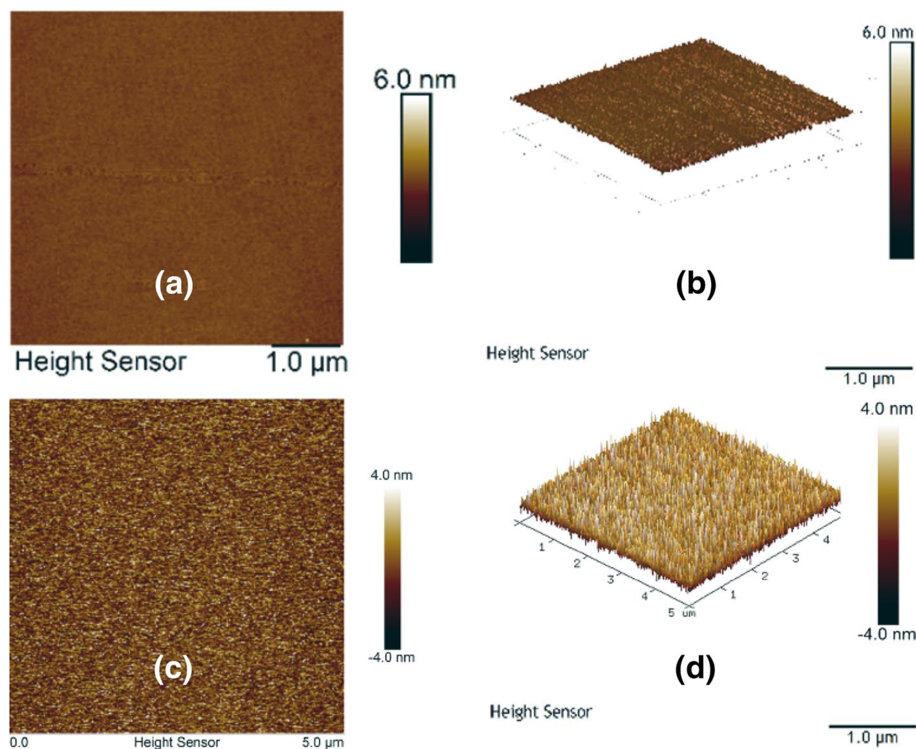


Fig. 7 AFM 2D and 3D image of **a**, **b** La_2O_3/Si thin film and **c**, **d** SiO_XN_Y/Si ultrathin film, respectively

thin films clearly indicates the improved La_2O_3/SiO_XN_Y/Si interface for MIS structures.

4 Conclusion

To summarize, RF sputtered high-κ lanthanum (III) oxide (La_2O_3) layer and rapid thermally oxidized (RTO) ultrathin silicon oxynitride (SiO_XN_Y) interfacial layer have been deposited to fabricate Pt/La_2O_3/SiO_XN_Y/p-Si/Pt MIS structures for CMOS applications. Electrical parameters extracted from C–V, |J|–V and G–V characteristics of Pt/La_2O_3/SiO_XN_Y/Si/Pt MIS structures show significant improvement in insulator–semiconductor La_2O_3/Si interface with the incorporation of ultrathin SiO_XN_Y interfacial layer. Positive gate bias side shift in flat-band voltage (V_{fb}) and in threshold voltage (V_{th}), by the incorporation of ultrathin SiO_XN_Y interfacial layer, indicates reduction in effective positive oxide charges at La_2O_3/SiO_XN_Y/Si interface. There is ~ 56.8% reduction in gate leakage current density extracted from |J|–V characteristics. Current conduction mechanism extracted from $\ln(J) - \ln(E)$ and $\ln(J/E^2) - 1/E$ characteristics show partially direct tunnelling current at low field E and Fowler–Nordheim tunnelling current at high field E regions. There is ~ 44.4% reduction in FWHM of G–V characteristics revealing reduction in interface states localized at La_2O_3/SiO_XN_Y/Si interface for Pt/La_2O_3(PDA)/SiO_XN_Y/Si/Pt MIS structures. C–t retention, temperature stability and stress reliability measurement tests show improved C–V and |J|-V characteristics to obtain also decent retention up to ~ 12 years. Depth profile XPS analysis of SiO_XN_Y/Si interface reveals decrease in intensity of nitrogen peak as a function of SiO_XN_Y depth, where nitrogen concentration is less in the bulk SiO_XN_Y as compared to SiO_XN_Y/Si interface. Less surface roughness of SiO_XN_Y/Si as compared to La_2O_3/Si thin films is measured using tapping mode AFM and EOT ~ 2.71 nm of gate dielectric La_2O_3/SiO_XN_Y stack has been confirmed by ellipsometry. The fabricated Pt/La_2O_3/SiO_XN_Y/p-Si/Pt MIS structures show enhanced electrical performance over Pt/La_2O_3/p-Si/Pt MIS structures. These MIS structures incorporating ultrathin SiO_XN_Y interfacial layer demonstrate its potential for use in stable and reliable CMOS logic devices and integrated circuits.

Acknowledgements The authors would like to strongly acknowledge Centre for Design and Fabrication of Electronic Devices (C*4*DFED), and Advanced Materials Research Centre (AMRC), Indian Institute of Technology (IIT) Mandi, India, for the use of various state-of-the-art device fabrication and characterization facilities for present work. Author Prachi Gupta would like to thank 'INSPIRE Ph.D. Fellowship Programme (research fellowship) support from Department of Science and Technology (DST) Govt. of India.

References

1. A.I. Kingon, J.P. Maria, S.K. Streiffer, Nature **406**, 1032 (2000)
2. J.M.A.G.D. Wilk, R.M. Wallace, Appl. Phys. Rev. **89**, (2001)
3. J. Robertson, Eur. Phys. J. Appl. Phys. **28**, 265 (2004)

4. R. Khosla, S.K. Sharma, J. Vac. Sci. Technol. B **36**, 012201 (2018)
5. J. Robertson, R.M. Wallace, Mater. Sci. Eng. R **88**, 1 (2015)
6. B.H. Lee, S.C. Song, R. Choi, P. Kirsch, IEEE Trans. Electron. Devices **55**, 8 (2008)
7. J. Robertson, Rep. Prog. Phys. **69**, 327 (2006)
8. H. Iwai, S. Ohmi, S. Akama, C. Ohshima, A. Kikuchi, I. Kashiwagi, J. Taguchi, H. Yamamoto, J. Tonotani, Y. Kim, I. Ueda, A. Kuriyama, Y. Yoshihara, *IEEE Int. Electron. Devices Meet.* (2002), pp. 625–628
9. K. Yim, Y. Yong, J. Lee, K. Lee, H. Nahm, J. Yoo, C. Lee, C.S. Hwang, S. Han, Nat. NPG Asia Mater. **7**, 1 (2015)
10. R. Khosla, P. Kumar, S.K. Sharma, IEEE Trans. Device Mater. Reliab. **15**, 610 (2015)
11. F.-C. Chiu, H.-W. Chou, J.Y.-M. Lee, J. Appl. Phys. **97**, 103503 (2005)
12. J. Robertson, J. Appl. Phys. **104**, 124111 (2008)
13. S. Abermann, C. Henkel, O. Bethge, E. Bertagnolli, Proc. 10th Int. Conf. Ultim. Integr. Silicon, ULIS (2009)
14. E.P. Gusev, V. Narayanan, M.M. Frank, IBM J. Res. Dev. **50**, 387 (2006)
15. B. Sen, B.L. Yang, H. Wong, C.W. Kok, M.K. Bera, P.K. Chu, A. Huang, K. Kakushima, H. Iwai, *IEEE Conference on Electron Devices and Solid-State Circuits* (IEEE, Tainan, 2007)
16. W. Kim, W.J. Maeng, K. Moon, J. Myoung, H. Kim, Thin Solid Films **519**, 362 (2010)
17. X. Wang, H. Liu, C. Fei, L. Zhao, S. Chen, S. Wang, AIP Adv. **6**, 065224 (2016)
18. R. Khosla, E.G. Rolseth, P. Kumar, S.S. Vadakupudhupalayam, S.K. Sharma, J. Schulze, IEEE Trans. Device Mater. Reliab. **17**, 80 (2017)
19. T. Perng, C. Chien, C. Chen, M. Yang, P. Lehnen, C. Chang, T. Huang, IEEE Trans. Electron. Devices **25**, 784 (2004)
20. T. Wang, C. Chang, J. Hwu, IEEE Sens. J **6**, 1468 (2006)
21. H. Uribe-vargas, J. Molina-reyes, E. Ortega, A. Ponce, IEEE Electron. Device Lett. **39**, 1461 (2018)
22. Y. Zhao, K. Kita, K. Kyuno, A. Toriumi, Appl. Phys. Lett. **94**, 042901 (2009)
23. H. Jin, S.K. Oh, H.J. Kang, Surf. Interface Anal. **38**, 1564 (2006)
24. D.A. Buchanan, IBM J. Res. Dev. **43**, 245 (1999)
25. J.R. Pfiester, F.K. Baker, T.C. Mele, H.-H. Tseng, P.J. Tobin, J.D. Hayden, J.W. Miller, C.D. Gunderson, L.C. Parrillo, IEEE Trans. Electron. Devices **37**, 842 (1990)
26. D. Mathiot, A. Straboni, E. Andre, P. Debenest, J. Appl. Phys. **73**, 8215 (1993)
27. E.P. Gusev, H.-C. Lu, E.L. Garfunkel, T. Gustafsson, M.L. Green, IBM J. Res. Dev. **43**, 265 (1999)
28. T. Ando, Materials (Basel). 478 (2012)
29. B. Balland, A. Glachant, *Instabilities in Silicon Devices* (Elsevier, Amsterdam, 1999)
30. C.V. Ramana, R.S. Vemuri, V.V. Kaichev, V.A. Kochubey, A.A. Saraev, V.V. Atuchin, ACS Appl. Mater. Interfaces **3**, 4370 (2011)
31. R. Leitsmann, F. Lazarevic, M. Drescher, E. Erben, J. Appl. Phys. **121**, 234501 (2017)
32. Nicollian and Brews, *MOS Physics and Technology* (Wiley Interscience, New York, 2003)
33. M.L. Green, E.P. Gusev, R. Degraeve, E.L. Garfunkel, J. Appl. Phys. **90**, 2057 (2001)
34. K. Kakushima, K. Tachi, M. Adachi, K. Okamoto, S. Sato, J. Song, T. Kawanago, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, Solid State Electron. **54**, 715 (2010)
35. K. Kakushima, T. Seki, H. Wakabayashi, K. Tsutsui, H. Iwai, Vacuum **140**, 14 (2017)
36. R. Perera, A. Ikeda, R. Hattori, Y. Kuroki, Thin Solid Films **423**, 212 (2003)
37. M. Soni, A. Soni, S.K. Sharma, Org. Electron. **51**, 48 (2017)
38. F.M. Fowkes, D.W. Hess, Appl. Phys. Lett. **377**, 1 (1973)
39. D.K. Schroder, *Semiconductor Material and Device Characterization* (Wiley, New York, 2006)
40. R. Khosla, D.K. Sharma, K. Mondal, S.K. Sharma, Appl. Phys. Lett. **105**, 152907 (2014)
41. P.K. Bhatnagar, S.R. Dhariwal, G.P. Srivastava, Phys. Status Solidi **67**, 305 (1981)
42. R. Clerc, P.O. Sullivan, K.G. Mccarthy, G. Ghibaudo, G. Pananakakis, A. Mathewson, Solid State Electron. **45**, 1705 (2001)
43. M. Shukla, G. Dutta, R. Mannam, N. Dasgupta, Thin Solid Films **607**, 1 (2016)
44. M.B. Haider, Nanoscale Res. Lett. **12**, 1 (2017)
45. Z. Zhuo, Y. Sannomiya, Y. Kanetani, T. Yamada, H. Ohmi, H. Kakiuchi, K. Yasutake, Nanoscale Res. Lett. **201**, 1 (2013)
46. M. Delfino, S. Salimian, D. Hodul, A. Ellingboe, W. Tsai, J. Appl. Phys. **71**, 1001 (1992)
47. M.S. Donley, D.R. Baer, T.G. Stoebe, Surf. Interface Anal. **11**, 335 (1988)
48. S. Alexandrova, E. Halova, S. Bakalova, A. Szekeres, A. Marin, P. Osiceanu, M. Gartner, N. Koujuharova, J. Phys. **514**, 012035 (2014)

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

View publication stats